3A, 5.5V, Low IQ ACOT Synchronous Step-Down Converter

General Description

The ET83301 is a full featured 5.5V, 3A, Advanced Constant-On-Time (ACOT) synchronous step-down converter with two integrated MOSFETs. The advanced COT operation allows transient responses to be optimized over a wide range of loads, and output capacitors to efficiently reduce external component count. The ET83301 provides up to 2MHz switching frequency to minimize the size of output inductor and capacitors. The ET83301 is available in the DFN8 (2mm×2mm) package.

Features

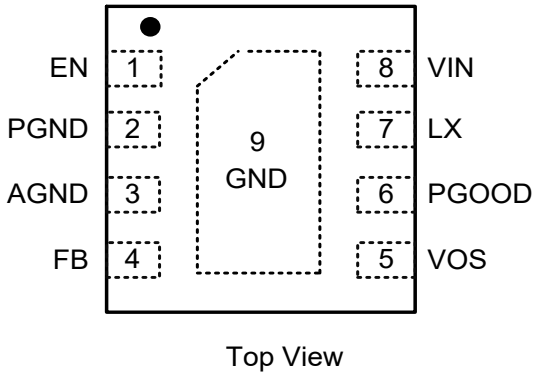
- 2.5V to 5.5V Input Voltage Range
- Advanced Constant On-Time ACOT Control
  - Ultra fast Transient Response
  - No Needs for External Compensations
  - Optimized for Low-ESR Ceramic Output
- Capacitors Fast Transient Response
- Internal 100mΩ and 70mΩ Synchronous Rectifier
- Steady Switching Frequency: 2.0MHz
  - Automatic Power Saving Mode (PSM)
- Highly Accurate V_{OUT} Regulation Over Load / Line Range
- Robust Loop Stability with Low-ESR C_{OUT}
- Ambient Temperature Range of -40 °C to +85 °C
- ESD HBM ±2 KV PASS
- ESD CDM ±1KV PASS
- Input Undervoltage Lockout (UVLO)
- Output Undervoltage Protection (UVP) with Hiccup Mode
- Over-Temperature Protection (OTP)
- Power Good Indication
- Package Information:

Part No.	Package	Packing Option	MSL
ET83301	DFN8 (2mm×2mm)	Tape and Reel , 3K/Reel	Level 1

Application

- WLAN ASIC Power / Storage (SSD and HDD)
- General Purpose for POL LV Buck Converter
- Automotive Infotainment
- Automotive Instrument Clusters & HUD
- Car Connectivity

Pin Configuration

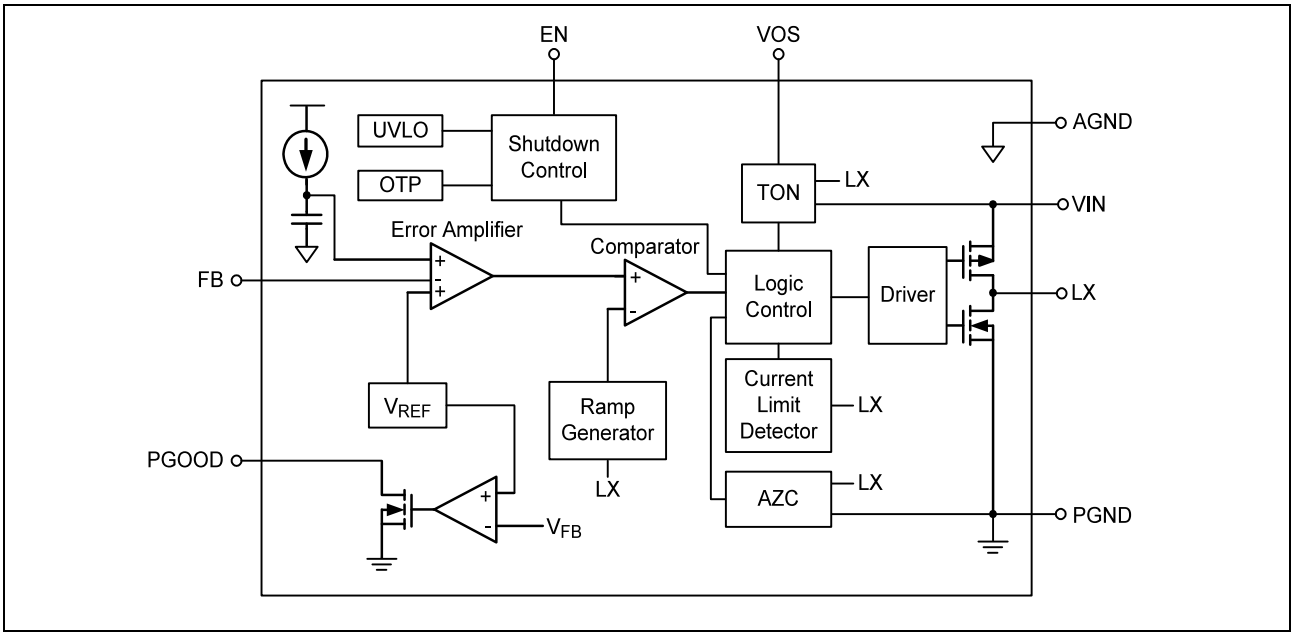


Top View

Pin Function

Pin NO.	Pin Name	Pin Function
1	EN	Enable control input. Pull high to enable
2,9	PGND	Power ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation
3	AGND	Analog ground. Should be electrically connected to GND close to the device
4	FB	Feedback voltage input
5	VOS	Output voltage sense pin for the internal control loop. Must be connected to output
6	PGOOD	Power good open-drain output. This pin is pulled to low if the output voltage is below regulation limits. Can be left floating if not used
7	SW	Switch node. The Source of the internal high-side power MOSFET, and Drain of the internal low-side (synchronous) rectifier MOSFET
8	VIN	Power input supply voltage, 2.5V to 5.5V

Block Diagram



Functional Description

The ET83301 is a low voltage synchronous step-down converter that can support input voltage ranging from 2.5V to 5.5V and the output current can be up to 3A. The ET83301 uses ACOT™ mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

In steady-state operation, the feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the equation1 :

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{OSC}} \quad (1)$$

where f_{OSC} is nominal 2MHz

Under-Voltage Protection (UVLO)

The UVLO continuously monitors the V_{CC} voltage to make sure the device works properly. When the V_{CC} is high enough to reach the UVLO high threshold voltage, the step-down converter softly starts or pre-bias to its regulated output voltage. When the V_{CC} decreases to its low threshold voltage, the device shuts down.

Power Good

When the output voltage is higher than PGOOD rising threshold, the PGOOD flag is high.

Output Under-Voltage Protection (UVP)

When the output voltage is lower than 66% reference voltage after soft-start, the UVP is triggered.

Over-Current Protection (OCP)

The ET83301 senses the current signal when the high-side and low-side MOSFET turns on. As a result, The OCP is a cycle-by-cycle current limit. If an over-current condition occurs, the converter turns off the next on pulse until inductor current drops below the OCP limit. If the OCP is continually activated and the load current is larger than the current provided by the converter, the output voltage drops. Also, when the output voltage triggers the UVP also, the current will drop to ZC and trigger the re-soft start sequence

Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft-start time is 200μs.

Over-Temperature Protection (OTP)

The ET83301 has an over-temperature protection. When the device triggers the OTP, the device shuts down until the temperature is back to normal.

Absolute Maximum Ratings(1)

Characteristic	Parameters	Value	Unit
V_{IN}	Supply Input Voltage	-0.3 to +7	V
	LX Pin Switch Voltage	-0.3 to (V_{IN} + 0.3)	V
	LX Pin Switch Voltage(< 100ns)	-5 to +9	V
	Other Pins	-0.3 to (V_{IN} + 0.3)	V
θ_{JA}	Package Thermal Resistance(2), DFN8(2×2)	31	°C/W
θ_{JC}		8	°C/W
T_{JMAX}	Max Junction Temperature	150	°C
T_L	Lead Temperature (Soldering, 10 sec)	260	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
V_{ESD}(3)	Human Body Model (JEDEC JS-001)	±2000	V
	Charged Device Model (JEDEC JS-002)	±1000	V

Recommended Operating Conditions(4)

Characteristic	Symbol	Min	Max	Unit
Supply Voltage Range	V_{IN}	2.5	5.5	V
Storage Junction Temperature	T_J	-40	125	°C
Ambient Temperature Range	T_A	-40	85	°C

Note1: Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note2: θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package. The copper area is 70mm² connected with IC exposed pad.

Note3: Devices are ESD sensitive. Handling precaution is recommended.

Note4: The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

Unless otherwise noted, V_{IN} = 3.6V, T_A = T_J = −40°C to 85°C.

Symbol	Parameters		Conditions	Min	Typ	Max	Unit
V_{UVLO}	Under-Voltage Lockout Threshold		V_{CC} rising		2.2		V
V_{UVLO_HY}	Under-Voltage Lockout Hysteresis				200		mV
I_{SHDN}	Shutdown Supply Current		EN = 0V			2	μA
I_Q	Quiescent Current		Active, V_{FB} = 0.5V, no switching		20		μA
V_{REF}	Voltage Reference			0.441	0.45	0.459	V
I_{LIM}	Current Limit	High-Side	Peak current		4.8		A
		Low-Side	Valley current		3.4		
V_{PGTH}	Power Good Threshold		V_{OUT} falling referenced to V_{OUT} nominal	-15	-10	-5	%
V_{PGHY}	Power Good Hysteresis		Hysteresis referenced to V_{OUT} nominal		5		%
I_{PG}	Power Good Leakage Current		V_{PG} = 5V		0.01	0.1	μA
V_{PGL}	Power Good Low Level Voltage		I_{sink} = 500μA			0.3	V
V_{ENH}	EN Threshold Voltage	H-Level	EN rising	1.2			V
V_{ENL}		L-Level	EN falling			0.4	V
$R_{P\text{-}MOSFET}$	Switch On-Resistance	High-Side			100		mΩ
$R_{N\text{-}MOSFET}$		Low-Side			70		
T_{SHDN}	Thermal Shutdown Temperature			130	150		°C
T_{SHDN_HYS}	Thermal Shutdown Hysteresis				20		°C
f_{OSC}	Switching Frequency				2		MHz
R_{DIS}	Output Discharge Resistor		EN = 0V, VOUT = 1.8 V		1		kΩ
$t_{ON(MIN)}$	Minimum on Time				58		ns

Application and Implementation

ETEK does not warrant its accuracy or completeness and Information in the following applications sections is not part of the ETEK component specification. Customers should be responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The ET83301 is a single-phase step-down converter. Advance Constant-on-Time (ACOT) with fast transient response. An internal 0.45V reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed switching frequency (2MHz) oscillator and internal compensation are integrated to minimize external component count. Protection features include over current protection, under voltage protection and over temperature protection.

Typical Application

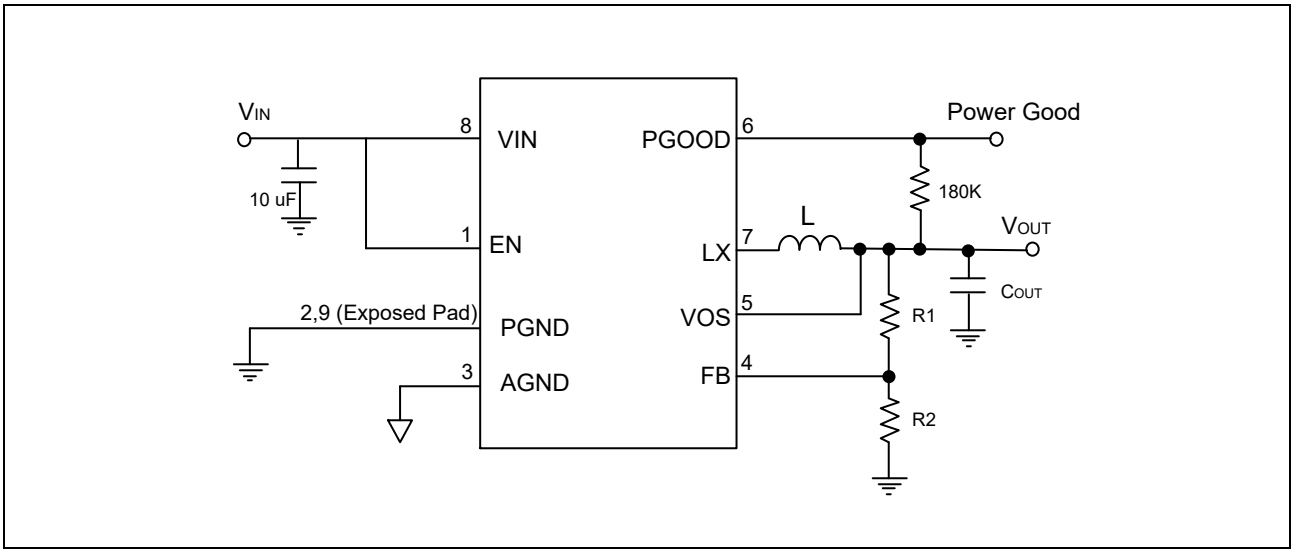


Table 1. Recommended Component Values

V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (μF)
1.2	65.3	39.2	1	22
1.8	117.6	39.2	1	22
2.5	178.6	39.2	1	22
3.3	248.3	39.2	1	22

Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation2 :

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2}) \quad (2)$$

where VREF equals to 0.45V typical. The resistive divider allows the FB pin to sense a fraction of the output voltage.

Low Supply Operation

The ET83301 is designed to operate down to an input supply voltage of 2.5V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-Channel and N-Channel power switches increases. The user should calculate the power dissipation when the ET83301 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Under Voltage Protection (UVP)

Hiccup Mode

For the ET83301, it provides Hiccup Mode Under Voltage Protection (UVP). When the output voltage is lower than 66% reference voltage after soft-start, the UVP is triggered. If the UVP condition remains for a period, the ET83301 will retry automatically. When the UVP condition is removed, the converter will resume operation. The UVP is disabled during soft-start period.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by equation3 :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1} \quad (3)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst case condition is commonly used for design because even significant deviations do not result in much difference. Choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by equation4:

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right] \quad (4)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR, but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects.

The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following equation5 :

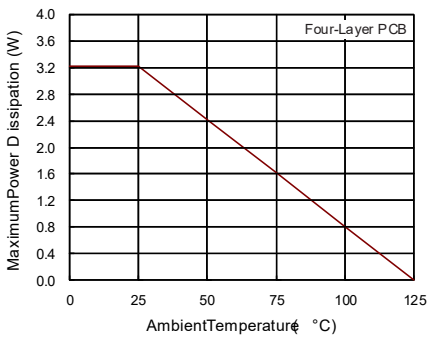
$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad (5)$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WSON8 package, the thermal resistance, θ_{JA}, is 31°C/W on a standard JEDEC 51-7 high effective-thermal conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below equation6 :

$$P_{D(MAX)} = (125°C - 25°C) / (31°C/W) = 3.22W \quad (6)$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

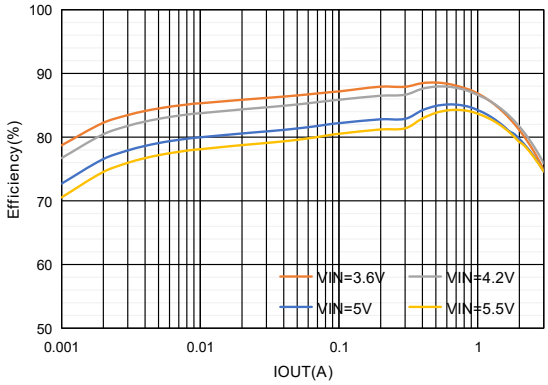


Derating Curve of Maximum Power Dissipation

Application Curves

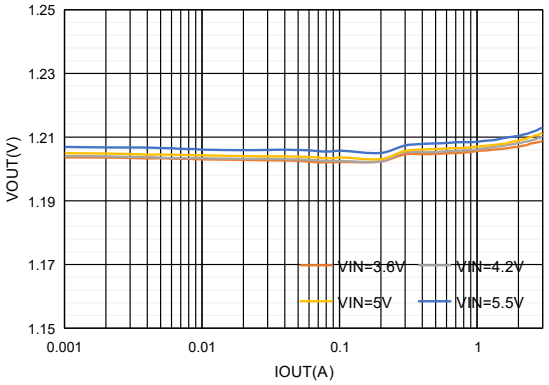
V_{IN} = 3.6V,V_{OUT}=1.2V T_A = +25°C (unless otherwise noted).

Figure1. Efficiency



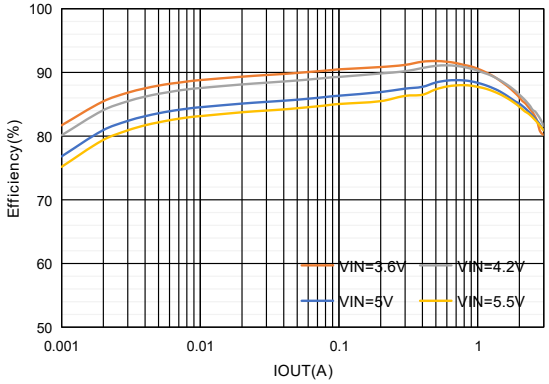
V_{OUT}=1.2V, L=1μH

Figure2. Load Regulation



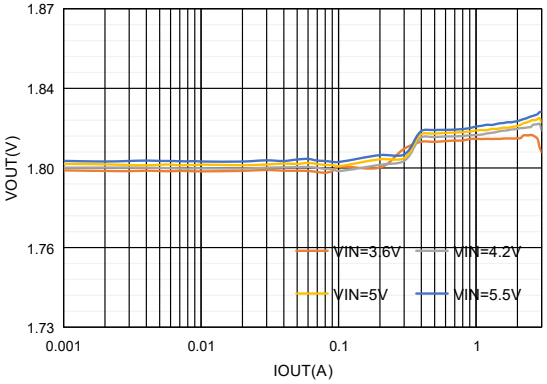
V_{OUT}=1.2V, L=1μH

Figure3. Efficiency



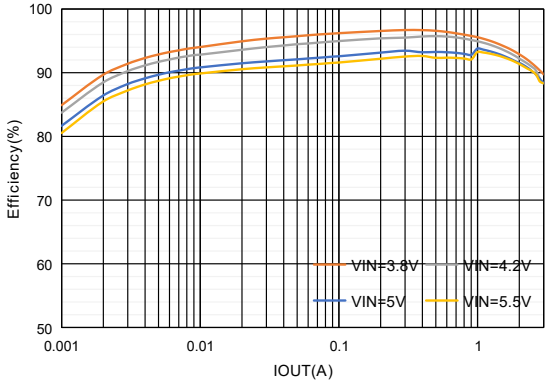
V_{OUT}=1.8V, L=1μH

Figure4. Load Regulation



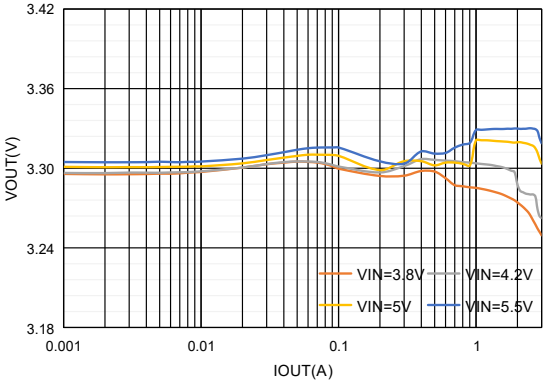
V_{OUT}=1.8V, L=1μH

Figure5. Efficiency



V_{OUT}=3.3V, L=1μH

Figure6. Load Regulation

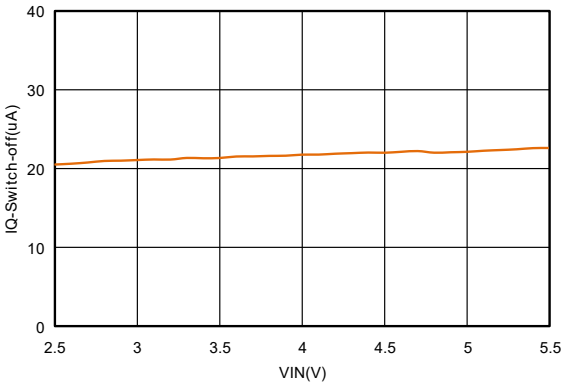


V_{OUT}=3.3V, L=1μH

Application Curves(Continued)

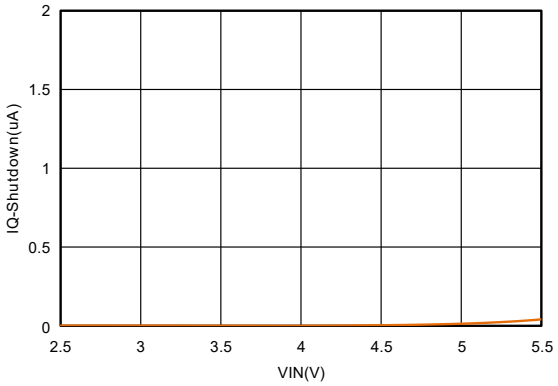
V_{IN} = 3.6V,V_{OUT}=1.2V T_A = +25°C (unless otherwise noted).

Figure7. Supply Current vs. Input Voltage



V_{EN}=2V, V_{FB}=0.5V

Figure8. Disabled Supply Current



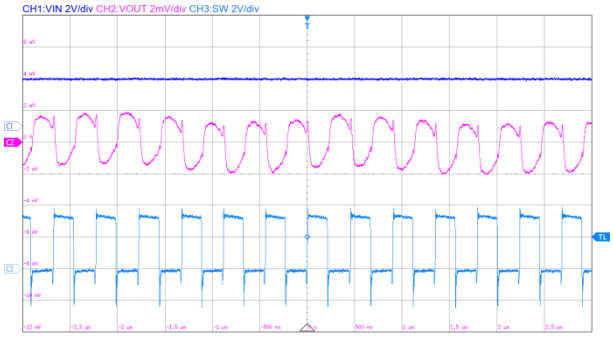
V_{EN}=0V

Figure9. Output Ripple vs. I_{OUT} = 0A



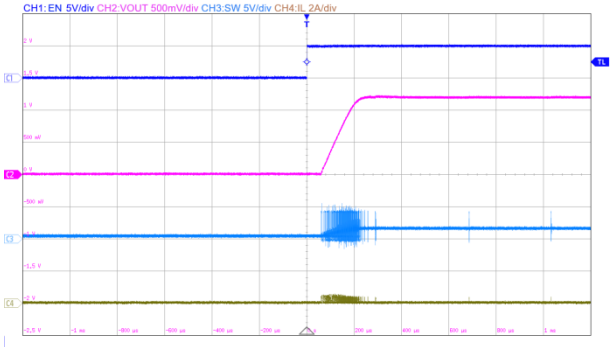
1ms/div

Figure10. Output Ripple vs. I_{OUT} = 3A



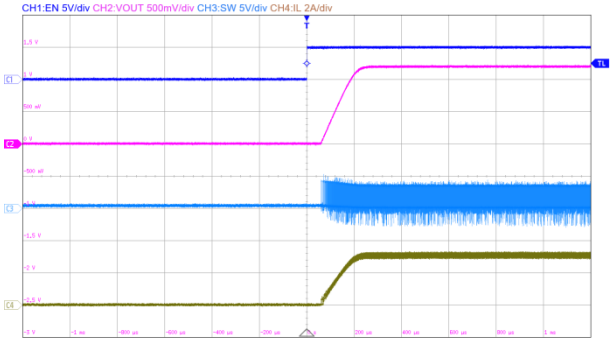
500ns/div

Figure11. Start-Up through Enable vs. I_{OUT} = 0A



200us/div

Figure12. Start-Up through Enable vs. I_{OUT} = 3A

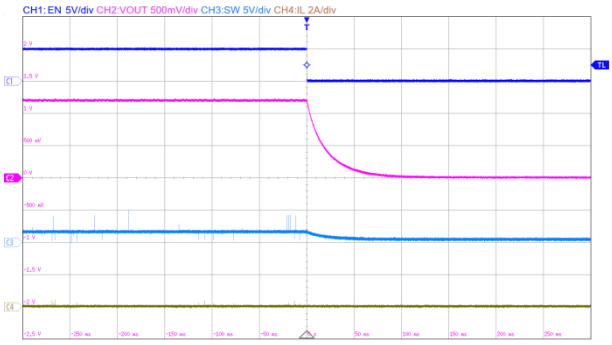


200us/div

Application Curves(Continued)

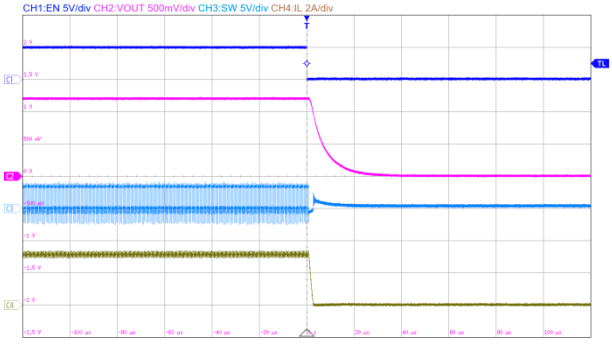
V_{IN} =3.6V,V_{OUT}=1.2V T_A = +25°C (unless otherwise noted).

Figure13. Shutdown through Enable vs. I_{OUT} = 0A



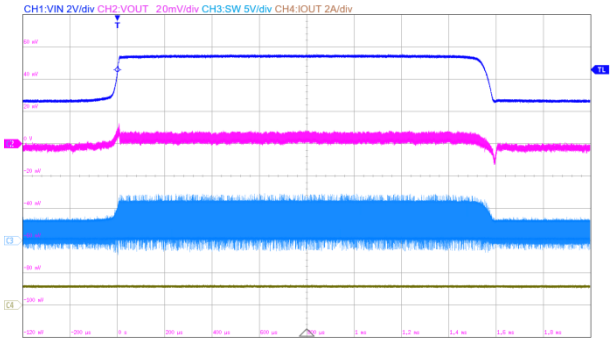
50ms/div

Figure14. Shutdown through Enable vs. I_{OUT} = 3A



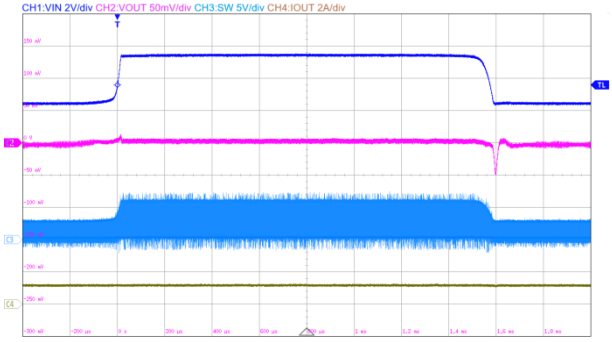
20us/div

Figure15. V_{IN} = 3.6V to 5.5V,V_{OUT}=1.2V
Line Transient Test



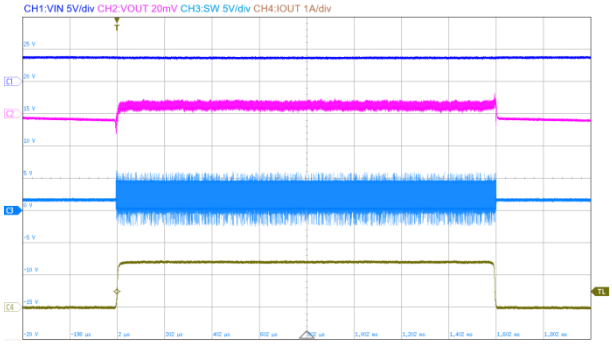
200us/div

Figure16. V_{IN} = 2.5V to 5.5V,V_{OUT}=1.2V
Line Transient Test



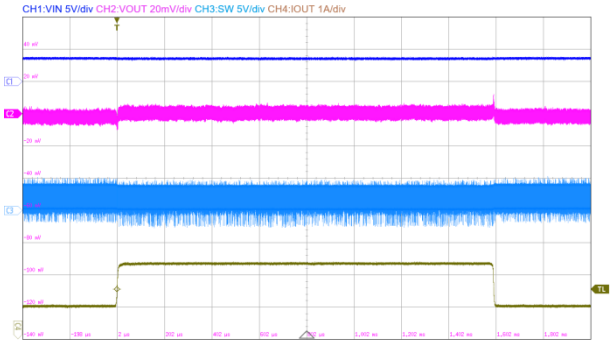
200us/div

Figure17. V_{IN} = 3.6V,V_{OUT}=1.2V I_{OUT} = 0A to 1.5A
Load Transient Test



200us/div

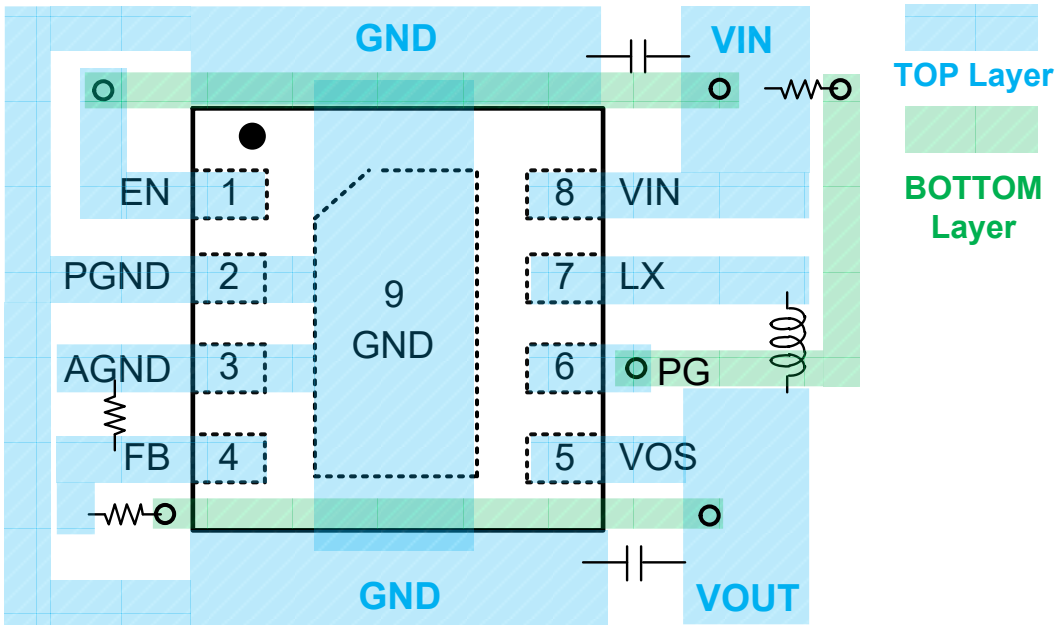
Figure18. V_{IN} = 3.6V,V_{OUT}=1.2V I_{OUT} = 1.5A to 3A
Load Transient Test



200us/div

Layout

Layout Example



* Circuit diagram is for reference only.

Layout Guidelines

Connect the terminal of the input capacitor(s), C_{IN}, as close as possible to the V_{IN} pin. This capacitor provides the AC current into the internal power MOSFETs.

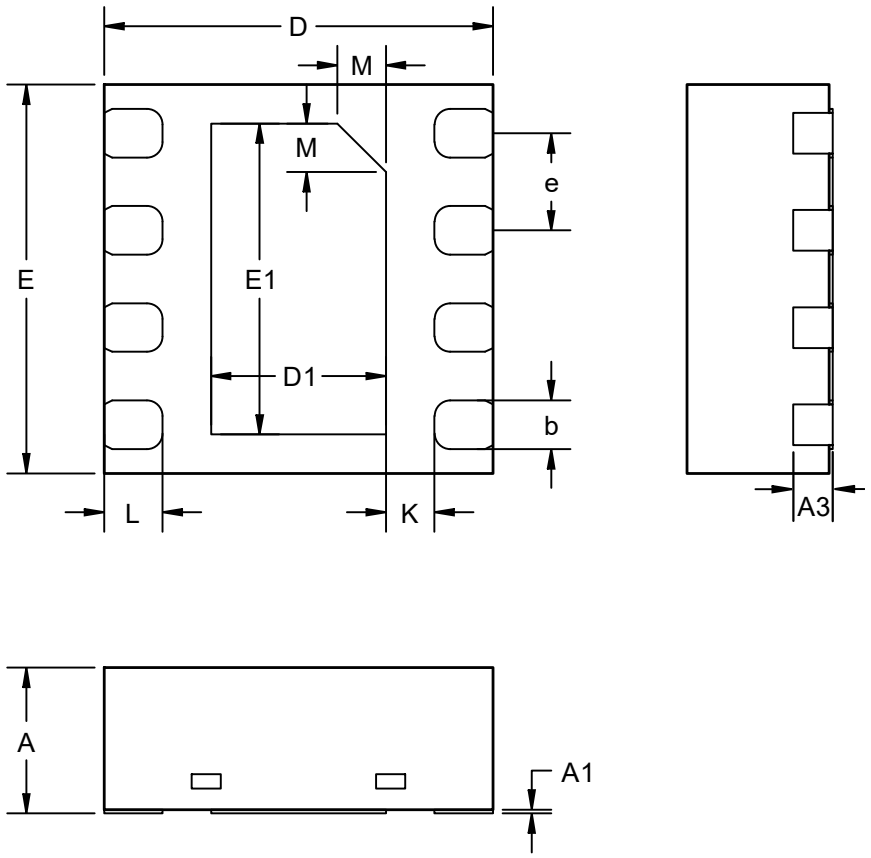
LX node experiences high frequency voltage swing and should be kept within a small area. Keep all sensitive small-signal nodes away from the LX node to prevent stray capacitive noise pick up.

Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN}, V_{OUT}, GND, or any other DC rail in the system).

Connect the FB pin directly to the feedback resistors. The resistive voltage divider must be connected between V_{OUT} and GND.

Package Dimension

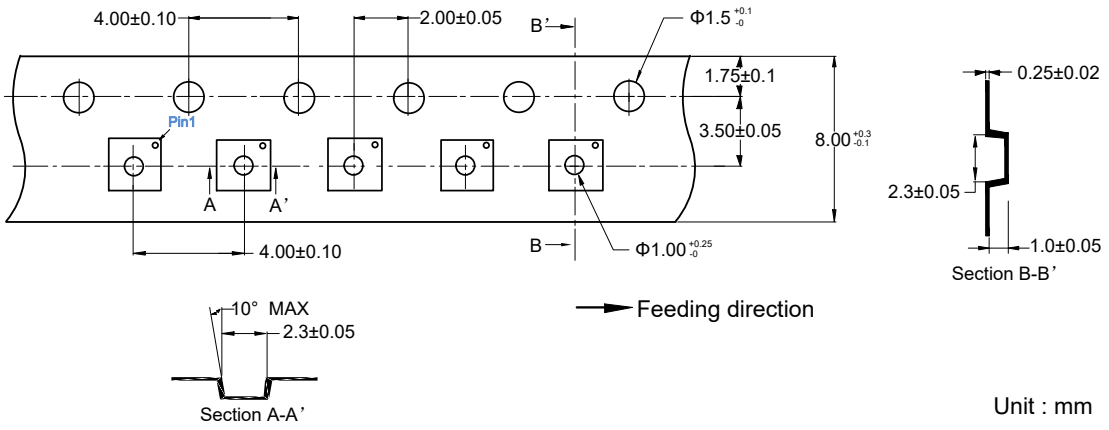
DFN8



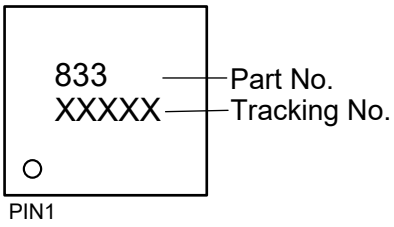
Dimensions Table (Units: mm)

Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D1	0.80	0.90	1.00
E1	1.50	1.60	1.70
e	0.40	0.50	0.60
K	0.15	0.25	0.35
L	0.25	0.30	0.35
M		0.25REF	

Tape Information



Marking



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024.01.16	Preliminary Version	Liwc	Wuhs	Liujy
0.1	2024.08.09	Preliminary Version	Caojc	Wuhs	Liujy
0.2	2026.07.22	Preliminary Version	Wangzw	Liuc	Liujy
1.0	2026.08.27	Officially Version	Wangzw	Liuc	Liujy
1.1	2026.09.23	Parameter Update	Wangzw	Liuc	Liujy
1.2	2026.11.05	Application Curves Update	Wangzw	Liuc	Liujy