# ET539XXYB - High PSRR Low Noise 300mA LDO

## General Description

The ET539XXYB family are the 300mA LDO with auto discharge function. It uses an advanced CMOS process and a PMOSFET pass device to achieve high power supply rejection ratio (PSRR), low noise, low dropout, low ground current, fast start-up and excellent output accuracy.

The ET539XXYB family are stable with a 1.0μF ceramic output capacitor, uses a precision voltage reference and feedback loop to achieve excellent regulation and transient response.

The ET539XXYB family offered in a small DFN4 package, which are ideal for small form factor portable equipment.

## Features

- Wide Input Voltage Range from 1.7V to 5.5V
- Up to 300mA Load Current
- Standard Fixed Output Voltage :1.1V,1.2V, 1.5V, 1.8V, 2.4V, 2.5V, 2.8V, 2.85V, 2.9V, 3.0V and 3.3V etc.
- Very Low $I_Q$ is 35μA Typical
- Low Dropout is Typical 400mV@1.8V at 300mA Load
- Very High PSRR: 75dB at 1KHz
- Very Low Noise is 45uVrms
- Excellent Load/Line Transient Response
- With Auto Discharging Function
- Part No. and Package Information

| Part No. | Package | MSL |
|---|---|---|
| ET539XXYB | DFN4 (1mm × 1mm) | Level 1 |

## Applications

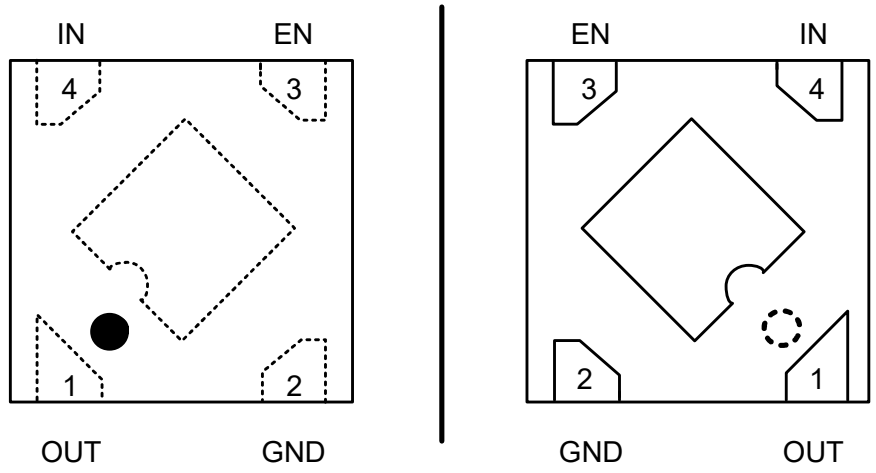
- Smart Phones and Cellular Phones
- Digital Still Cameras
- Portable Instrument

## Device Information

**ET 539 XX X B**

| **XX** Output Voltage | | **X** Package | | **B** Auto-Discharging Function |
|---|---|---|---|---|
| XX | Output Voltage<br>For example, 18 is 1.8V output | Y | DFN4 (1mm × 1mm) | B: With Auto-discharging Function |

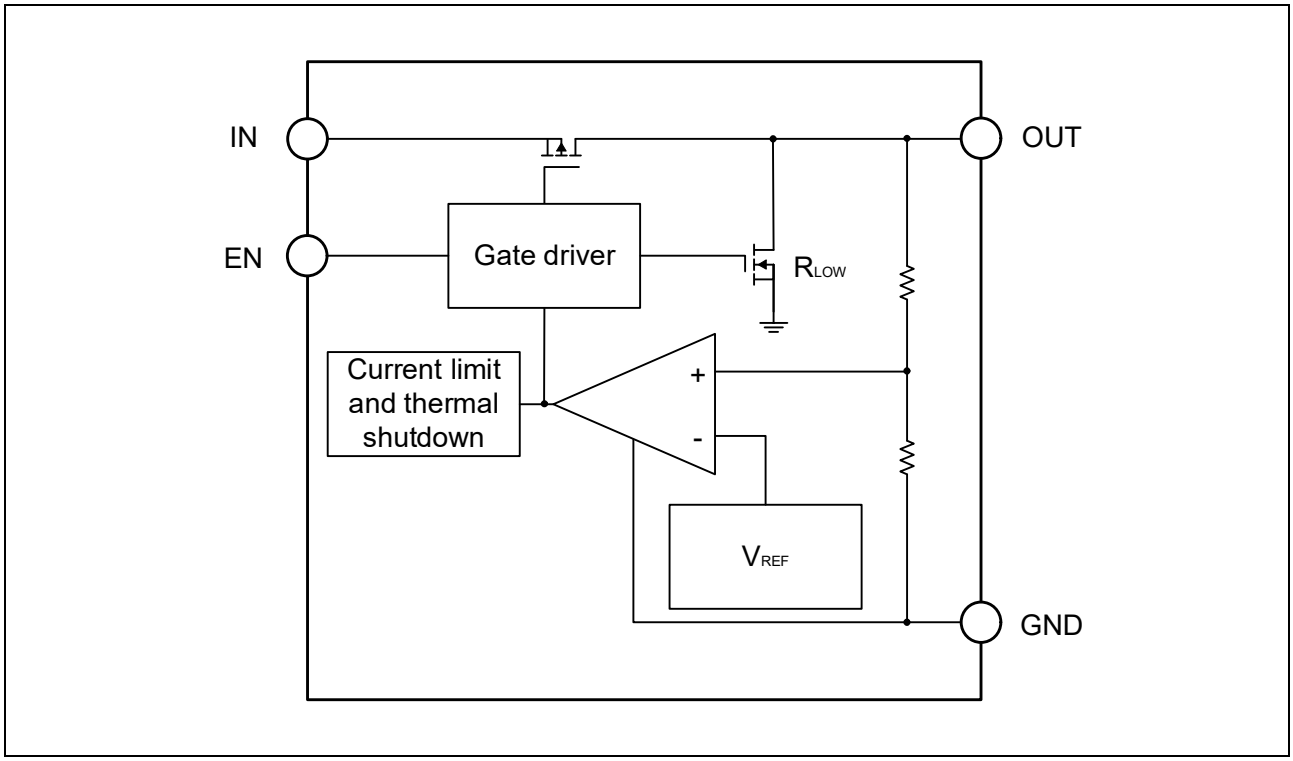
## Pin Configuration




## Pin Function

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | OUT | Output Pin. A low-ESR capacitor should be connected to this pin to GND. |
| 2 | GND | Ground Pin. |
| 3 | EN | Enable Control Input Pin, Active High. Do not leave EN floating |
| 4 | IN | Supply Input Pin. Must be closely decoupled to GND with a ceramic capacitor |

## Block Diagram




## Functional Description

### Input Capacitor

A 1μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

### Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 0.47μF to 4.7μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics is X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

### ON/OFF Input Operation

The ET539XXYB is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time.

### Ultra-Fast Start-up

After enabled, the ET539XXYB is able to provide full power in as little as tens of microseconds, typically 75μs. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

**Current Limit Protection**

When output current at the OUT pin is higher than current limit threshold or the OUT pin, the current limit protection will be triggered and clamp the output current to approximately 650mA to prevent over-current and to protect the regulator from damage due to overheating.

**Thermal shutdown Protection**

Thermal protection disables the output when the junction temperature rises to approximately +155°C, allowing the device to cool down. When the junction temperature reduces to approximately +125°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

## Absolute Maximum Ratings

| Symbol | Parameters (Items) | Value | Unit |
|---|---|---|---|
| $V_{IN}$ | IN Voltage | -0.3 to 6.0 | V |
| $V_{EN}$ | Input Voltage (EN Pin) | -0.3 to $V_{IN}$ + 0.3 | V |
| $V_{OUT}$ | Output Voltage | -0.3 to $V_{IN}$ + 0.3 | V |
| $P_D$ (1) | Maximum Power Consumption | 400 | mW |
| $V_{ESD}$ | Human Body Model (JEDEC JS-001) | ±2000 | V |
| | Charged Device Model (JEDEC JS-002) | ±1500 | |
| $L_U$ | JEDEC JESD78F | ±200 | mA |
| $R_{\theta JA}$ | DFN4 | 250 | °C/W |
| $T_J$ | Operating Junction Temperature | -40 to 150 | °C |
| $T_{STG}$ | Storage Temperature | -65 to 150 | °C |
| $T_{SL}$ | Lead Temperature (Soldering, 10 sec) | 300 | °C |

***Note1***: Test at $T_A$=25℃ with the component mounted on 5*5mm, FR4, 2layer, Top and Bottom layer 1oz.

## Recommended Operating Conditions

| Symbol | Parameters | Rating | Unit |
|---|---|---|---|
| $V_{IN}$ | Input Voltage | 1.7 to 5.5 | V |
| $I_{OUT}$ | Output Current | 0 to 300 | mA |
| $T_A$ | Operating Ambient Temperature | -40 to +85 | ºC |
| $C_{IN}$ | Effective Input Ceramic Capacitor Value | 0.47 to 4.7 | μF |
| $C_{OUT}$ | Effective Output Ceramic Capacitor Value | 0.47 to 4.7 | μF |
| ESR | Input and Output Capacitor Equivalent Series Resistance (ESR) | 5 to 100 | mΩ |

## Electrical Characteristics

($V_{IN}$ = $V_{OUT}$ + 1V, $V_{EN}$ = 1.2V, $I_{OUT}$ = 1mA, $C_{IN}$ = 1μF, $C_{OUT}$ = 1μF, Typical value test @$T_A$ = 25°C, unless otherwise stated)

| Symbol | Parameters | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ (2) | Input Voltage Range | | 1.7 | | 5.5 | V |
| $V_{OUT}$ | Regulated Output Voltage | $I_{OUT}$ = 1mA, -40°C ≤ $T_A$ ≤ 85°C | -1.5 | | +1.5 | % |
| $V_{DROP}$ (3) | Dropout Voltage | $V_{OUT}$ = 1.2V, $I_{OUT}$ = 300mA | | 650 | 850 | mV |
| | | $V_{OUT}$ = 1.8V, $I_{OUT}$ = 300mA | | 400 | 600 | |
| | | $V_{OUT}$ = 2.8V, $I_{OUT}$ = 300mA | | 390 | 510 | |
| | | $V_{OUT}$ = 2.9V, $I_{OUT}$ = 300mA | | 390 | 510 | |
| | | $V_{OUT}$ = 3.0V, $I_{OUT}$ = 300mA | | 380 | 510 | |
| | | $V_{OUT}$ = 3.3V, $I_{OUT}$ = 300mA | | 380 | 510 | |
| $I_{Q_ON}$ | Input Quiescent Current | Active Mode: $V_{EN}$ = $V_{IN}$ | | 35 | 70 | μA |
| $I_{Q\ OFF}$ | Input Shutdown Current | $V_{EN}$ = 0V | | 0.01 | 1 | μA |
| $Reg_{LINE}$ | Output Line Regulation | $V_{IN}$ = $V_{OUT}$ + 1V to 5.5V, $I_{OUT}$ = 10mA | | 0.02 | 0.1 | %/V |
| $Reg_{LOAD}$ | Output Load Regulation | $I_{OUT}$ from 0mA to 300mA | | 12 | 30 | mV |
| $T_{ON}$ | Soft-start Time | From Enable to 90%*$V_{OUT}$ | | 75 | 120 | μs |
| $I_{LIMIT}$ | Current Limit | | 350 | 650 | | mA |
| $I_{SHORT}$ | Short Current Limit | $V_{OUT}$ = 0V | | 55 | | mA |
| PSRR (4) | Power Supply Rejection Ratio | f = 1kHz, $C_{OUT}$ = 1μF, $I_{OUT}$ = 20mA | | 75 | | dB |
| | | f =10kHz, $C_{OUT}$ = 1μF, $I_{OUT}$ = 20mA | | 72 | | |
| $e_N$ (4) | Output Noise | 10Hz to 100kHz, $I_{OUT}$ = 20mA | | 45 | | $μV_{RMS}$ |
| $V_{IL}$ | EN Low Threshold | $V_{IN}$ = 1.7V to 5.5V, $V_{EN}$ Falling Until the Output is Disabled | | | 0.4 | V |
| $V_{IH}$ | EN High Threshold | $V_{IN}$ = 1.7V to 5.5V, $V_{EN}$ Rising Until the Output is Enabled | 0.9 | | | V |
| $I_{EN}$ | EN Pin Input Current | $V_{EN}$ = 0V | | 0 | 0.1 | μA |
| $R_{PD}$ | EN pull-down Resistance | $T_A$ = 25°C | 0.8 | 1 | 1.2 | MΩ |
| $R_{LOW}$ | Output Resistance of Auto Discharge at Off State | $V_{EN}$ = 0V, $V_{IN}$ = $V_{OUT}$ = 4V | | 35 | | Ω |
| $T_{TSD}$ (4) | Over-temperature Shutdown Threshold | $T_J$ Rising | | 155 | | °C |
| $T_{HYS}$ (4) | Over-temperature Shutdown Hysteresis | $T_J$ Falling from Shutdown | | 30 | | °C |

***Note2*:** The maximum input voltage should take into account the maximum power consumption ($P_{D(MAX)}$). The calculation formula is as follows:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT}$$

The maximum power consumption of the DFN4 is 400mW.

$$V_{IN(MAX)} = 400mW / I_{OUT} + V_{OUT}$$

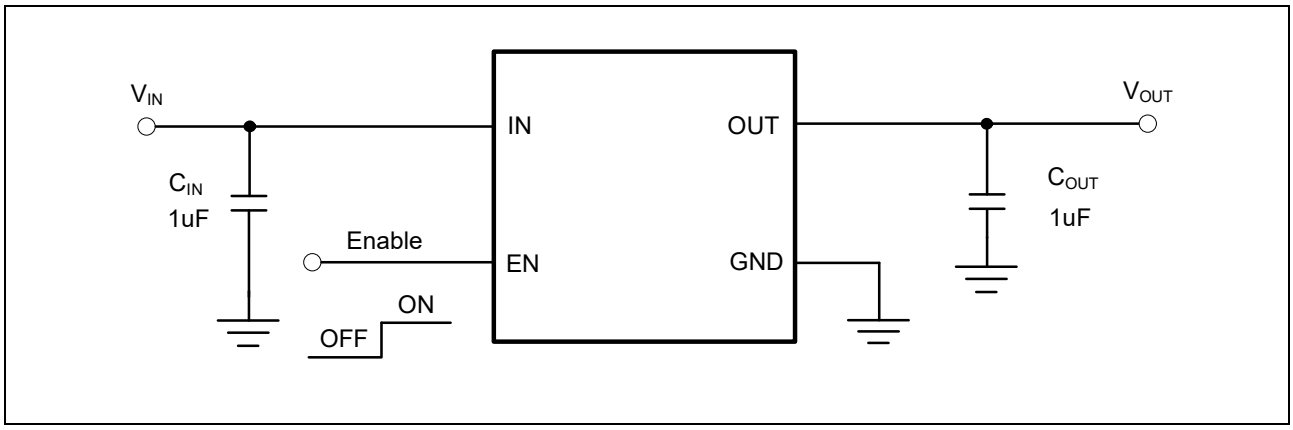
For example:

If $V_{OUT}$ = 1.2V, $I_{OUT}$ = 300mA, the maximum input voltage is $V_{IN(MAX)}$ = 400mW / 300mA + 1.2 = 2.53V

***Note3*:** $V_{DROP}$ FT test method: test the $V_{OUT}$ voltage at $V_{SET}$ + $V_{DROPMAX}$ with output current.

***Note4*:** Guaranteed by design and characterization. Not a FT item.

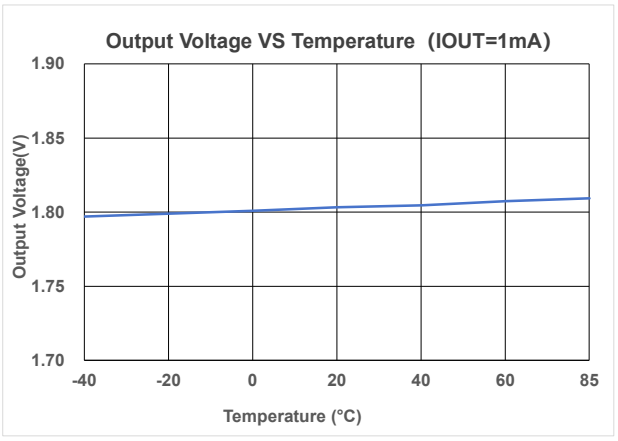
## Application Circuits

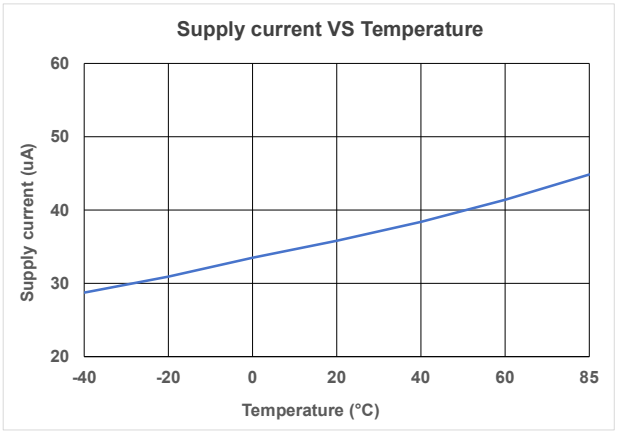


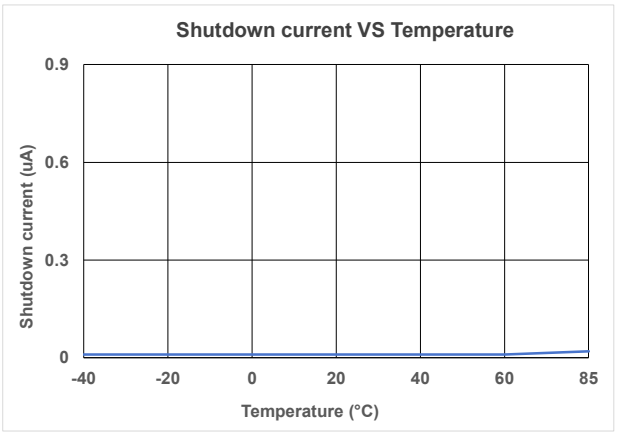
## Typical Characteristics

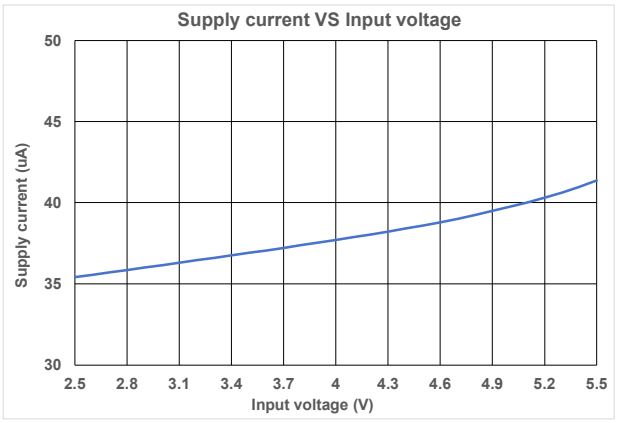
### VOLTAGE VERSION 1.8 V

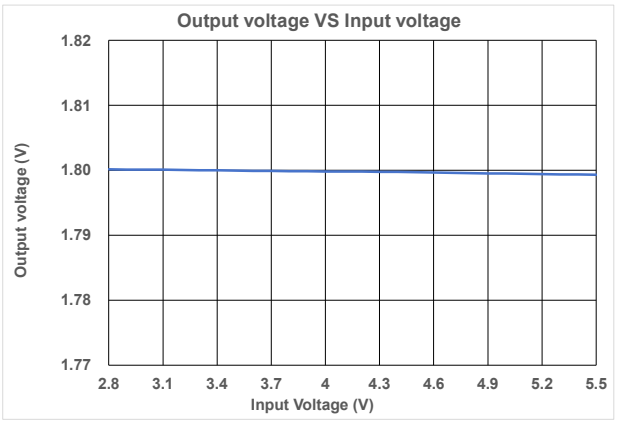
($V_{IN}$ = 2.8V; $I_{OUT}$ = 1mA, $C_{IN}$ = $C_{OUT}$ = 1.0μF, unless otherwise noted. Typical values are at $T_A$ = 25°C.)

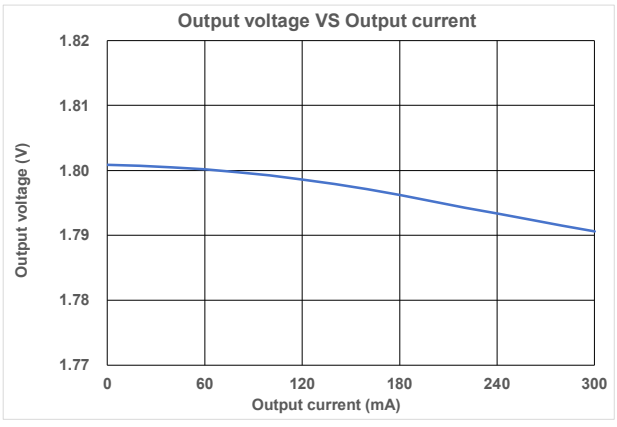


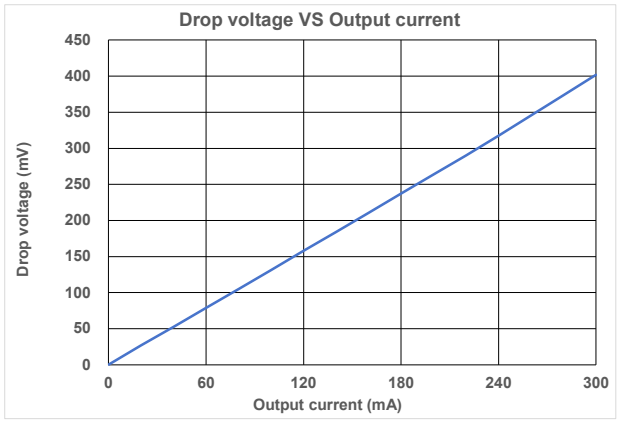



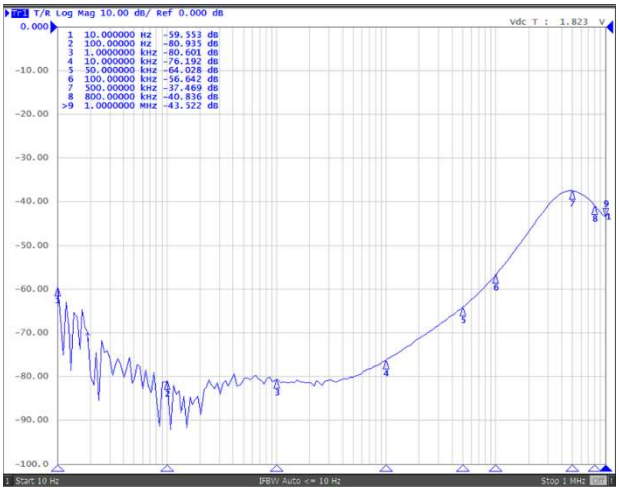



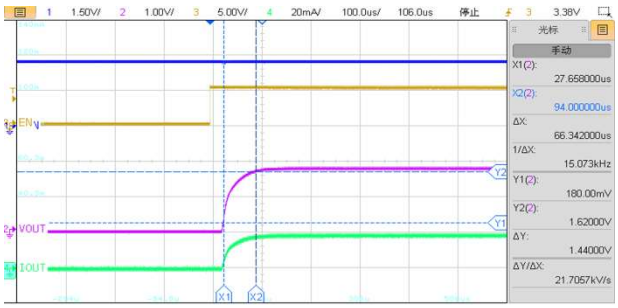



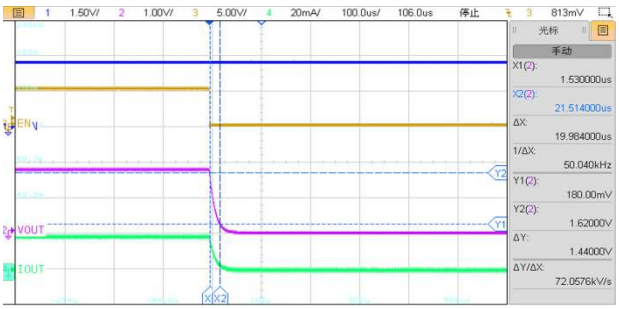


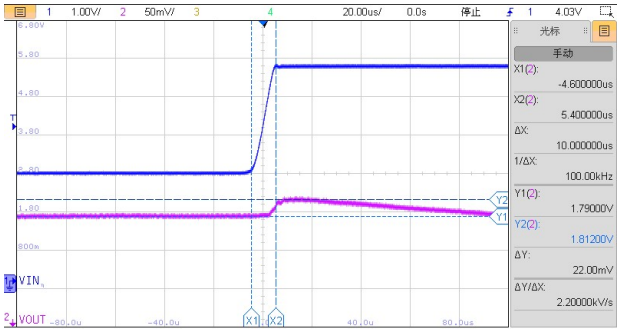
PSRR $V_{IN}$ = 2.8V; $I_{OUT}$ = 20mA



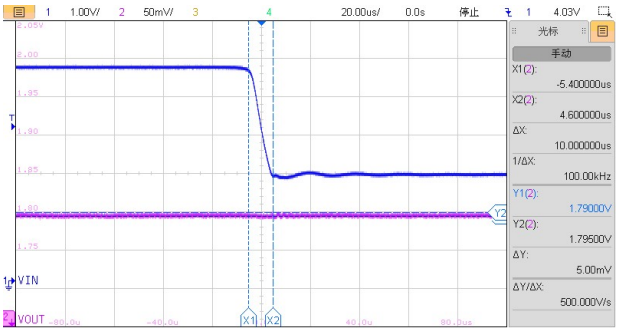
Ton $V_{IN}$ = 2.8V; $I_{OUT}$ = 20mA



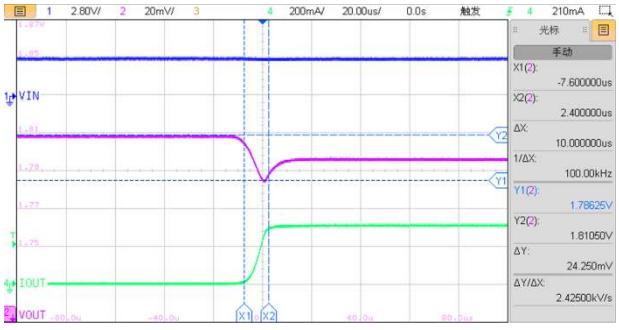
Toff $V_{IN}$ = 2.8V; $I_{OUT}$ = 20mA



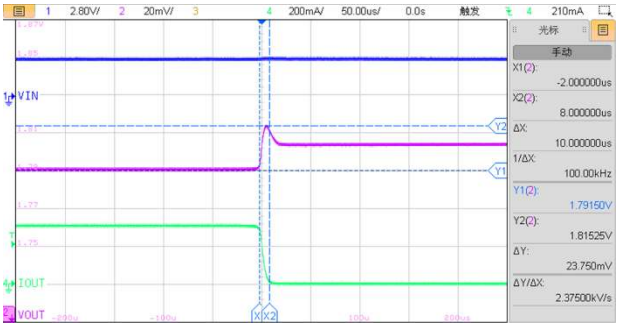
$I_{OUT}$ = 1mA; $V_{IN}$ = 2.8V to 5.5V



$I_{OUT}$ = 1mA; $V_{IN}$ = 5.5V to 2.8V



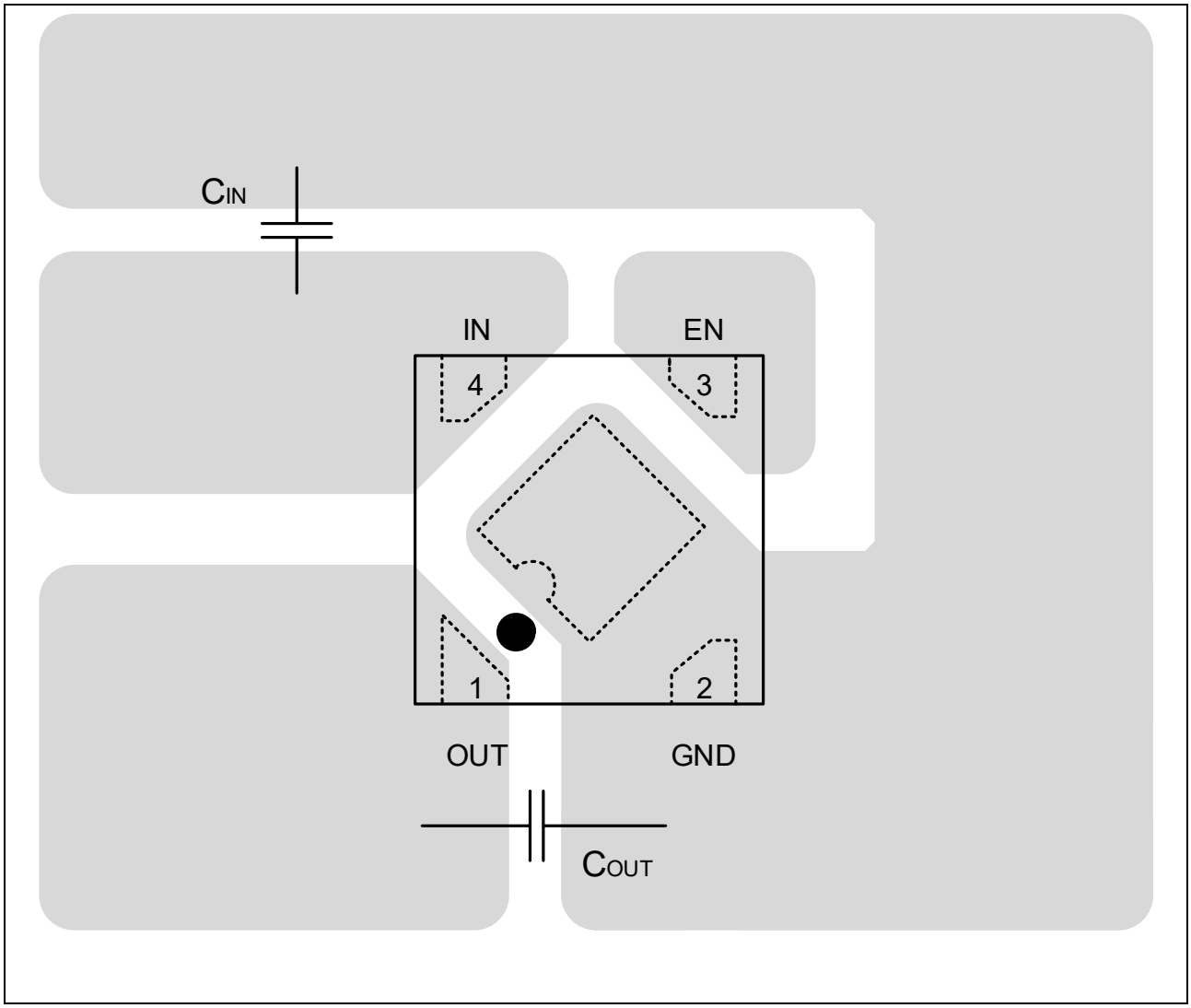
$V_{IN}$ = 2.8V; $I_{OUT}$ = 1mA to 300mA



$V_{IN}$ = 2.8V; $I_{OUT}$ = 300mA to 1mA

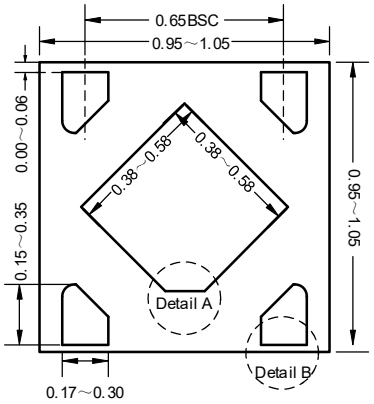
## PCB Layout Guide

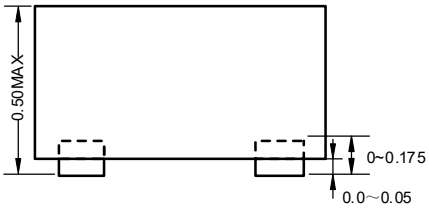
DFN4

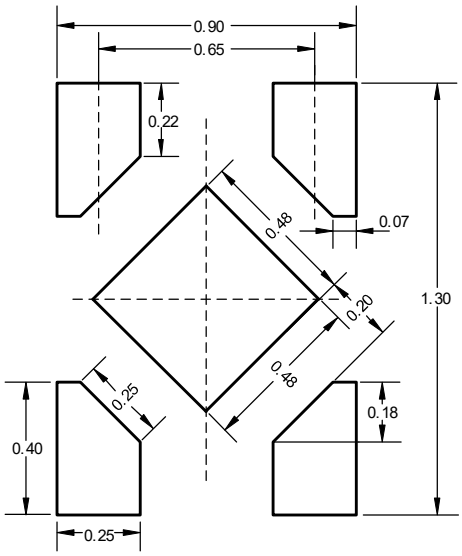


## Package Dimension

DFN4

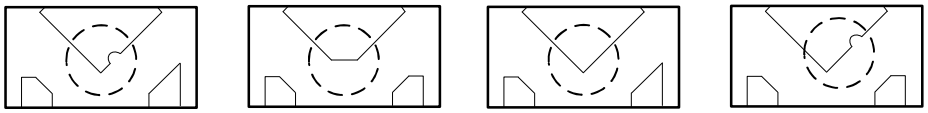



**Recommended Land Pattern**

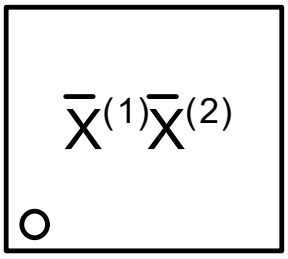
**Detail A&B shape**



Unit: mm

## Marking

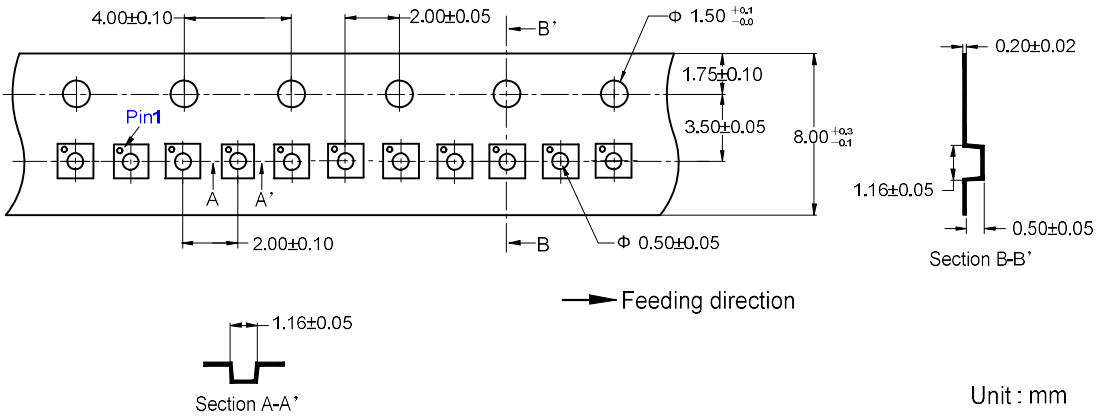
DFN4 Package




$\bar{X}^{(1)}$ = $V_{OUT}$ Version

$\bar{X}^{(2)}$ = Tracking Number

## Tape Information




## Revision History and Checking Table

| Version | Date | Revision Item | Modifier | Function & Spec Checking | Package & Tape Checking |
|---|---|---|---|---|---|
| 0.0 | 2024-06-22 | Original Version | Tugz | Liuxm | Liujy |
| 0.1 | 2024-12-5 | Update EC table | Tugz | Liuxm | Liujy |
| 0.2 | 2025-01-13 | Update EC table and Package | Wangar | Liuxm | Liujy |
| 0.3 | 2025-01-23 | Update EC table | Yangxx | Liuxm | Liujy |
| 1.0 | 2025-02-11 | Official Version | Yangxx | Liuxm | Liujy |
| 1.1 | 2025-03-19 | Add 2.9V Vdrop | Yangxx | Liuxm | Liujy |