

Single Bus Buffer Gate with 3-State Output

General Description

The ET74LVC1G125 is a high performance non-inverting buffer operating from a 1.65V to 5.5V supply. This device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive.

Features

- Designed for 1.65V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- $\pm 32\text{mA}$ Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- 3-State $\overline{OE}$ Input is Active-Low
- ESD Protection Complies with JESD22 Standard
 - HBM: $\pm 4000\text{V}$ Pass (JEDEC JS-001)
 - CDM: $\pm 1000\text{V}$ Pass (JEDEC JS-002)
- Latch-up Performance Exceeds $\pm 100\text{mA}$ per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74LVC1G125	SC70-5 (1.3mm $\times$ 2.1mm)	Tape and Reel, 3K/Reel	1
ET74LVC1G125T	SOT23-5 (1.6mm $\times$ 2.9mm)	Tape and Reel, 3K/Reel	3
ET74LVC1G125Y	DFN6 (1.0mm $\times$ 1.5mm)	Tape and Reel, 3K/Reel	1
ET74LVC1G125Y1	DFN4 (0.8mm $\times$ 0.8mm)	Tape and Reel, 10K/Reel	1

Pin Configuration

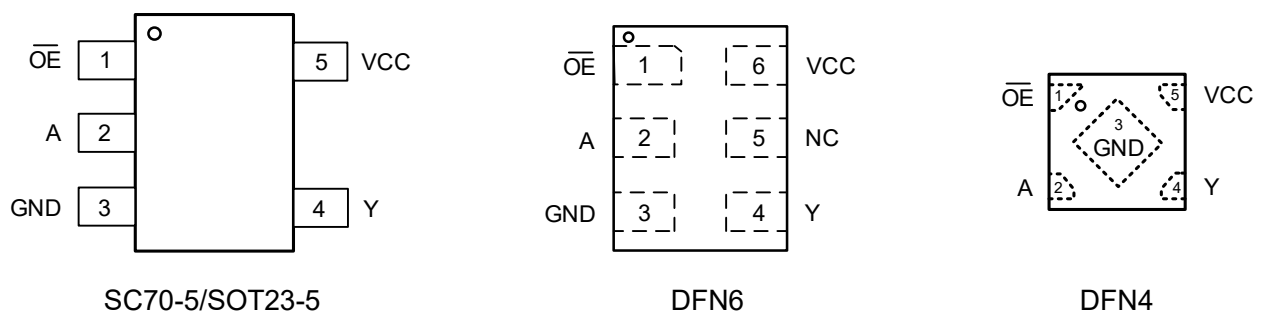


Figure1. Pin Configuration

ET74LVC1G125

Pin Function

SC70-5/ SOT23-5

Pin No.	Pin Name	Function
1	$\overline{\text{OE}}$	Enable Input
2	A	Input
3	GND	Ground
4	Y	Output
5	VCC	Supply Voltage

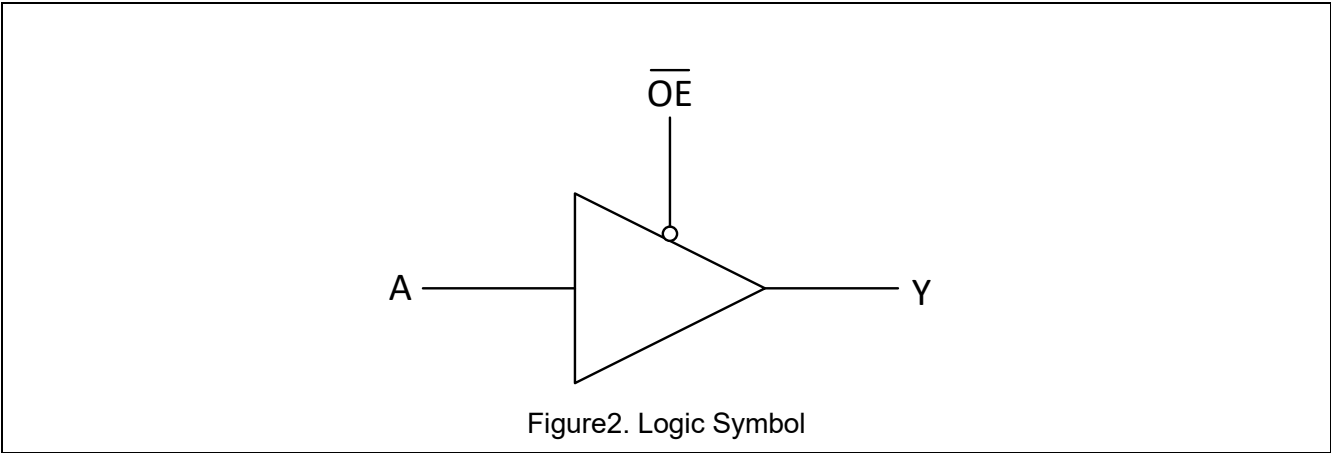
DFN6

Pin No.	Pin Name	Function
1	$\overline{\text{OE}}$	Enable Input
2	A	Input
3	GND	Ground
4	Y	Output
5	NC	No Connect
6	VCC	Supply Voltage

DFN4

Pin No.	Pin Name	Function
1	$\overline{\text{OE}}$	Enable Input
2	A	Input
3	GND	Ground
4	Y	Output
5	VCC	Supply Voltage

Block Diagram



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Function Table

Input		Output
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 6.5	V
V_I	DC Input Voltage ⁽¹⁾		$-0.5 \leq V_I \leq 6.5$	V
V_O	DC Output Voltage Output in Higher or Low State		-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current, $V_I < GND$		-50	mA
I_{OK}	DC Output Diode Current, $V_O < GND$, $V_O > V_{CC}$		± 50	mA
I_O	DC Output Sink Current		± 50	mA
I_{CC}	DC Supply Current Per Supply Pin		± 100	mA
I_{GND}	DC Ground Current Per Supply Pin		± 100	mA
T_{STG}	Storage Temperature Range		-65 to 150	°C
T_L	Lead Temperature, Soldering 10 Seconds		260	°C
T_J	Max Junction Temperature		150	°C
V_{ESD}	ESD Classification	Human Body Model ⁽²⁾	± 4000	V
		Charged Device Model ⁽³⁾	± 1000	
I_{LU}	Max Latch Up Current Above V_{CC} and GND at 125°C ⁽⁴⁾		± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch Up Current Maximum Rating tested per JEDEC JESD78F.

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Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SC70-5	Thermal Characteristics, Thermal Resistance, Junction-to-Air	300	°C/W
	SOT23-5		250	
	DFN6		440	
	DFN4		285	
P_D	SC70-5	Power Dissipation in Still Air at 85°C	215	mW
	SOT23-5		260	
	DFN6		150	
	DFN4		350	

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage Operating		1.65	5.5	V
	Data Retention		1.5	5.5	
V_I	DC Input Voltage		0	V_{CC}	V
V_O	DC Output Voltage (High or Low State)		0	V_{CC}	V
T_A	Operating Temperature Range		-40	125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.5V \pm 0.2V$	0	20	ns/V
		$V_{CC} = 3.0V \pm 0.3V$	0	10	
		$V_{CC} = 5.0V \pm 0.5V$	0	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied.

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Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65~1.95 2.3~5.5	0.75V _{CC} 0.7V _{CC}			0.75V _{CC} 0.7V _{CC}		V
V _{IL}	Low-Level Input Voltage		1.65~1.95 2.3~5.5			0.25V _{CC} 0.3V _{CC}		0.25V _{CC} 0.3V _{CC}	V
V _{OH}	High-Level Output Voltage	I _{OH} = -100uA	1.65~5.5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V
		I _{OH} = -3mA	1.65	1.29	1.52		1.29		
		I _{OH} = -8mA	2.3	1.9	2.1		1.9		
		I _{OH} = -12mA	2.7	2.2	2.4		2.2		
		I _{OH} = -16mA	3.0	2.4	2.7		2.4		
		I _{OH} = -24mA	3.0	2.3	2.5		2.3		
		I _{OH} = -32mA	4.5	3.8	4.0		3.8		
V _{OL}	Low-Level Output Voltage	I _{OH} = 100uA	1.65~5.5		0.0	0.1		0.1	V
		I _{OL} = 3mA	1.65		0.08	0.24		0.24	
		I _{OL} = 8mA	2.3		0.20	0.3		0.3	
		I _{OL} = 12mA	2.7		0.22	0.4		0.4	
		I _{OL} = 16mA	3.0		0.28	0.4		0.4	
		I _{OL} = 24mA	3.0		0.38	0.55		0.55	
		I _{OL} = 32mA	4.5		0.42	0.55		0.55	
I _{IN}	Input Leakage Current	V _I = 5.5V or GND	0~5.5			±0.1		±1.0	uA
I _{OFF}	Power Off Leakage Current	V _I = 5.5V or V _O = 5.5V	0			1		10	uA
I _{CC}	Quiescent Supply Current	V _I = 5.5V or GND	5.5			1		10	uA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC Electrical Characteristics

$t_r = t_f = 3\text{ns}$

Symbol	Parameter	Condition	$V_{CC}(V)$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PD}	Propagation Delay (Figure3 and 4)	$R_L = 1\text{M}\Omega$ $C_L = 15\text{pF}$	1.65	2.0	12	16	2.0	20	ns
			1.8	2.0	10.1	14	2.0	17	
			2.5	0.2	6.2	9.1	0.8	11.1	
		$R_L = 1\text{M}\Omega$ $C_L = 15\text{pF}$ $R_L = 500\Omega$ $C_L = 50\text{pF}$	3.3	0.8	5.0	7.5	0.5	8	
				1.2	5.6	8.1	1.5	8.6	
		$R_L = 1\text{M}\Omega$ $C_L = 15\text{pF}$ $R_L = 500\Omega$ $C_L = 50\text{pF}$	5.0	0.5	4.4	5.6	0.5	6.1	
				0.8	4.8	6.1	0.8	6.6	
$t_{PZL},$ t_{PZH}	Output Enable Time (Figure5 and 6)	$R_L = 500\Omega$ $C_L = 50\text{pF}$	1.65	2.0	15	20.0	2.0	23.0	ns
			1.8	2.0	12.4	18.0	2.0	22.0	
			2.5	1.5	7.2	8.8	1.5	9.4	
			3.3	1.5	5.8	7.1	1.5	7.6	
			5.0	0.8	4.5	5.5	0.8	5.9	
$t_{PLZ},$ t_{PHZ}	Output Disable Time (Figure5 and 6)	$R_L = 500\Omega$ $C_L = 50\text{pF}$	1.65	2.0	11.5	20.0	2.0	23.0	ns
			1.8	2.0	9.8	18.0	2.0	22.0	
			2.5	1.5	7.7	9.5	1.5	10.1	
			3.3	1.0	7.2	8.8	1.0	9.4	
			5.0	0.5	5.4	6.8	0.5	7.3	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5\text{V}, V_I = 0\text{V}$ or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance ⁽⁵⁾	10MHz, $V_{CC} = 3.3\text{V}, V_I = 0\text{V}$ or V_{CC}	15	pF
		10MHz, $V_{CC} = 5.5\text{V}, V_I = 0\text{V}$ or V_{CC}	15	

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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AC Test Circuit

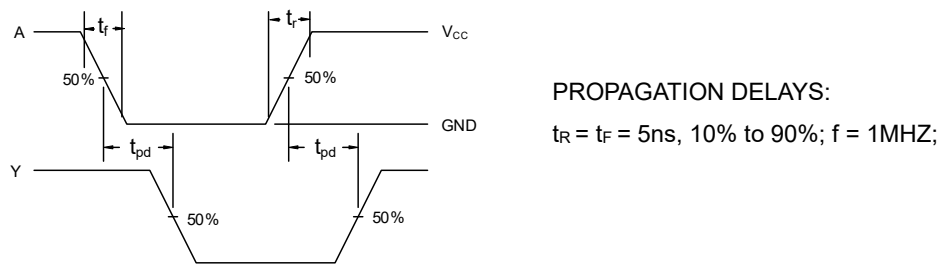


Figure3. Switch Waveform

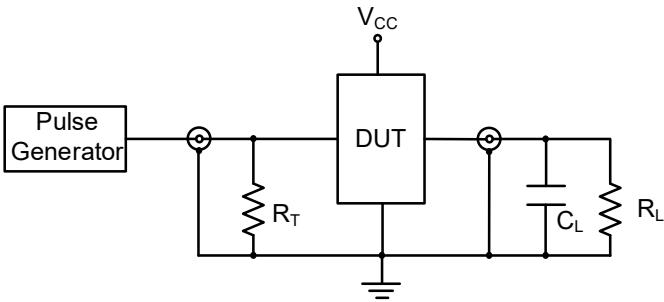


Figure4. Test Circuit $R_T = 50\Omega(\text{typ})$

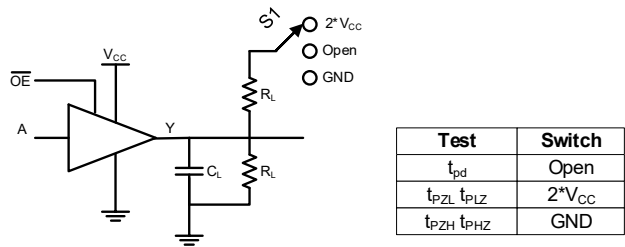


Figure5. Output Enable/Disable Time Test Circuit

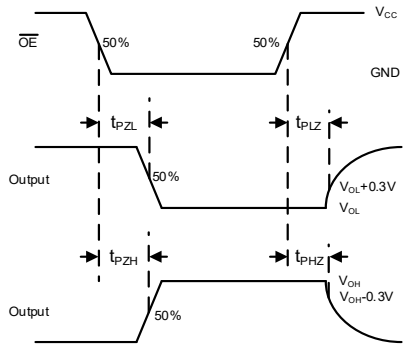


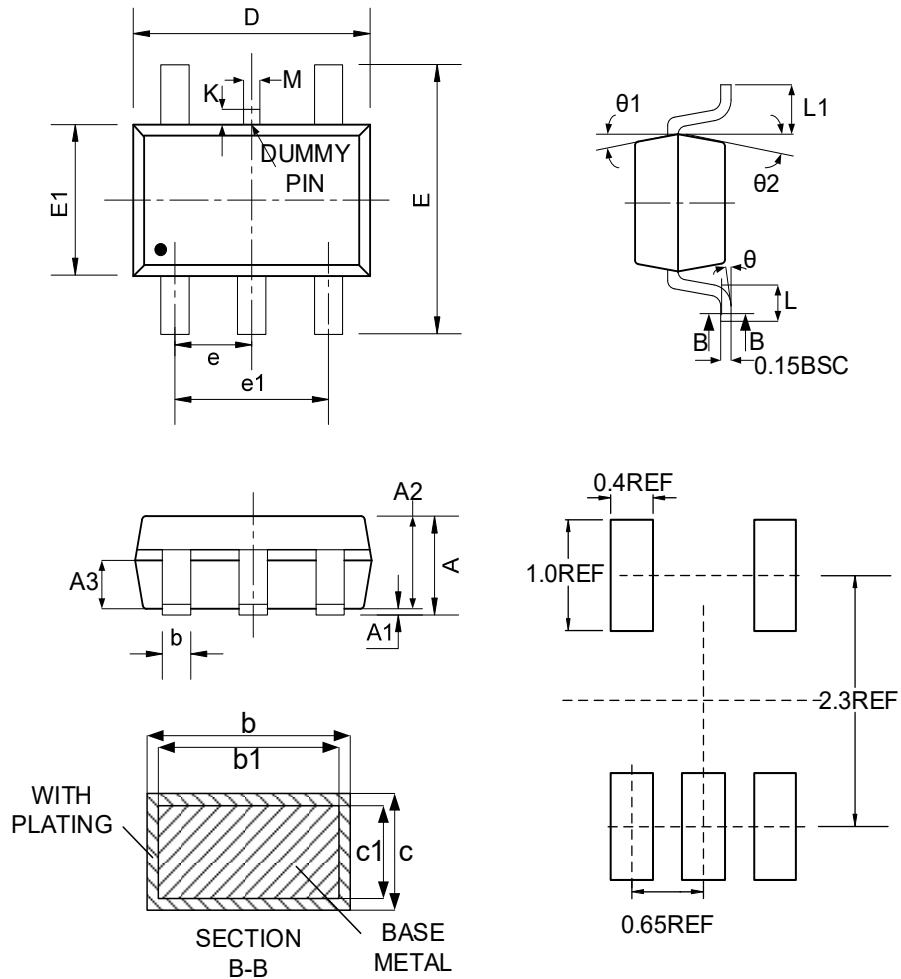
Figure6. Output Enable/Disable Waveform

Note6: This electric circuit only supplies for reference. It is recommended to ground the unused I/O ports and ensure they are **not left floating**.

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Package Dimension

SC70-5 (1.3mm × 2.1mm)



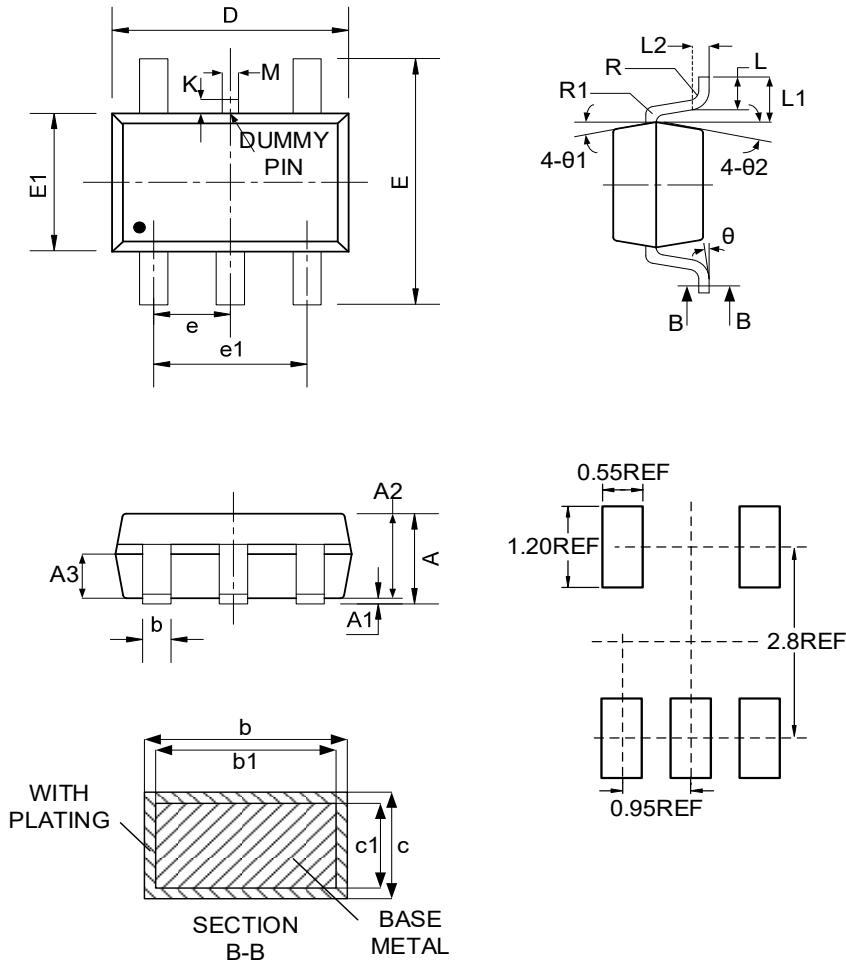
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	0.80	-	1.10	e	0.60	0.65	0.70
A1	0.00	-	0.10	e1	1.20	1.30	1.40
A2	0.80	0.90	1.00	L	0.26	0.33	0.46
A3	0.40	0.50	0.60	E1	1.21	1.26	1.31
b	0.17	-	0.30	L1	0.52REF		
b1	0.17	0.22	0.25	M	0.10	0.15	0.20
c	0.12	-	0.20	K	0.00	-	0.20
c1	0.12	0.15	0.16	θ	0°	-	8°
D	2.02	2.07	2.12	θ1	10°	12°	14°
E	2.20	2.30	2.40	θ2	10°	12°	14°

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SOT23-5 (1.6mm × 2.9mm)



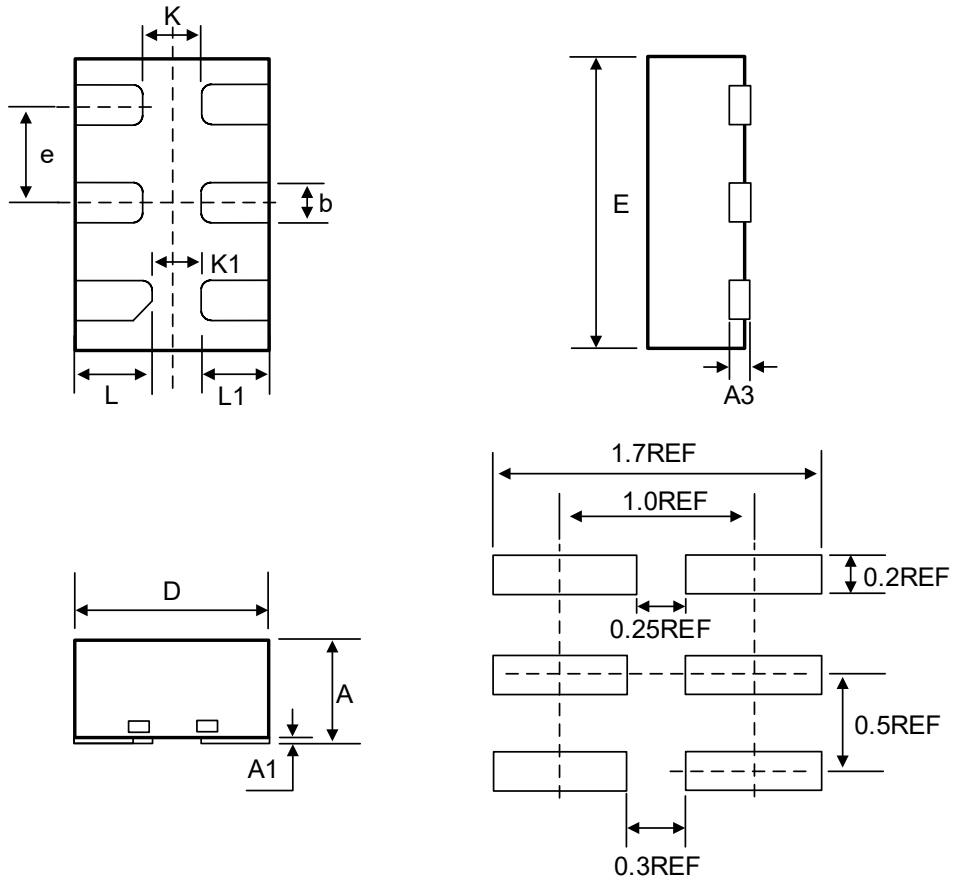
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	-	-	1.25	K	0	-	0.20
A1	0.00	-	0.15	M	0.10	0.15	0.20
A2	1.00	1.10	1.20	L	0.30	0.40	0.60
A3	0.60	0.65	0.70	L1	0.59REF		
b	0.34	-	0.45	L2	0.25BSC		
b1	0.34	0.38	0.41	R	0.05	-	0.20
c	0.12	-	0.20	R1	0.05	-	0.20
c1	0.12	0.15	0.16	θ	0°	-	8°
D	2.826	2.926	3.026	θ1	8°	10°	12°
E	2.60	2.80	3.00	θ2	10°	12°	14°
E1	1.526	1.626	1.70				
e	0.90	0.95	1.00				
e1	1.80	1.90	2.00				

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DFN6 (1.0mm × 1.5mm)



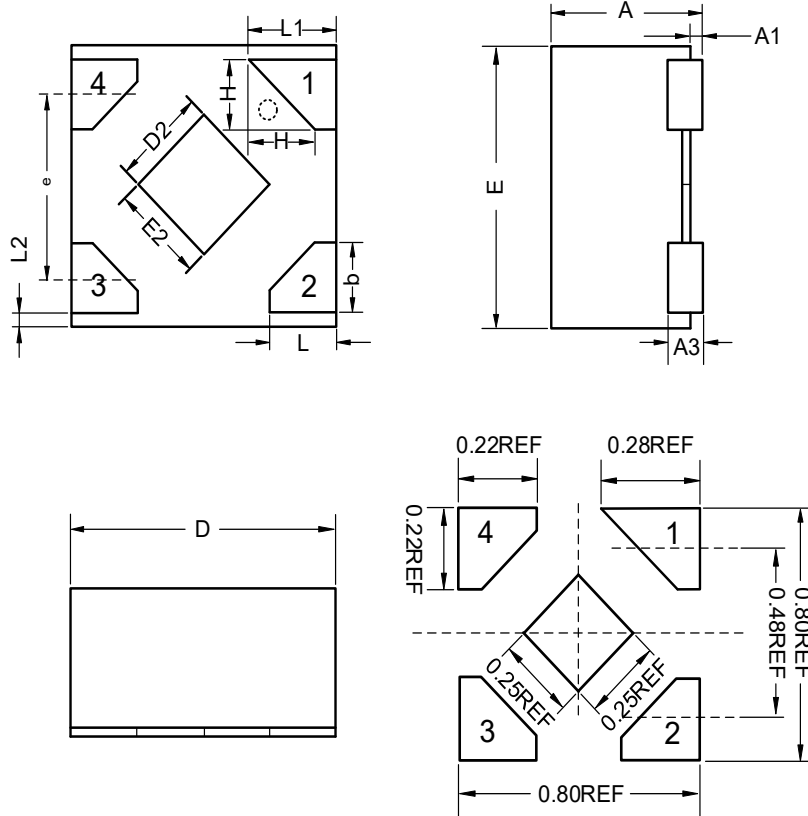
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	0.50	--	0.60
A1	0.00	0.02	0.05
A3	0.10REF		
b	0.15	0.20	0.25
D	0.90	1.00	1.10
E	1.40	1.50	1.60
e	0.50BSC		
K	0.30REF		
K1	0.25REF		
L	0.35	0.40	0.45
L1	0.30	0.35	0.40

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DFN4 (0.8mm × 0.8mm)



COMMON DIMENSIONS

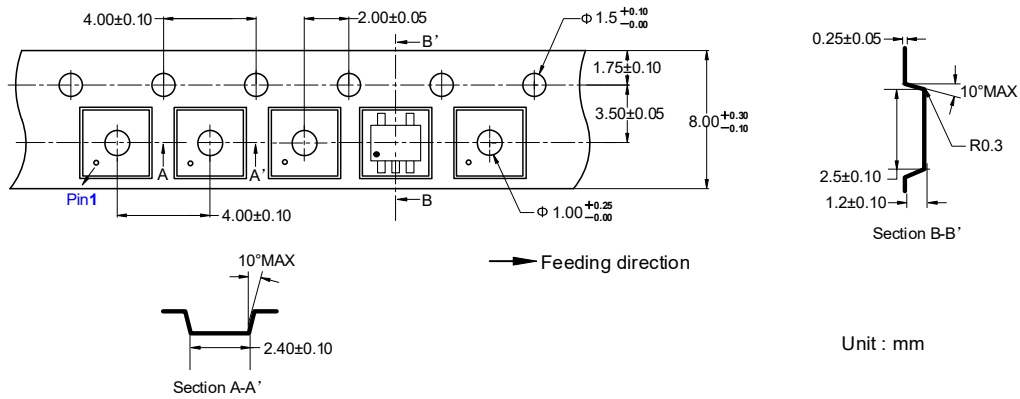
(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	0.34	0.37	0.40
A1	0.00	0.02	0.05
A3	0.10REF		
b	0.17	0.22	0.27
D	0.75	0.80	0.85
E	0.75	0.80	0.85
D2	0.20	0.25	0.30
E2	0.20	0.25	0.30
e	0.43	0.48	0.53
H	0.22REF		
L	0.17	0.22	0.27
L1	0.18	0.28	0.38
L2	0.05REF		

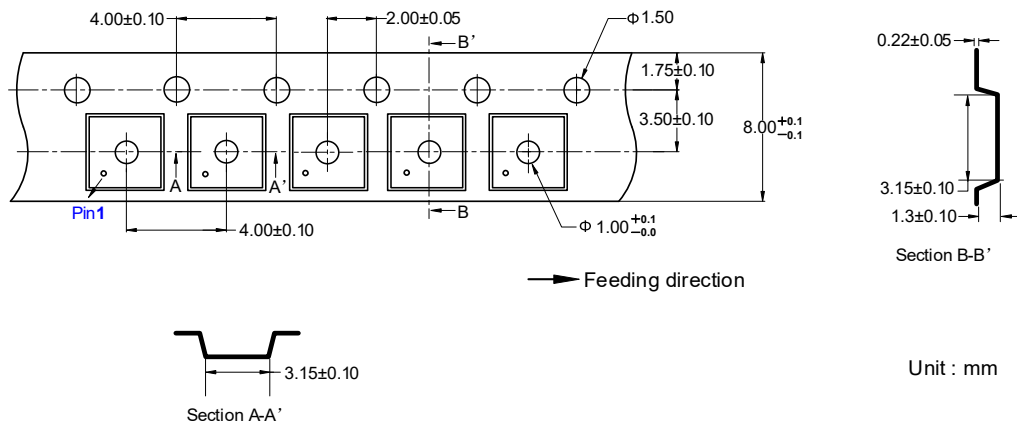
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Tape Information

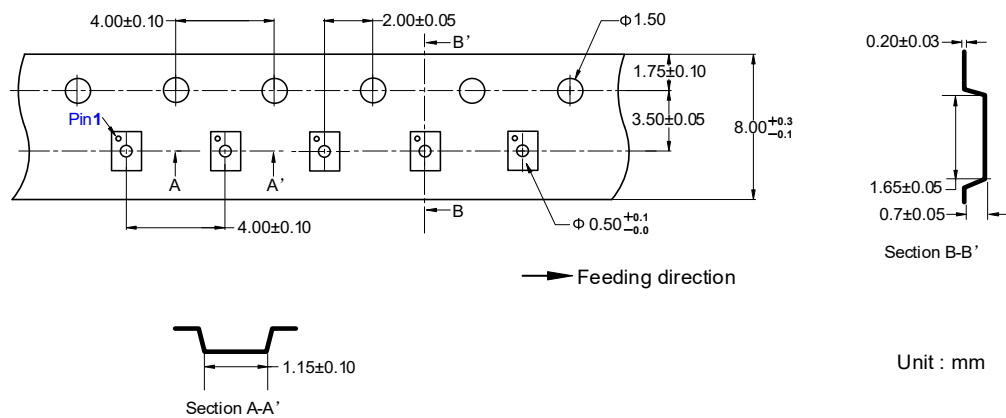
SC70-5 (1.3mm × 2.1mm)



SOT23-5 (1.6mm × 2.9mm)



DFN6 (1.0mm × 1.5mm)



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Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2017-10-23	Original Version	Ma Yong Jian	Ma Yong Jian	Liu Jiaying
1.1	2019-07-18	Update AC Table and Device Information	Ma Yong Jian	Ma Yong Jian	Liu Jiaying
1.2	2019-08-22	Add Output Enable/Disable Time & Test Circuit	Ma Yong Jian	Ma Yong Jian	Liu Jiaying
1.3	2022-06-10	ESD Update	Shi Bo	Shi Bo	Liu Jiaying
1.4	2023-11-29	Update Typeset /ESD/ Package Picture	Shi Bo	Shi Bo	Liu Jiaying
1.5	2024-1-12	Add Marking	Wang Peng	Wang Peng	Liu Jiaying
1.6	2024-4-07	Add Tape	Tu Guo Zhu	Lu Hao	Liu Jiaying
1.7	2025-06-03	Add Packing Option	Yang Xiao Xu	Yang Xiao Xu	Liu Jiaying
1.8	2025-07-25	Update AC Electrical Characteristics	Ma Ruijie	Yang Xiao Xu	Liu Jiaying
1.9	2025-10-31	Update Format	Wang Qi fan	Yang Xiao xu	Liu Jiaying
1.10	2026-03-19	Add DFN4 Package	Yang Xiao xu	Yang Xiao xu	Liu Jiaying
1.11	2026-7-31	Update Package	Lu Shao jie	Yang Xiao xu	Liu Jiaying