Single SPDT Analog Switch

General Description

The ET3157 is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very low propagation delay and RDSON resistances while maintaining CMOS low power dissipation. Analog and digital voltages that may vary across the full power-supply range (from VCC to GND).

The Select pin has over voltage protection that allows voltages above VCC, up to 6.0 V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage.

ET3157 offered in a small SC70-6、SC88、SOT23-6 or DFN6 package, which is ideal for small form factor portable equipment.

Features

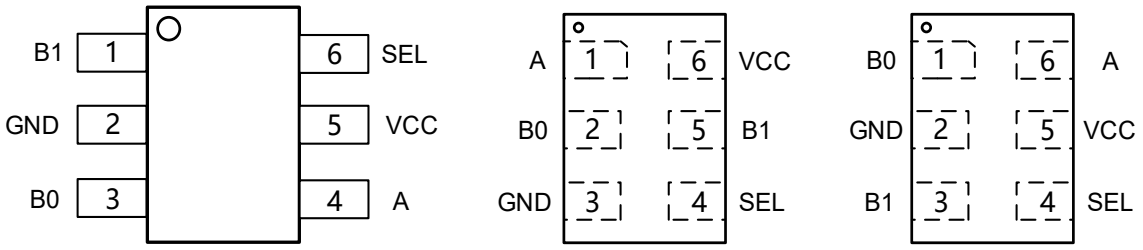
- VCC Operating Range from 1.8 V to 5.5 V
- High speed and low delay
- Low power dissipation
- Standard CMOS logic levels
- High bandwidth up to 250MHz, improved linearity
- Low R_{DSON} is 3.0Ω @ V_{CC} =4.5V
- Break before make Circuitry, Prevents inadvertent shorts
- Operating temperature for -40°C～+85°C
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET3157	SC70-6 (2.3mm ×2.1mm)	Tape and Reel, 3K/Reel	Level 3
ET3157SC	SC-88 (2.1mm ×2.0mm)	Tape and Reel, 3K/Reel	Level 3
ET3157T	SOT23-6 (2.926mm ×2.8mm)	Tape and Reel, 3K/Reel	Level 3
ET3157Y	DFN6 (1.45mm ×1.0mm)	Tape and Reel, 3K/Reel	Level 1
ET3157Y1	DFN6 (1.1mm ×0.9mm)	Tape and Reel, 3K/Reel	Level 1
ET3157Y2	DFN6 (1.1mm ×0.9mm)	Tape and Reel, 3K/Reel	Level 1

Applications

- NTSC/PAL Video
- Audio Signal Routing
- SPDIF and HDTV

Pin Configuration



SC70-6/SC-88/SOT23-6 DFN6(ET3157Y/ET3157Y1) DFN6(ET3157Y2)

Top View

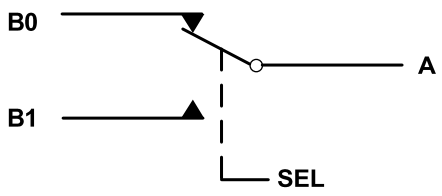
Pin Function

Pin Number	I/O	Pin Function
A，B0，B1	I/O	Data port
SEL	I	Controlling choice
VCC	—	Power supply port
GND	—	Ground

Functions Description

SEL port Level	Function
L	B0 Connected to A
H	B1 Connected to A

Analog Symbol



Analog Symbol

Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5～+6.0	V
DC Switch Voltage (1)	V_{IN}	-0.5～V_{CC}+0.5	V
DC Input Voltage (1)	V_S	-0.5～+6.0	V
DC Input Diode Current @V_{IN}<0V	I_{IK}	-50	mA
DC Output Current	I_{OUT}	128	mA
DC V_{CC} or Ground Current	I_{CC} / I_{GND}	100	mA
Storage Temperature Range	T_{STG}	-65～+150	°C
Junction Temperature Under Bias	T_J	150	°C
Junction Lead Temperature (Soldering 10 Seconds)	T_{SOLD}	260	°C
HBM Max Capability (EIA/JESD22-A114)	V_{ESD}	± 4000	V
CDM Max Capability (JESD22-C101)		± 1000	V
Latch up Current Maximum Rating (JEDEC78)	I_{LU}	± 200	mA
Power Dissipation @ +85°C (SC70-6/SC-88)	P_D	180	mW
Power Dissipation @ +85°C (DFN6)		250	

Maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The data sheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. ETEK does not recommend operation outside data sheet specifications.

Note1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Supply Voltage Operating	V_{CC}	1.8	5.5	V
SEL Input Voltage(2)	V_S	0	V_{CC}	V
Switch Input Voltage	V_{IN}	0	V_{CC}	V
Output Voltage	V_{OUT}	0	V_{CC}	V
Operating Temperature	T_A	-40	+85	°C
Input Rise and Fall Time Control Input V_{CC}=2.3V~3.6V Control Input V_{CC}=4.5V~5.5V	tr / tf	 0 0	 10 5.0	ns/V

Note2. SEL input must be held HIGH or LOW, it must not float.

Electrical Characteristics

Symbol	Parameter	Test Conditions	V_{CC}	T_A=25°C			T_A=-40~+85°C		Unit
				Min	Typ	Max	Min	Max	
DC ELECTRICAL CHARACTERISTICS									
V_{IH}	HIGH Level Input Voltage		1.8~2.9	1.4			1.5		V
			3~4.2	2.3			2.4		
			4.3~5.5	3.2			3.3		
V_{IL}	LOW Level Input Voltage		1.8~2.9			0.4		0.35	V
			3~4.2			0.4		0.35	
			4.3~5.5			0.6		0.55	
I_S	SEL Input Leakage Current	0< V_S<5.5V	0~5.5			±0.1		±1	uA
I_{OFF}	OFF State Leakage Current	0< A,B<V_{CC}	1.8~5.5			±0.1		±1	uA
I_{CC}	Quiescent Supply	V_S=V_{CC} or GND I_{OUT}=0	5.5			1.0		10	uA
V_{AS}	Analog Signal Range		V_{CC}	0		V_{CC}	0	V_{CC}	V
R_{ON}	Switch On Resistance (3)	V_{IN}=0V, I_O=30mA	4.5		3	6		9	Ω
		V_{IN}=2.4V, I_O=-30mA			3.5	7		12	Ω
		V_{IN}=4.5V, I_O=-30mA			5	10		15	Ω
		V_{IN}=0V, I_O=24mA	3.0		3.5	7		12	Ω
		V_{IN}=3V, I_O=-24mA			7	12		18	Ω
		V_{IN}=0V, I_O=8mA	2.3		4	8		13	Ω
		V_{IN}=2.3V, I_O=-8mA			9	15		25	Ω
		V_{IN}=0V, I_O=4mA	1.8		5	10		15	Ω
		V_{IN}=1.8V, I_O=-4mA			15	25		35	Ω
R_{RANGE}	On Resistance Over Signal Range (3)(7)	I_A=-30mA 0≤V_{Bn}≤V_{CC}	4.5		6	10		25	Ω
		I_A=-24mA 0≤V_{Bn}≤V_{CC}	3		12	20		35	Ω
		I_A=-8mA 0≤V_{Bn}≤V_{CC}	2.3		45	85		120	Ω
		I_A=-4mA 0≤V_{Bn}≤V_{CC}	1.8		130	200		300	Ω

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	V_{CC}	T_A=25°C			T_A=-40~+85°C		Unit
				Min	Typ	Max	Min	Max	
ΔR_{ON}	On Resistance Match Between Channels (3)(4)(5)	I_A=-30mA, V_{Bn}=3.1V	4.5		0.15	0.3			Ω
		I_A=-24mA, V_{Bn}= 2.1V	3		0.2	0.4			Ω
		I_A=-8mA, V_{Bn}= 1.6V	2.3		0.5	1			Ω
		I_A=-4mA, V_{Bn}= 1.15V	1.8		0.5	1			Ω
R_{FLAT}	On Resistance Flatness (3)(4)(6)	I_A=-30mA $0 \le V_{Bn} \le V_{CC}$	4.5		4	8			Ω
		I_A=-24mA $0 \le V_{Bn} \le V_{CC}$	3		10	20			Ω
		I_A=-8mA $0 \le V_{Bn} \le V_{CC}$	2.3		35	65			Ω
		I_A=-4mA $0 \le V_{Bn} \le V_{CC}$	1.8		125	200			Ω
AC ELECTRICAL CHARACTERISTICS									
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus (8)	Figure 1 S1=OPEN	1.8~2.9		2				ns
			3~4.2		1.5				ns
			4.3~5.5		1				ns
t_{PZL} t_{PZH}	Output Enable Time, Turn On Time (7)	Figure 1 S1=2*V_{CC} for t_{PZL}; S1=0V for t_{PZH}	1.8~2.9		20				ns
			3~4.2		10				ns
			4.3~5.5		8				ns
t_{PLZ} t_{PHZ}	Output Disable Time, Turn Off Time (7)	Figure 1 S1=2*V_{CC} for t_{PLZ} ; S1=0V for t_{PHZ}	1.8~2.9		12				ns
			3~4.2		8				ns
			4.3~5.5		6				ns
t_{BBM}	Break Before Make Time (7)	Figure 2; C_L=50pF; R_L=600Ω	1.8~2.9		3				ns
			3~4.2		0.5				ns
			4.3~5.5		0.5				ns
Q	Charge Injection (7)	Figure3, C_L=0.1nF, R_L=1MΩ	5.0		7.0				pC
			3.3		3.0				pC
O_{IRR}	Off Isolation (7) (9)	Figure 4, R_L=50Ω, f= 10MHz	1.8~5.5		-57				dB

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	V_{CC}	T_A=25°C			T_A=-40~+85°C		Unit
				Min	Typ	Max	Min	Max	
X_{TALK}	Crosstalk (7)	Figure 5, R_L=50Ω, f= 10MHz	1.8~5.5		-54				dB
BW	−3dB Bandwidth (7)	Figure 8, R_L=50Ω	1.8~5.5		250				MHz
THD	Total Harmonic Distortion (7)	R_L=600Ω,0.5V_{PP} f=600Hz~20k Hz	5.0		0.011				%
C_{IN}	Select Pin Input Capacitance (10)		0		4.5				pF
C_{IO_B}	B Port Off Capacitance (10)	Figure 6	5.0		7.0				pF
C_{IOA_ON}	A Port Capacitance when Switch is Enabled (10)	Figure 7	5.0		21.0				pF

Note3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

Note4. Parameter is characterized but not tested in production.

Note5. $\Delta R_{ON} = R_{ON}\_max - R_{ON}\_min$ measured at identical V_{CC}, temperature and voltage levels.

Note6. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

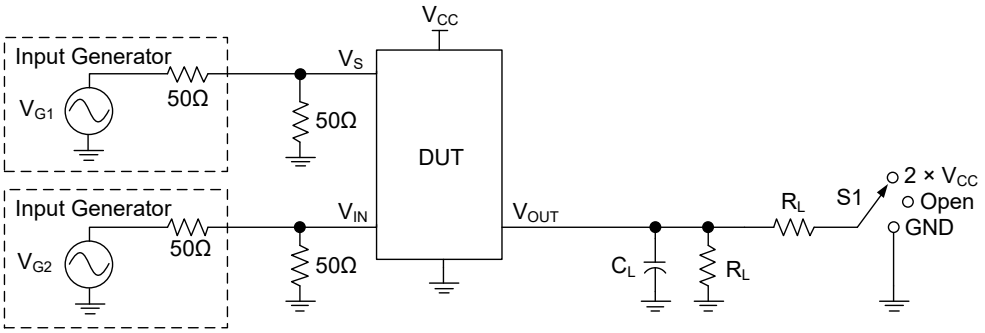
Note7. Guaranteed by Design.

Note8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

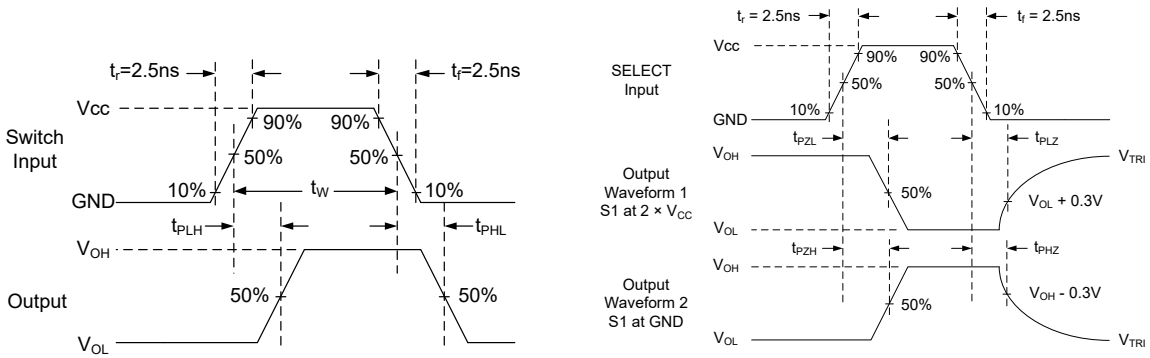
Note9. Off Isolation = 20 log10 [V_A/V_{Bn}].

Note10. T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

Test Reference Circuit



Test	V_{CC}	S1	R_L	V_{IN}	C_L
t_{PLZ}/t_{PZL}	1.8~5.5V	2*V_{CC}	600Ω	GND	50pF
t_{PHZ}/t_{PZH}	1.8~5.5V	GND		V_{CC}	50pF



NOTE : Input driven by 50 Ω source terminated in 50 Ω

NOTE : CL includes load and stray capacitance

Figure 1. AC Test Circuit , AC Waveforms

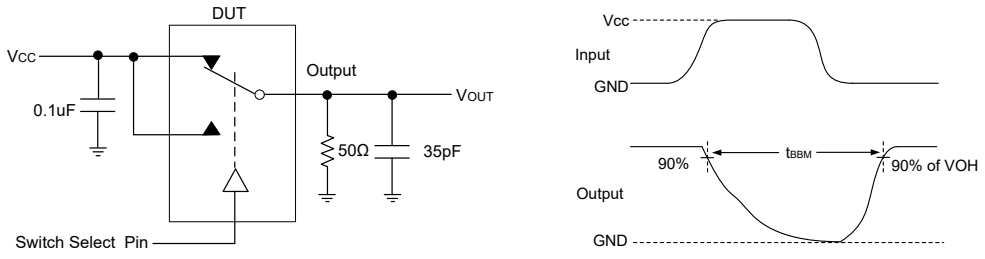


Figure 2. t_{BBM} (Time Break-Before-Make)

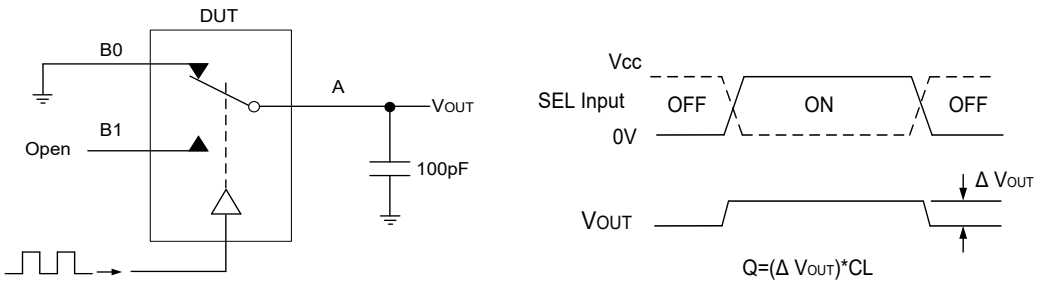


Figure 3. Charge Injection Test

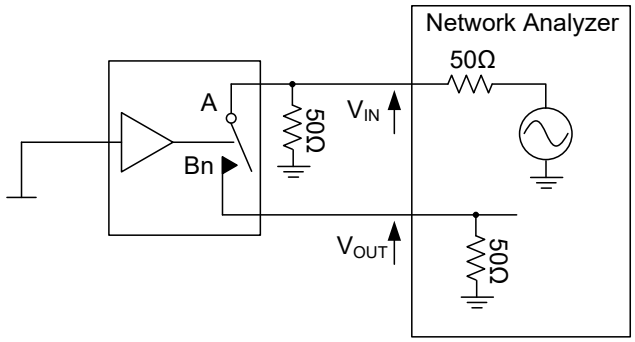


Figure 4. Off Isolation

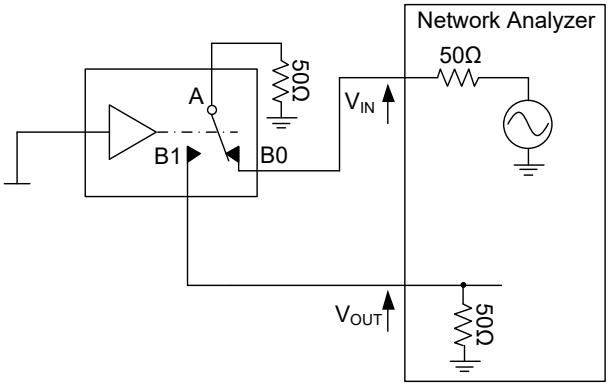


Figure 5.Crosstalk

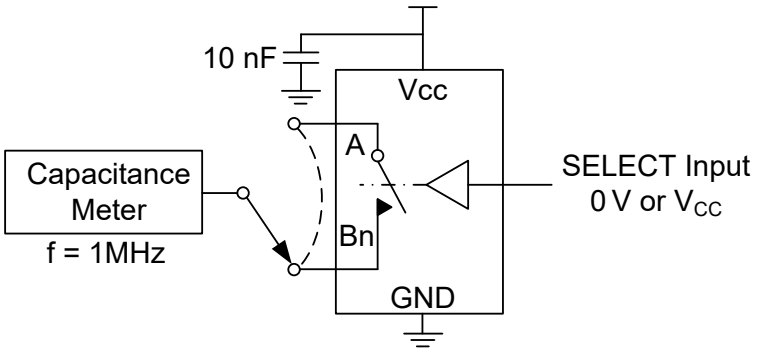


Figure 6. Channel Off Capacitance

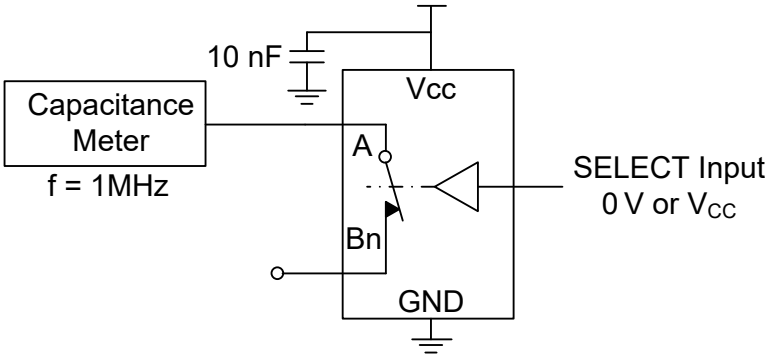


Figure 7. Channel On Capacitance

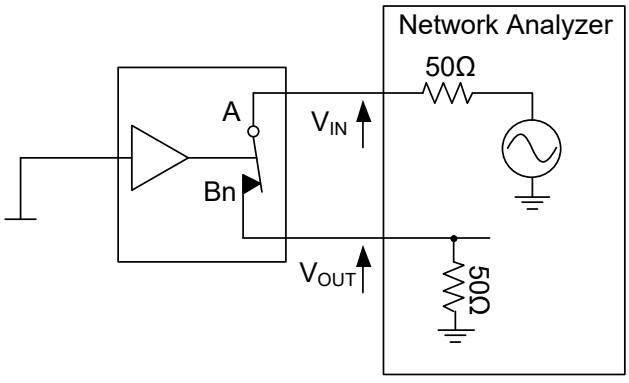
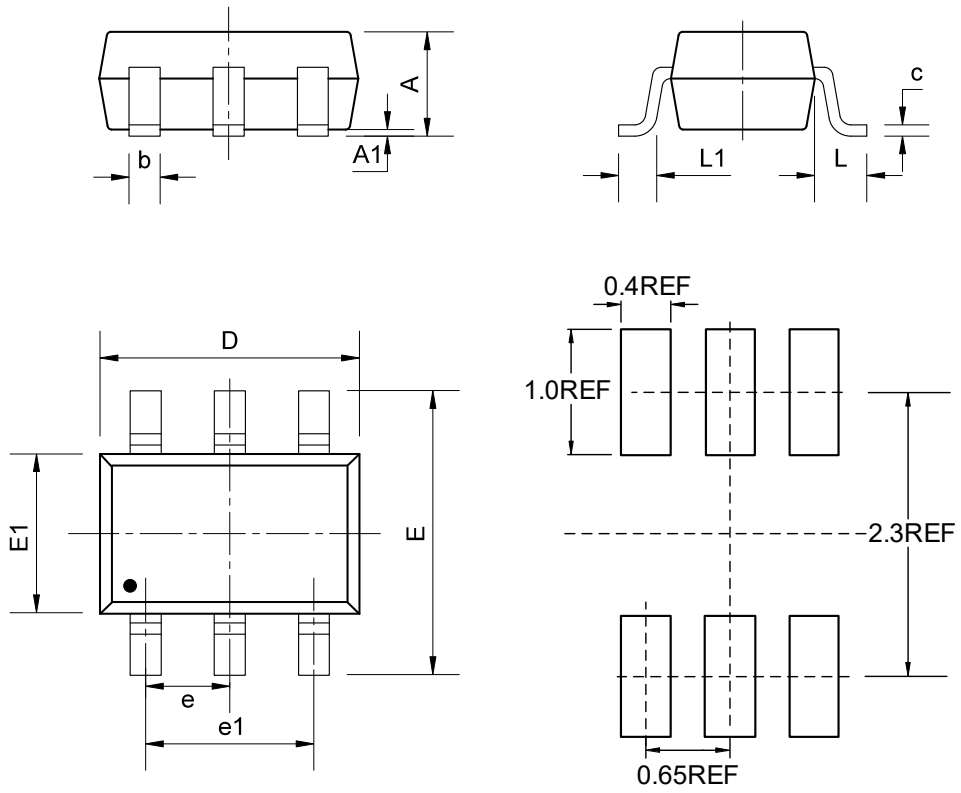


Figure 8. Bandwidth

Package Dimension

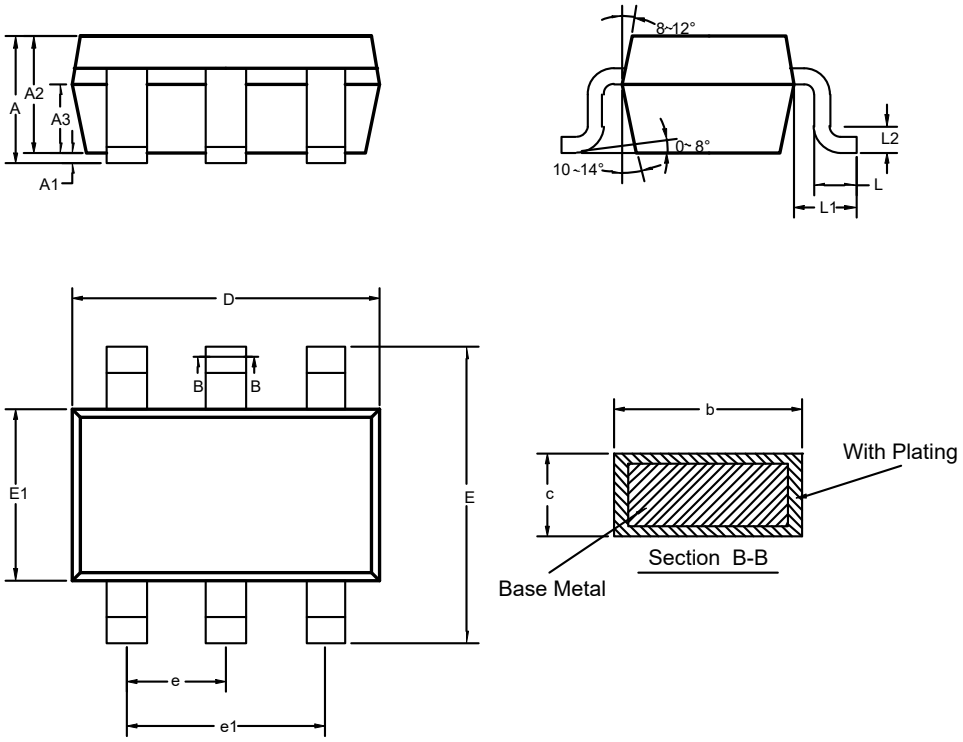
SC70-6



COMMON DIMENSIONS(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	0.80	-	1.10
A1	0.00	-	0.10
b	0.15	-	0.35
c	0.15BSC		
D	2.00	-	2.20
e	0.65BSC		
e1	1.30BSC		
E	2.20	2.30	2.40
E1	1.25	-	1.35
L	0.50REF		
L1	0.33REF		

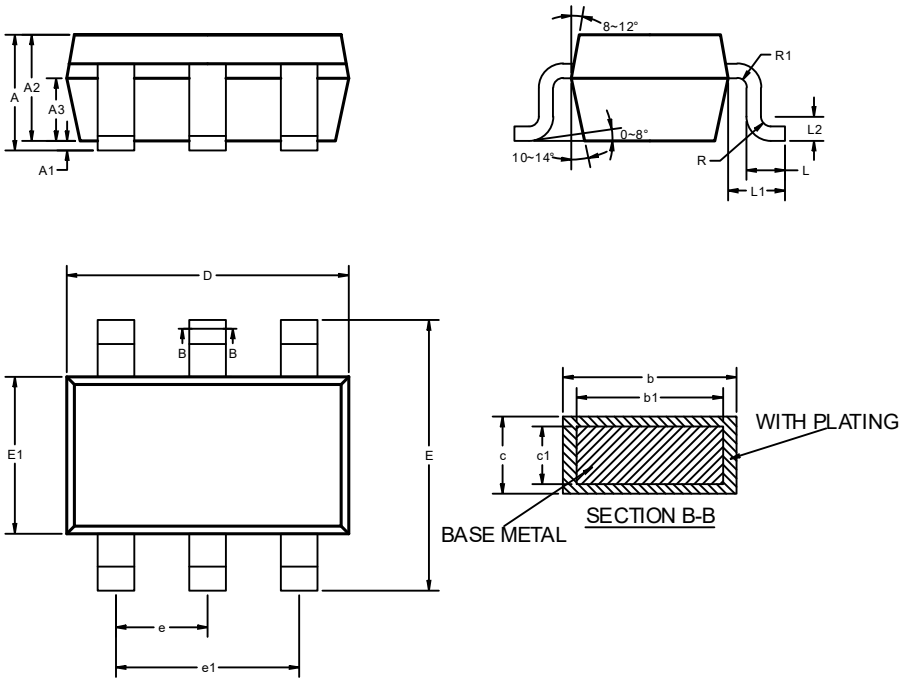
SC-88



Dimensions Table (Units:mm)

SYMBOL	MIN	NOM	MAX
A	0.80	-	1.10
A1	0	-	0.10
A2	0.80	0.90	1.00
A3	0.47	0.52	0.57
b	0.15	-	0.30
c	0.08	-	0.22
D	1.85	2.00	2.15
E	1.95	2.10	2.20
E1	1.10	1.25	1.40
e	0.65BSC		
e1	1.30BSC		
L	0.26	0.36	0.46
L1	0.42REF		
L2	0.15BSC		

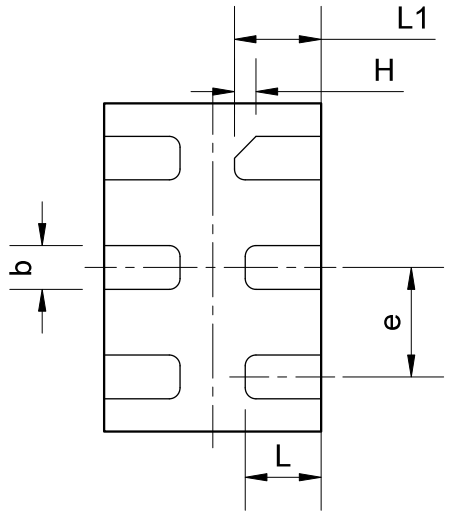
SOT23-6



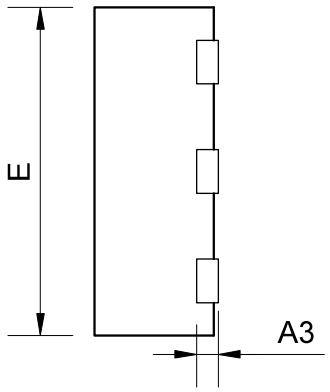
Dimensions Table (Units:mm)

Symbol	Min	Typ	Max
A	-	-	1.250
A1	0	-	0.150
A2	0.750	-	1.200
A3	0.350	0.650	0.700
b	0.360	-	0.460
b1	0.350	0.380	0.430
c	0.130	-	0.200
c1	0.120	0.150	0.160
D	2.820	2.926	3.026
E	2.600	2.800	3.000
E1	1.500	1.626	1.726
e	0.900	0.950	1.000
e1	1.800	1.900	2.000
L	0.300	0.400	0.500
L1	0.590 REF		
L2	0.250 BSC		
R	0.050	—	0.200
R1	0.050	—	0.200

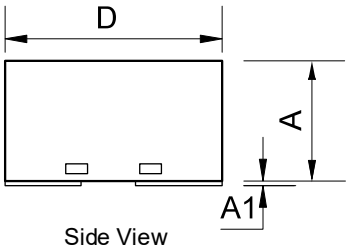
DFN6 (1.45mm*1.0mm)



Bottom View



Side View

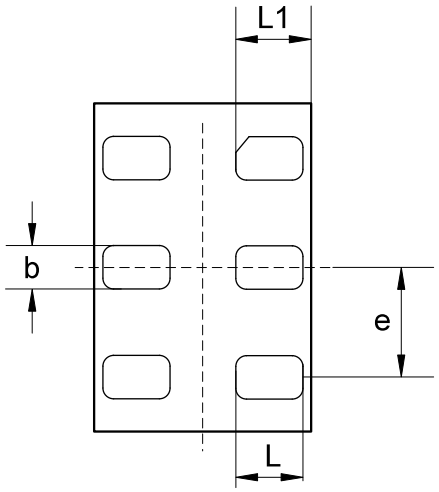


Side View

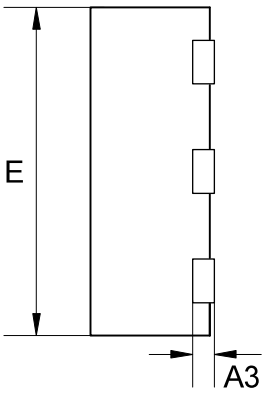
Dimensions Table (Units:mm)

SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	-	0.05
A3		0.15 REF	
b	0.18	0.23	0.28
D	0.95	1.00	1.05
E	1.40	1.45	1.50
e		0.50 BSC	
H		0.10 REF	
L	0.25	0.35	0.45
L1	0.30	0.40	0.50

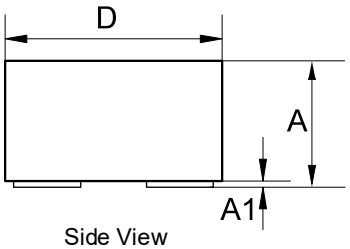
DFN6 (1.1mm*0.9mm)



Bottom View



Side View

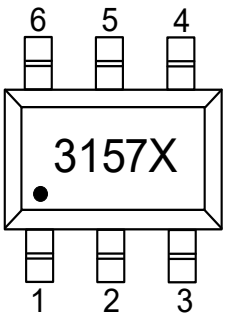


Side View

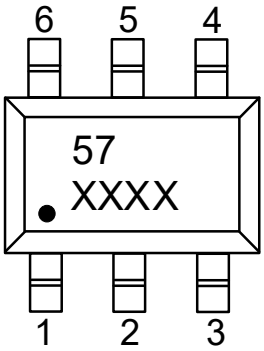
Dimensions Table (Units:mm)

SYMBOL	MIN	NOM	MAX
A	0.40	-	0.50
A1	0.00	-	0.05
A3		0.125 REF	
b	0.15	0.20	0.25
D	0.85	0.90	0.95
E	1.05	1.10	1.15
e		0.40 BSC	
L	0.25	0.30	0.35
L1	0.30	0.35	0.40

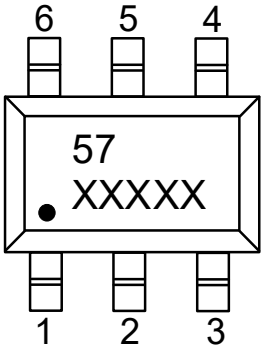
Marking



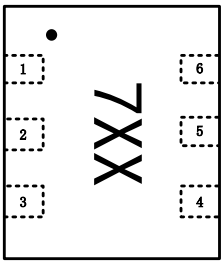
SC70-6 Marking
3157: Part Number
X: Tracking Number



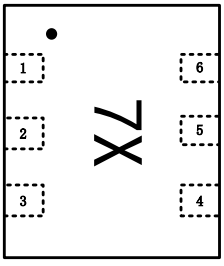
SC-88 Marking
57: Part Number
XXXX: Tracking Number



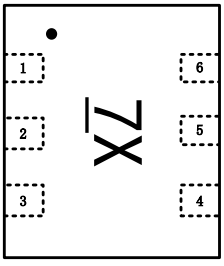
SOT23-6 Marking
57: Part Number
XXXXX: Tracking Number



DFN6(ET3157Y) Marking
7: Part Number
XX: Tracking Number



DFN6(ET3157Y1) Marking
7: Part Number
X: Tracking Number



DFN6(ET3157Y2) Marking
7: Part Number
X: Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.2	2020-09-05	Add SC70-5 PIN1 in tape	Liuxm	Liuxm	Zhujl
1.3	2021-8-11	Update Marking	Liuxm	Liuxm	Zhujl
1.4	2022-12-19	Update Typesetting Update t_P. characteristics	Shib	Shib	Liujy
1.5	2023-08-01	Update ESD & LU DFN6 package size	Tugz	Shib	Liujy
1.6	2023-12-10	Update SC70/SC-88 package	Shibo	Shib	Liujy
1.7	2024-01-15	Update EC table spec according to test data	Yinpeng	Shib	Liujy
1.8	2025-09-09	Add SOT23-6 package	Yinpeng	Shib	Liujy
1.9	2026-07-21	Add DFN6 (1.1mm*0.9mm) package	Yinpeng	Shib	Liujy