

Single D-type Flip-Flop with Reset; Positive-Edge Trigger

General Description

The ET74LVC1G175 is a low-power, low-voltage single positive edge triggered D-type flip-flop with individual data (D) input, clock (CP) input, master reset ($\overline{MR}$) input, and Q output.

The master reset ($\overline{MR}$) is an asynchronous active LOW input and operates independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device in a mixed 3.3V and 5V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging back-flow current through the device when it is powered down.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

Features

- Designed for 1.65V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- High Noise Immunity
- $\pm 32\text{mA}$ Balanced Output Sink and Source Capability
- CMOS Low Power Consumption
- I_{OFF} Circuitry Provides Partial Power-down Mode Operation
- Direct Interface with TTL Levels
- Multiple Package Options
- ESD Protection Complies with JESD22 Standard
 - HBM: $\pm 4000\text{V}$ Pass (JEDEC JS-001)
 - CDM: $\pm 1500\text{V}$ Pass (JEDEC JS-002)
- Latch-up Performance Exceeds $\pm 200\text{mA}$ per JEDEC JESD78F
- Part No. and Package Information

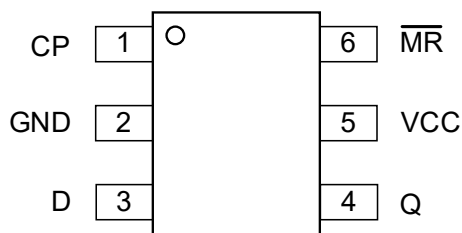
Part No.	Package	Packing Option	MSL
ET74LVC1G175	SC70-6 (1.3mm $\times$ 2.1mm)	Tape and Reel, 3K/Reel	1
ET74LVC1G175T	SOT23-6 (1.6mm $\times$ 2.9mm)	Tape and Reel, 3K/Reel	3

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Applications

- Server
- LED Display Screen
- Network Switches
- Telecommunications Infrastructure
- Motor Driver
- I/O Extender

Pin Configuration



SC70-6/SOT23-6

Figure1. Pin Configuration

Pin Function

SC70-6/SOT23-6

Pin No.	Pin Name	Pin Function
1	CP	Clock Input (Low-to-High, Edge-Triggered)
2	GND	Ground
3	D	Data Input
4	Q	Flip-Flop Output
5	VCC	Supply Voltage
6	MR	Master Reset Input (Active LOW)

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Functional Diagram

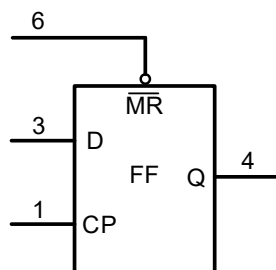


Figure2. Logic Symbol

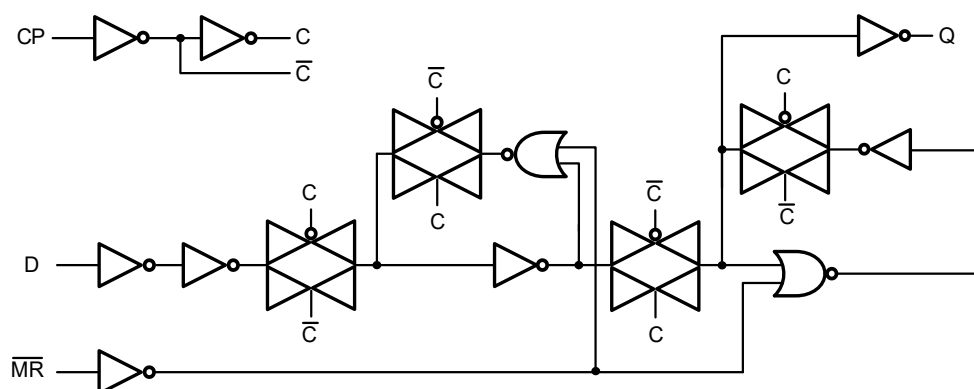


Figure3. Logic Diagram

Function Table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;

↑ = LOW-to-HIGH CP transition; X = don't care.

Operating Mode	Input			Output
	$\overline{MR}$	CP	D	Q
Reset (Clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

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Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 6.5	V
I _{IK}	DC Input Diode Current, V _I < GND		-50	mA
V _I	DC Input Voltage ⁽¹⁾		-0.5 ≤ V _I ≤ 6.5	V
I _{OK}	DC Output Diode Current, V _O < GND		±50	mA
V _O	DC Output Voltage Output in Higher or Low State		-0.5 to V _{CC} + 0.5	V
I _O	DC Output Sink Current, V _O = 0V to V _{CC}		±50	mA
I _{CC}	DC Supply Current per Supply Pin		100	mA
I _{GND}	DC Ground Current per Supply Pin		-100	mA
T _J	Max Junction Temperature		150	°C
T _{STG}	Storage Temperature Range		-65 to 150	°C
V _{ESD}	ESD Classification	Human Body Model ⁽²⁾	±4000	V
		Charged Device Model ⁽³⁾	±1500	
I _{LU}	Max Latch Up Current Above V _{CC} and GND at 125°C ⁽⁴⁾		±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage Operating		1.65	5.5	V
V _I	DC Input Voltage		0	V _{CC}	V
V _O	DC Output Voltage (High or Low State)		0	V _{CC}	V
T _A	Operating Temperature Range		-40	125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 1.65V to 2.7V		20	ns/V
		V _{CC} = 2.7V to 5.5V		10	

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Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65~1.95	0.65V _{CC}			0.65V _{CC}		V
			2.3~2.7	1.7			1.7		
			2.7~3.6	2.0			2.0		
			4.5~5.5	0.7V _{CC}			0.7V _{CC}		
V _{IL}	Low-Level Input Voltage		1.65~1.95			0.35V _{CC}		0.35V _{CC}	V
			2.3~2.7			0.7		0.7	
			2.7~3.6			0.8		0.8	
			4.5~5.5			0.3V _{CC}		0.3V _{CC}	
V _{OH}	High-Level Output Voltage	I _{OH} = -100uA	1.65~5.5	V _{CC} - 0.1			V _{CC} - 0.1		V
		I _{OH} = -4mA	1.65	1.2	1.54		0.95		
		I _{OH} = -8mA	2.3	1.9	2.15		1.7		
		I _{OH} = -12mA	2.7	2.2	2.5		1.9		
		I _{OH} = -24mA	3.0	2.3	2.62		2.0		
		I _{OH} = -32mA	4.5	3.8	4.11		3.4		
V _{OL}	Low-Level Output Voltage	I _{OL} = 100uA	1.65~5.5			0.10		0.10	V
		I _{OL} = 4mA	1.65		0.07	0.45		0.70	
		I _{OL} = 8mA	2.3		0.09	0.30		0.45	
		I _{OL} = 12mA	2.7		0.16	0.40		0.60	
		I _{OL} = 24mA	3.0		0.17	0.55		0.80	
		I _{OL} = 32mA	4.5		0.18	0.55		0.80	
I _I	Input Leakage Current	V _I = 5.5V or GND	0~5.5		±0.1	±5		±20	uA
I _{OFF}	Power Off Leakage Current	V _I = 5.5V or V _O = 5.5V	0		±0.1	±10		±20	uA
I _{CC}	Quiescent Supply Current	V _I = 5.5V or GND	1.65~5.5		0.1	10		40	uA
ΔI _{CC}	Additional Supply Current	Per Pin: V _I = V _{CC} - 0.6V; I _O = 0mA	2.3~5.5		5.0	500		500	uA

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AC Electrical Characteristics

Voltages are referenced to GND (ground = 0V); for test circuit see [Figure6](#).

Symbol	Parameter	Conditions	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
			Min	Typ ⁽⁵⁾	Max	Min	Max	
t _{pd}	Propagation Delay	CP to Q; See Figure4						ns
		V _{CC} = 1.65V to 1.95V	1.5	7.2	13.4	1.5	17	
		V _{CC} = 2.3V to 2.7V	1.0	4.2	7.1	1.0	9.0	
		V _{CC} = 2.7V	1.0	3.9	7.1	1.0	9.0	
		V _{CC} = 3.0V to 3.6V	1.0	3.8	5.7	0.5	7.5	
		V _{CC} = 4.5V to 5.5V	1.0	2.6	4.0	0.5	5.5	
		$\overline{\text{MR}}$ to Q; See Figure5						
		V _{CC} = 1.65V to 1.95V	1.5	6.0	12.9	1.5	17	
		V _{CC} = 2.3V to 2.7V	1.0	3.6	7.0	1.0	9.0	
		V _{CC} = 2.7V	1.0	3.6	7.0	1.0	9.0	
		V _{CC} = 3.0V to 3.6V	1.0	3.0	5.8	0.5	7.5	
		V _{CC} = 4.5V to 5.5V	1.0	2.5	4.1	0.5	5.5	
t _w	Pulse Width	CP H or L; See Figure4						ns
		V _{CC} = 1.65V to 1.95V	6.2			6.2		
		V _{CC} = 2.3V to 2.7V	2.7			2.7		
		V _{CC} = 2.7V	2.7			2.7		
		V _{CC} = 3.0V to 3.6V	2.7			2.7		
		V _{CC} = 4.5V to 5.5V	2.0			2.0		
		$\overline{\text{MR}}$ Low; See Figure5						
		V _{CC} = 1.65V to 1.95V	6.2			6.2		
		V _{CC} = 2.3V to 2.7V	2.7			2.7		
		V _{CC} = 2.7V	2.7			2.7		
		V _{CC} = 3.0V to 3.6V	2.7			2.7		
		V _{CC} = 4.5V to 5.5V	2.0			2.0		
t _{rec}	Recovery Time	$\overline{\text{MR}}$; See Figure5						ns
		V _{CC} = 1.65V to 1.95V	1.9			1.9		
		V _{CC} = 2.3V to 2.7V	1.4			1.4		
		V _{CC} = 2.7V	1.3			1.3		
		V _{CC} = 3.0V to 3.6V	1.2			1.2		
		V _{CC} = 4.5V to 5.5V	1.0			1.0		
t _{su}	Set-up Time	D to CP; See Figure4						ns
		V _{CC} = 1.65V to 1.95V	2.9			2.9		
		V _{CC} = 2.3V to 2.7V	1.7			1.7		
		V _{CC} = 2.7V	1.7			1.7		
		V _{CC} = 3.0V to 3.6V	1.3			1.3		
		V _{CC} = 4.5V to 5.5V	1.1			1.1		

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AC Electrical Characteristics (Continued)

Voltages are referenced to GND (ground = 0V); for test circuit see [Figure6](#); for wave forms see [Figure4](#) and [Figure5](#).

Symbol	Parameter	Conditions	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
			Min	Typ ⁽⁵⁾	Max	Min	Max	
t _h	Hold time	D to CP; See Figure4						ns
		V _{CC} = 1.65V to 1.95V	0.0			0.0		
		V _{CC} = 2.3V to 2.7V	0.3			0.3		
		V _{CC} = 2.7V	0.5			0.5		
		V _{CC} = 3.0V to 3.6V	1.2			1.2		
		V _{CC} = 4.5V to 5.5V	0.5			0.5		
f _{max}	Maximum Frequency	D; See Figure4						MHz
		V _{CC} = 1.65V to 1.95V	80	125		80		
		V _{CC} = 2.3V to 2.7V	175			175		
		V _{CC} = 2.7V	175			175		
		V _{CC} = 3.0V to 3.6V	175			175		
		V _{CC} = 4.5V to 5.5V	200			200		

Note5: All typical values are measured at corresponding V_{CC} and T_A = 25°C.

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5V, V _I = 0V or V _{CC}	4.5	pF
C _{PD}	Power Dissipation Capacitance ⁽⁶⁾	10MHz, V _{CC} = 3.3V, V _I = 0V or V _{CC}	19	pF

Note6: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = Input Frequency in MHz;

f_o = Output Frequency in MHz;

C_L = Output Load capacitance in pF;

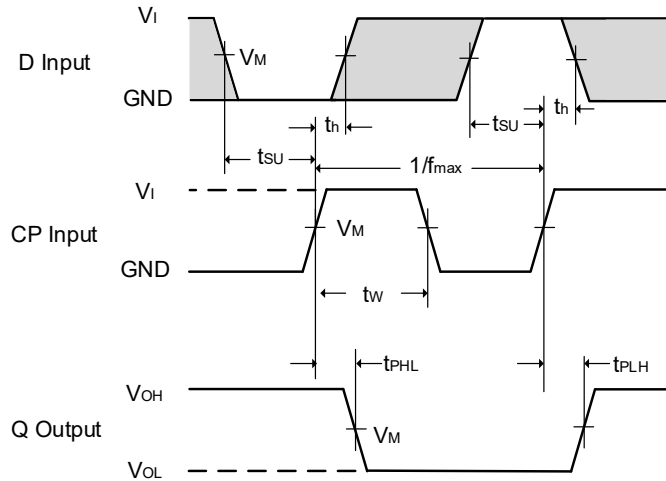
V_{CC} = Supply Voltage in V;

N = Number of Inputs Switching;

Σ(C_L × V_{CC}² × f_o) = Sum of Outputs.

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Test Waveform

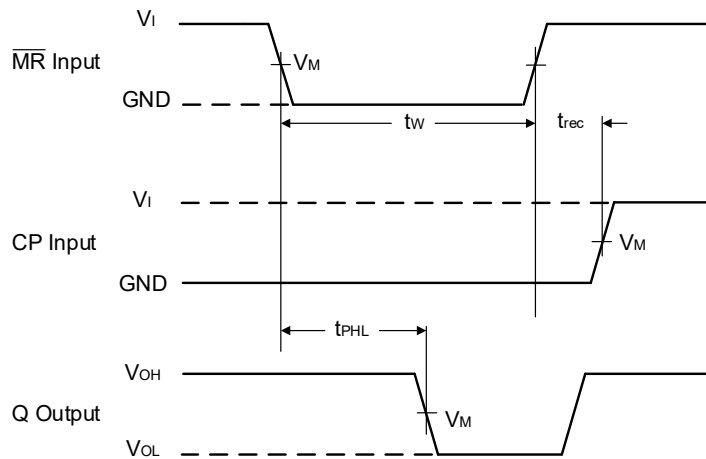


Measurement points are given in [Table 1](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure4. The clock input (CP) to output (Q) propagation delays, the clock pulse width, D to CP set-up, CP to D hold times, and the maximum clock pulse frequency



Measurement points are given in [Table 1](#).

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

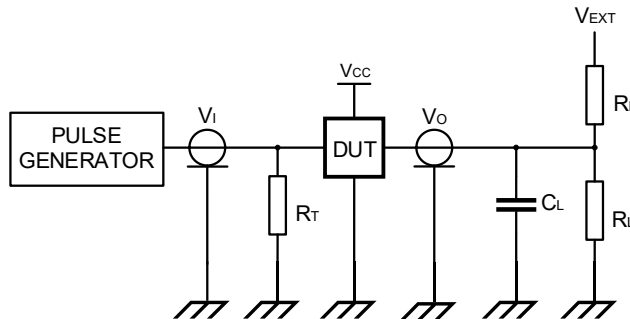
Figure5. The master reset ($\overline{MR}$) input to output (Q) propagation delays, the master reset pulse widths, and the $\overline{MR}$ to CP recovery time

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Table1.Measurement Points

Supply Voltage	Input	Output
V_{CC}	V_M	V_M
1.65V to 1.95V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3V to 2.7V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7V	1.5V	1.5V
3.0V to 3.6V	1.5V	1.5V
4.5V to 5.5V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

Test Circuit



Measurement points are given in [Table2](#).

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Figure6. Load circuit for switching times

Table2.Test Data

Supply Voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
1.65V to 1.95V	V_{CC}	$\leq 3.0ns$	30pF	1k Ω	Open
2.3V to 2.7V	V_{CC}	$\leq 3.0ns$	30pF	500 Ω	Open
2.7V	2.7V	$\leq 3.0ns$	50pF	500 Ω	Open
3.0V to 3.6V	2.7V	$\leq 3.0ns$	50pF	500 Ω	Open
4.5V to 5.5V	V_{CC}	$\leq 3.0ns$	50pF	500 Ω	Open

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Layout Guide

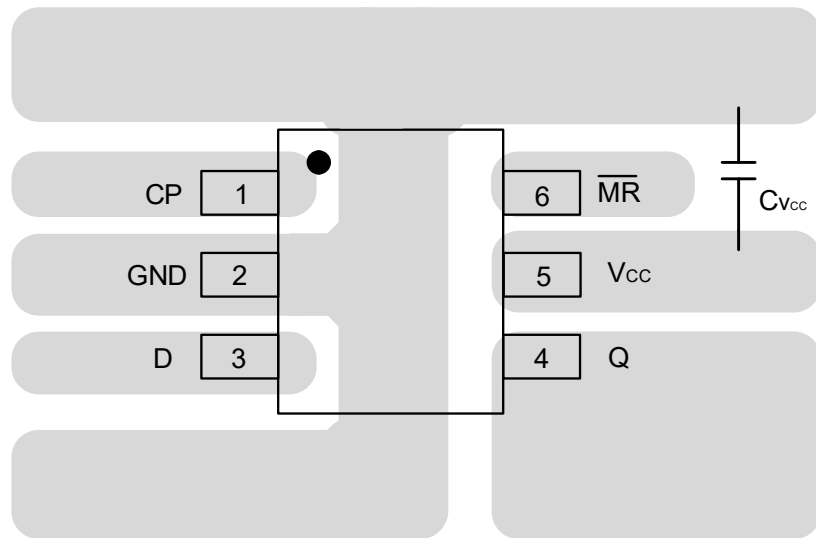
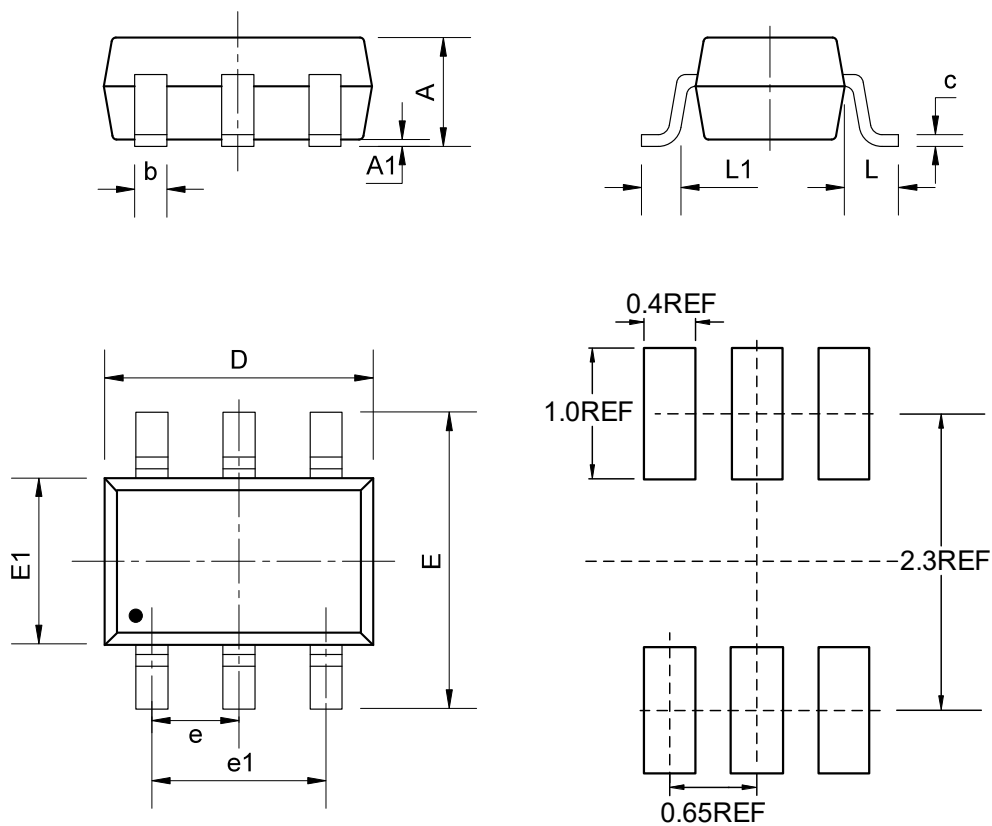


Figure7. Layout Guide

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Package Dimension

SC70-6 (1.3mm × 2.1mm)



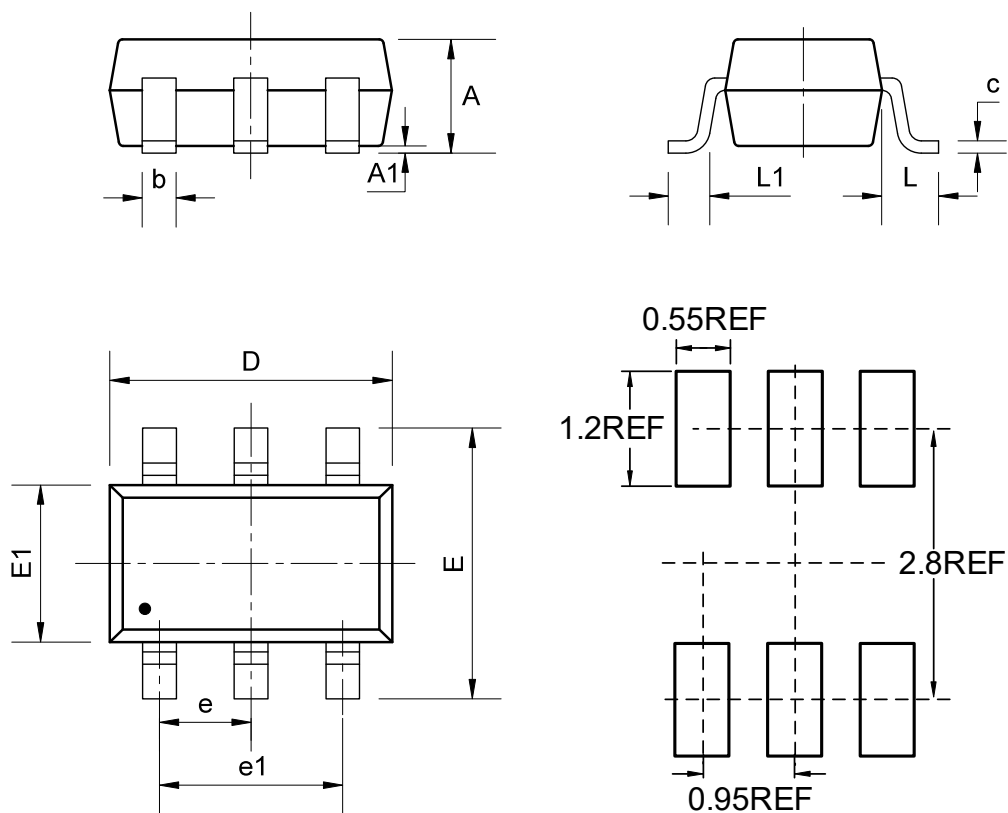
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
b	0.15	-	0.35
c	0.08	-	0.20
D	2.00	2.10	2.30
e	0.65BSC		
e1	1.30BSC		
E	2.15	2.30	2.50
E1	1.15	1.30	1.45
L	0.50REF		
L1	0.33REF		

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SOT23-6 (1.6mm × 2.9mm)



COMMON DIMENSIONS

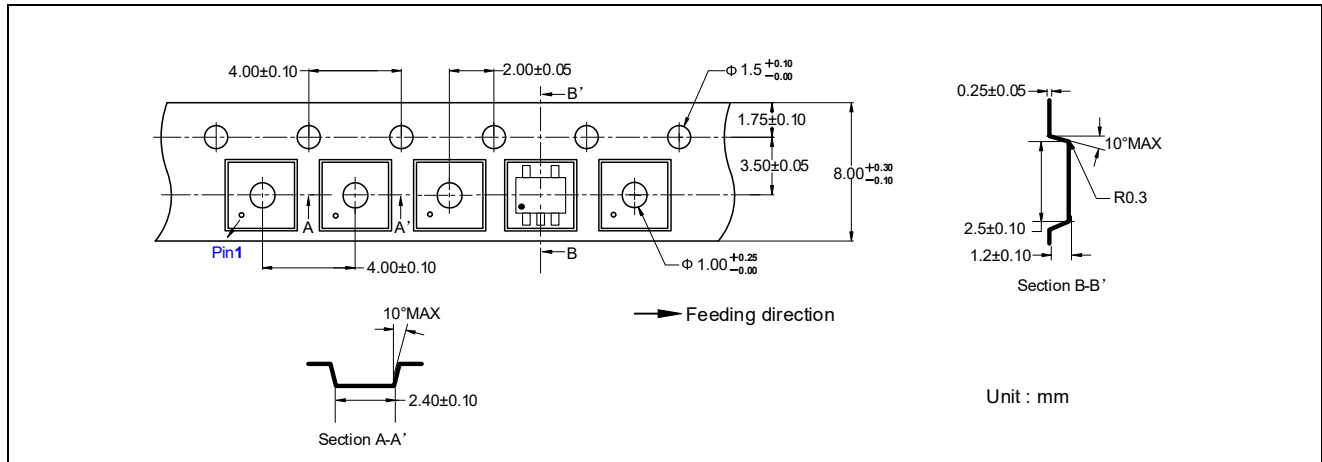
(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0.00	-	0.15
b	0.28	0.35	0.50
c	0.08	0.15	0.22
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

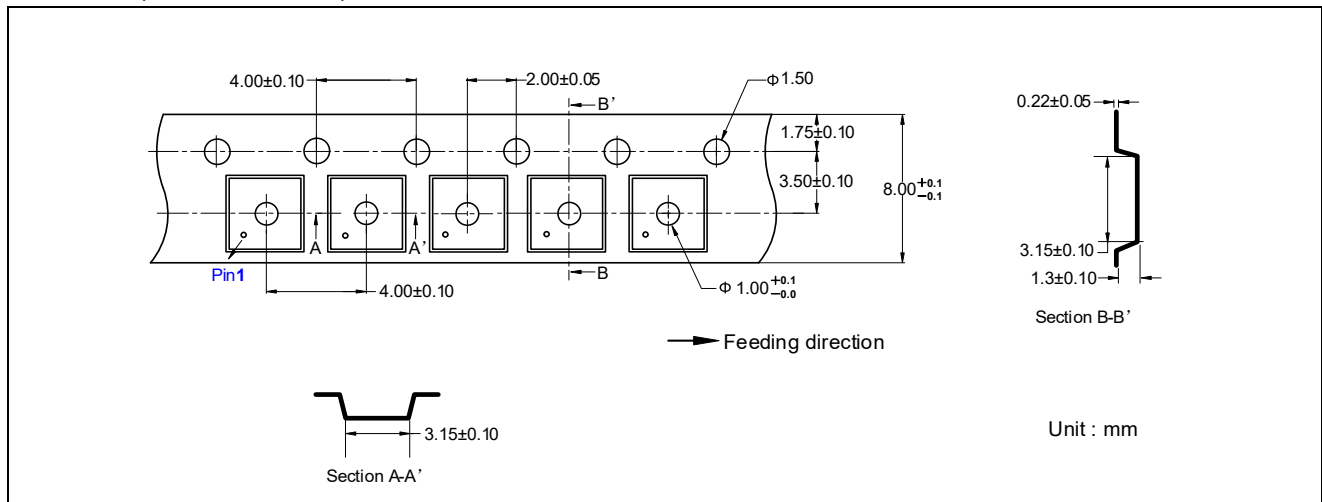
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Tape Information

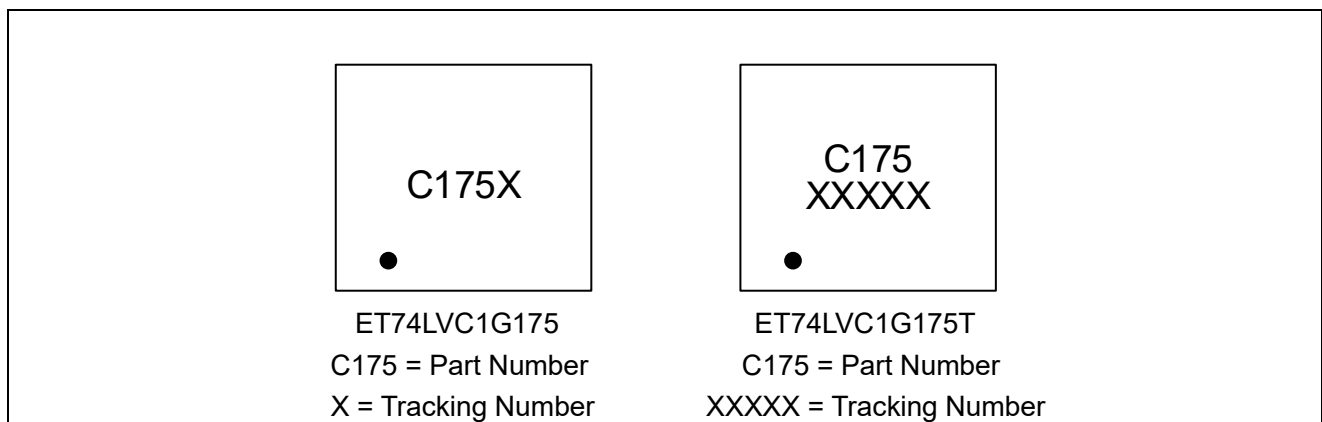
SC70-6 (1.3mm × 2.1mm)



SOT23-6 (1.6mm × 2.9mm)



Marking Information



ET74LVC1G175

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-08-14	Preliminary Version	Xu tao	Tu guozhu	Liu jiaying
1.0	2025-03-29	Official Version	Wang anran	Yang xiaoxu	Liu jiaying
1.1	2025-05-27	Add Packing Option	Yang xiaoxu	Yang xiaoxu	Liu jiaying
1.2	2026-05-08	Update Format and Package, Add Marking	Xu tao	Yang xiaoxu	Liu jiaying