8-bit D-type Transparent Latch with 3-state Outputs

Description

The ET74HC573 is an 8-bit D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable ($\overline{OE}$) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features

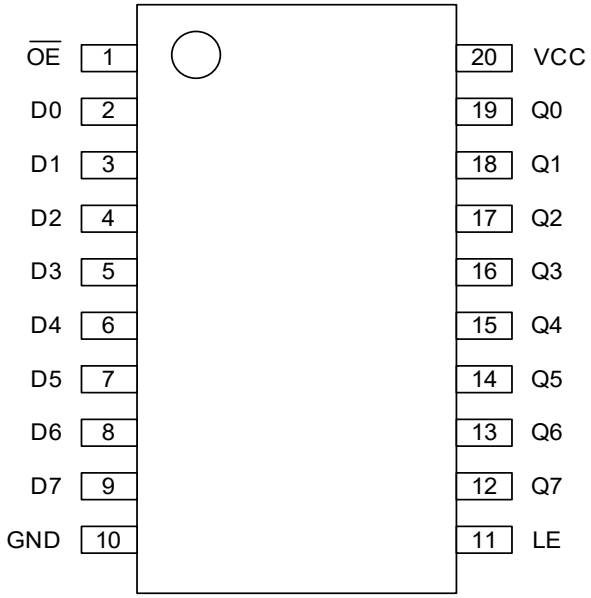
- Designed for 2V to 6V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 6V
- ±8mA Balanced Output Sink and Source Capability
- Input levels: CMOS level
- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors and Microcomputers
- 3-state Non-inverting Outputs for Bus-oriented Applications
- Common 3-state Output Enable Input
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±2000V Pass (JEDEC JS-001)
  -- CDM: ±1000V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74HC573V	TSSOP20 (6.5mm × 4.4mm)	Tape and Reel, 4K/Reel	3

Applications

- Memory Chip Select Decoding
- Data Transmission System

Pin Configuration



TSSOP20

Figure1. Pin Configuration

Pin Function

Pin Number	Pin Symbol	Description
1	$\overline{OE}$	3-state Output Enable Input (Active LOW)
2~9	D0~A7	Data Input
10	GND	GND
11	LE	Latch Enable Input (Active HIGH)
12~19	Q7~Q0	3-state Latch Output
20	VCC	Supply Voltage

Block Diagram

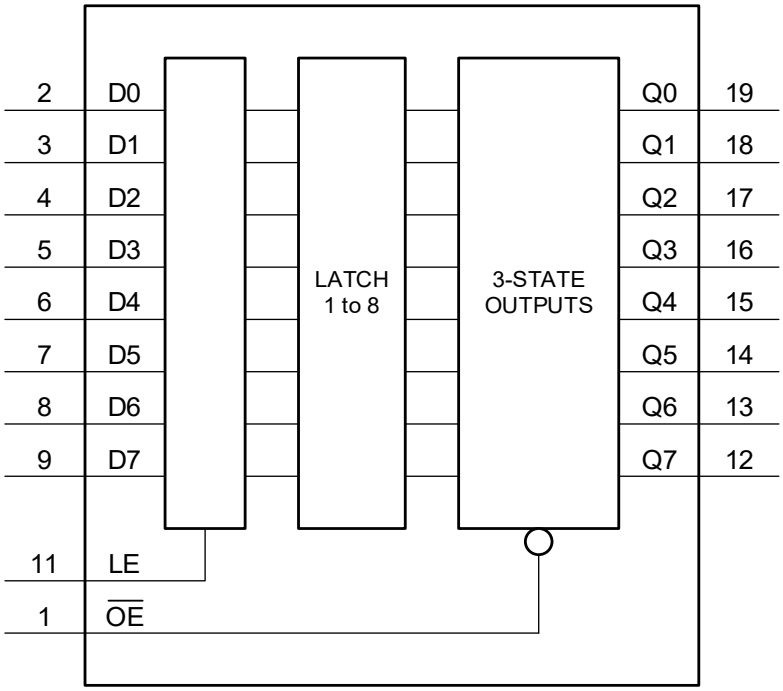


Figure2. Functional Diagram

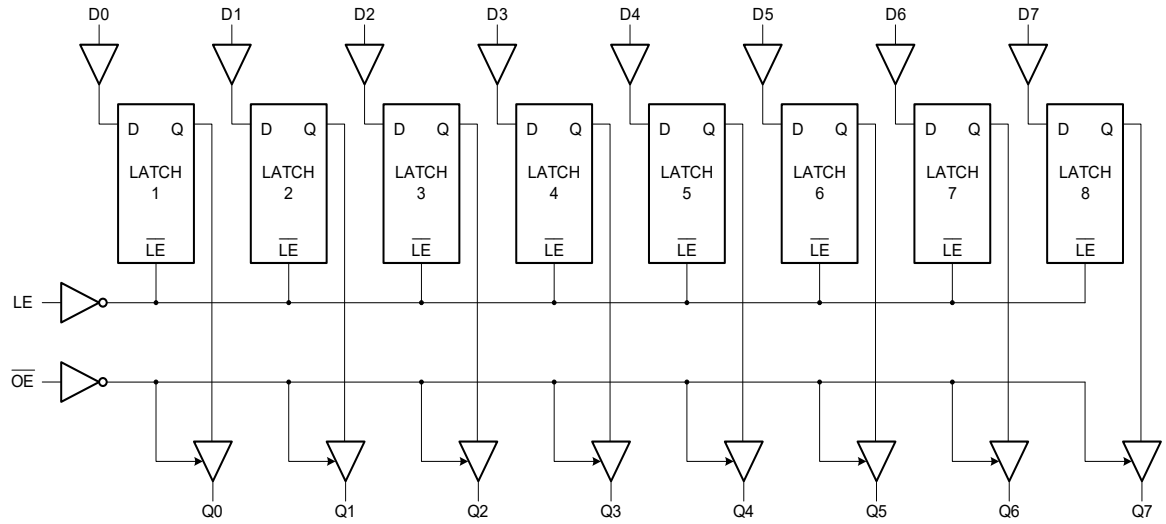


Figure3. Logic Diagram

Functional Description

Operating Mode	Control		Input	Intemal Latches	Output
	$\overline{OE}$	LE	Dn		Qn
Enable and Read Register (Transparent Mode)	L	H	L	L	L
			H	H	H
Latch and Read Register	L	L	l	L	L
			h	H	H
Latch Register and Disable Outputs	H	L	l	L	Z
			h	H	Z

Note: H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition, L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition, Z = High-impedance OFF-state.

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 6.5	V
V_I	DC Input Voltage (1)		-0.5 to V_{CC}	V
V_O	DC Output Voltage		-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current, V_I < -0.5V or V_I > V_{CC} + 0.5V		±20	mA
I_{OK}	DC Output Diode Current, V_O < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	DC Output Sink Current, V_O = -0.5V to (V_{CC} + 0.5V)		±35	mA
I_{CC}	DC Supply Current per Supply Pin		70	mA
I_{GND}	DC Ground Current per Supply Pin		-70	mA
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to 150	°C
V_{ESD}	ESD Classification	Human Body Model (2)	±2000	V
		Charged Device Model (3)	±1500	
I_{LU}	Max Latch Up Current Above V_{CC} and GND (4)		±200	mA
P_D	Total Power Dissipation		500	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level Input Voltage		2	1.5	1.2		1.5		V
			4.5	3.15	2.4		3.15		V
			6	4.2	3.2		4.2		V
V_{IL}	LOW-level Input Voltage		2		0.8	0.5		0.5	V
			4.5		2.1	1.35		1.35	V
			6		2.8	1.8		1.8	V
V_{OH}	HIGH-level Output Voltage	I_{OH} = -20μA	2	1.9	2.0		1.9		V
		I_{OH} = -20μA	4.5	4.4	4.5		4.4		V
		I_{OH} = -20μA	6	5.9	6.0		5.9		V
		I_{OH} = -6.0mA	4.5	3.98	4.32		3.7		V
		I_{OH} = -8mA	6	5.48	5.81		5.2		V
V_{OL}	LOW-level Output Voltage	I_{OL} = 20μA	2		0	0.1		0.1	V
		I_{OL} = 20μA	4.5		0	0.1		0.1	V
		I_{OL} = 20μA	6		0	0.1		0.1	V
		I_{OL} = 6.0mA	4.5		0.15	0.26		0.4	V
		I_{OL} = 8mA	6		0.16	0.26		0.4	V
I_I	Input Leakage Current	V_I = V_{CC} or GND	6			±0.1		±1.0	μA
I_{OZ}	OFF-state Output Current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	6			±0.5		±10	μA
I_{CC}	Supply Current	V_I = V_{CC} or GND I_O = 0mA	6			8.0		160	μA

Dynamic Characteristics

Symbol	Parameter	Conditions	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t_{pd}	Propagation Delay	Dn to Qn							
		C_L = 50pF	2		47	150		225	ns
		C_L = 50pF	4.5		17	30		45	ns
		C_L = 15pF	5		14				ns
		C_L = 50pF	6		14	26		38	ns
		LE to Qn							
		C_L = 50pF	2		50	150		225	ns
		C_L = 50pF	4.5		18	30		45	ns
		C_L = 15pF	5		15				ns
		C_L = 50pF	6		14	26		38	ns
t_{en}	Enable Time	$\overline{OE}$ to Qn							
		C_L = 50pF	2		44	140		210	ns
		C_L = 50pF	4.5		16	28		42	ns
		C_L = 50pF	6		13	24		36	ns
t_{dis}	Disable Time	$\overline{OE}$ to Qn							
		C_L = 50pF	2		55	150		225	ns
		C_L = 50pF	4.5		20	30		45	ns
		C_L = 50pF	6		16	26		38	ns
t_t	Transition Time	Qn							
		C_L = 50pF	2		14	60		90	ns
		C_L = 50pF	4.5		5	12		18	ns
		C_L = 50pF	6		4	10		15	ns
t_w	Pulse Width	LE HIGH							
		C_L = 50pF	2	80	14		120		ns
		C_L = 50pF	4.5	16	5		24		ns
		C_L = 50pF	6	14	4		20		ns
t_{su}	Set-up Time	Dn to LE							
		C_L = 50pF	2	50	11		75		ns
		C_L = 50pF	4.5	10	4		15		ns
		C_L = 50pF	6	9	3		13		ns
t_h	Hold Time	Dn to LE							
		C_L = 50pF	2	5	3		5		ns
		C_L = 50pF	4.5	5	1		5		ns
		C_L = 50pF	6	5	1		5		ns

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_I	Input Capacitance	V_{CC} = 6V, V_I = 0V or V_{CC}	3.5	pF
C_{PD}	Power Dissipation Capacitance (5)	C_L = 50pF, 1MHz, V_{CC} = 6V, V_I = 0V or V_{CC}	26	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Dynamic Characteristics Test Waveform

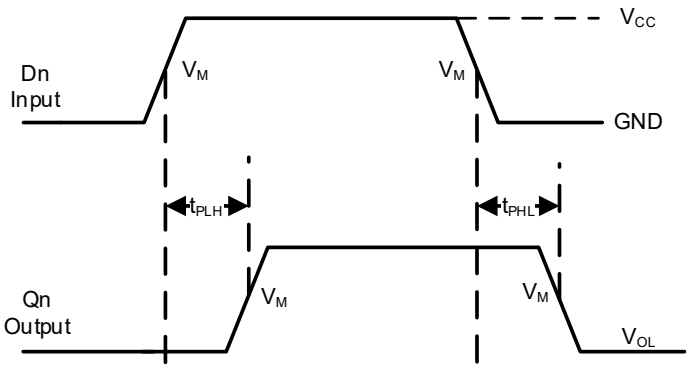


Figure3. Propagation Delay Data Input (Dn) to Output (Qn) and Output Transition Time

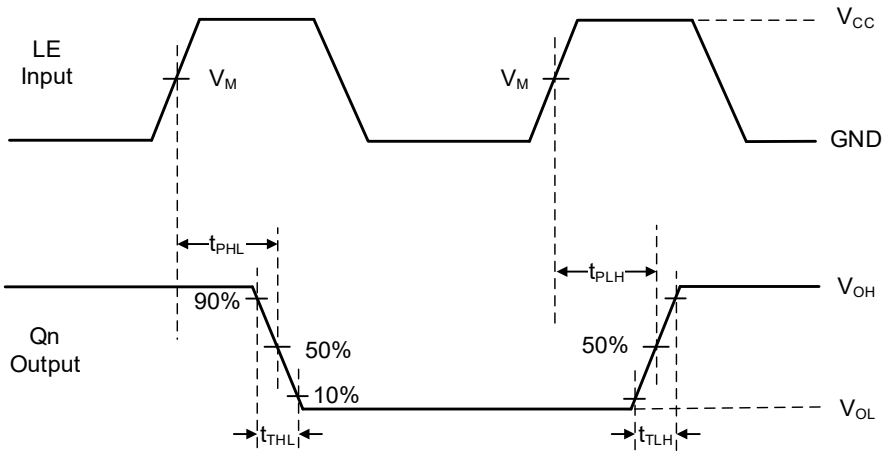


Figure4. Pulse Width Latch Enable Input (LE)
Propagation Delay Latch Enable Input (LE) to Output (Qn) and Output Transition Time

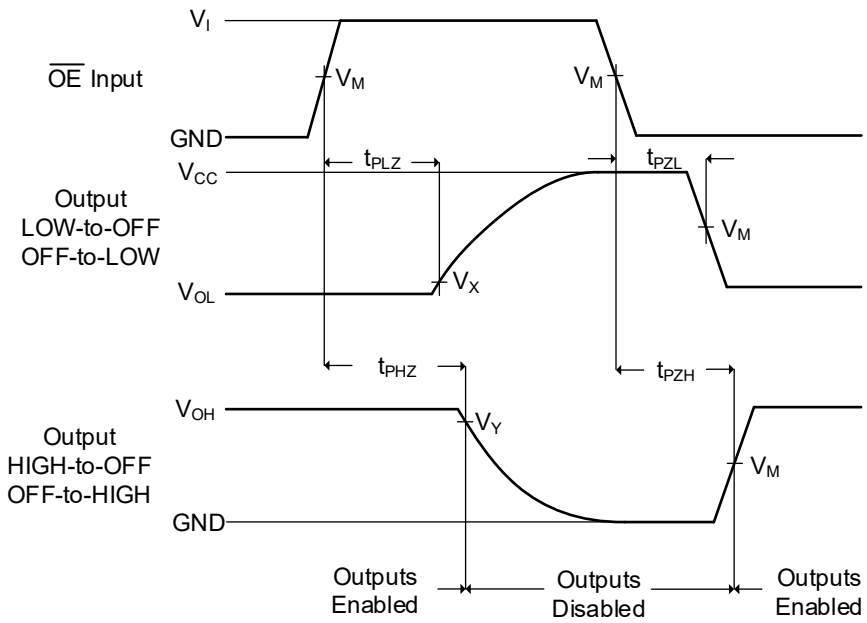


Figure5. Enable and Disable Times

V_{OL} and V_{OH} are Typical Voltage Output Levels that Occur with the Output Load

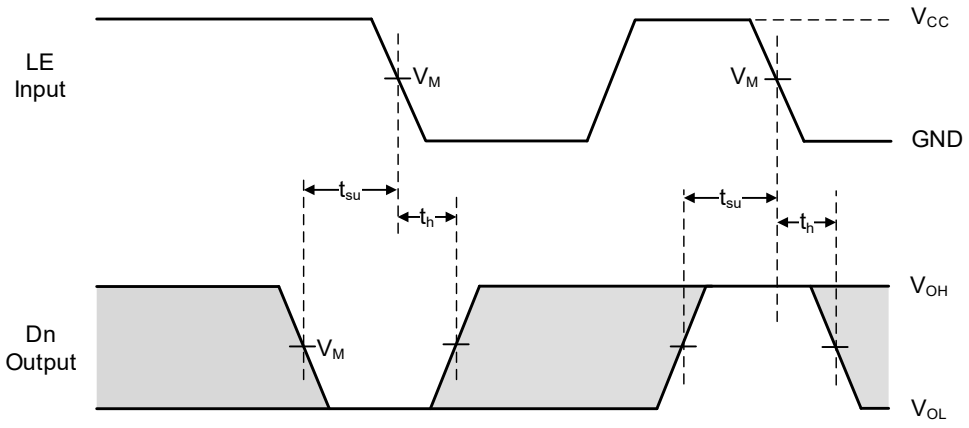


Figure6. Set-up and Hold Times for Data Input (Dn) to Latch Input (LE)

The Shaded Areas Indicate when the Input is Permitted to Change for Predictable Output Performance

Measurement points

Input V_M	Output V_M
$0.5V_{CC}$	$0.5V_{CC}$

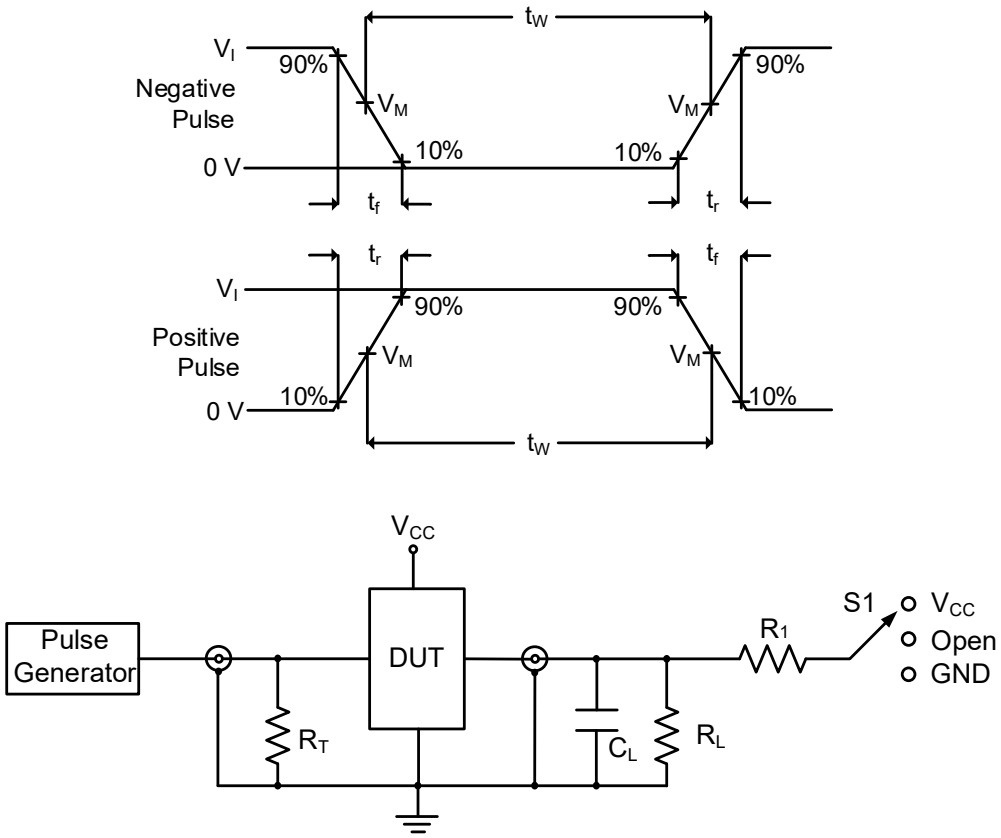


Figure7. Test Circuit for Measuring Switching Times

Definitions test circuits:

R_T = Termination resistance should be equal to output impedance Zo of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

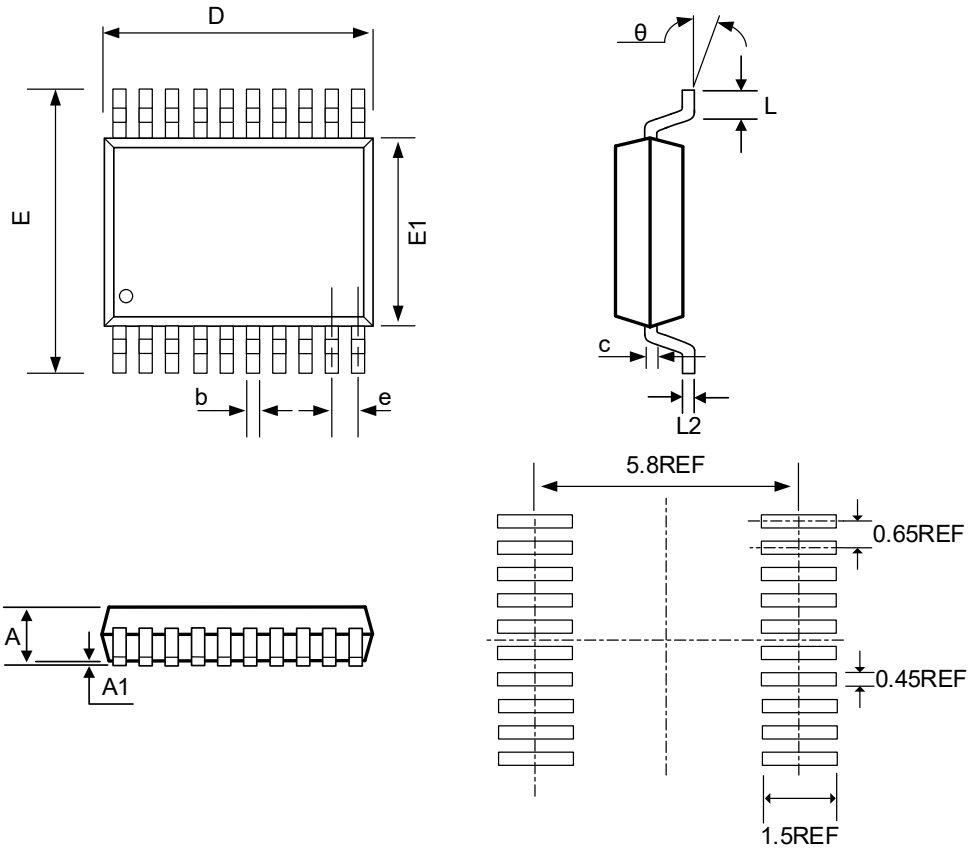
S1 = Test selection switch.

Test Data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL},t_{PLH}	t_{PZH},t_{PHZ}	t_{PZL},t_{PLZ}
V_{CC}	6ns	15pF,50pF	1kΩ	open	GND	V_{CC}

Package Dimension

TSSOP20 (6.5mm × 4.4mm)



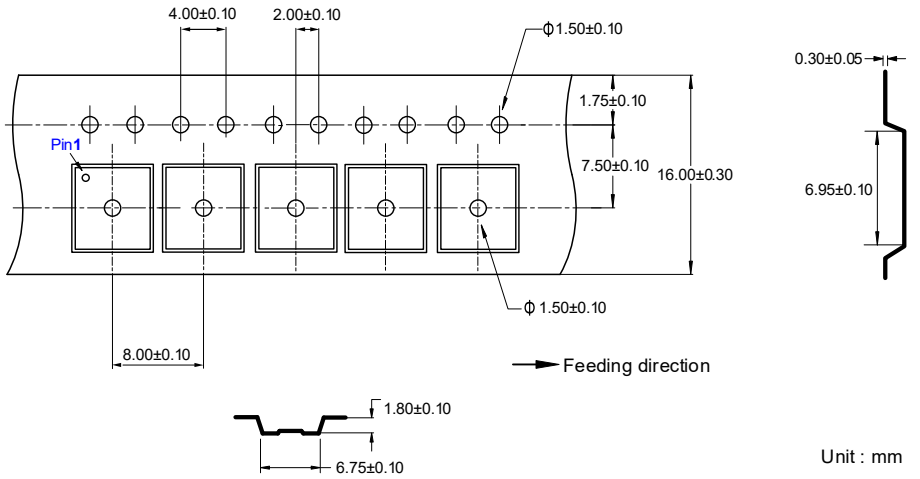
COMMON DIMENSIONS

(Unit: mm)

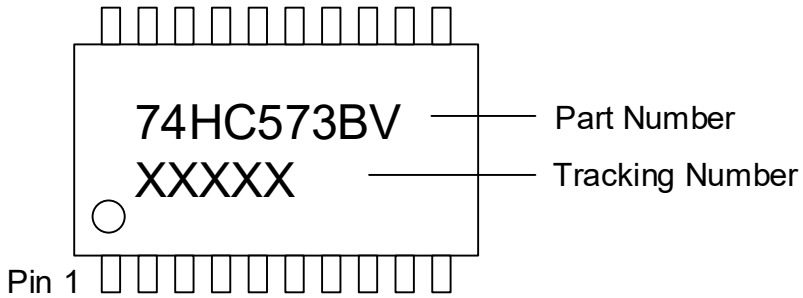
SYMBOL	MIN	MAX
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 REF	
D	6.40	6.60
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.50	0.72
L2	0.25 REF	
θ	0°	8°

Tape Information

TSSOP20 (4.4mm × 6.5mm)



Marking Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.1	2022-10-12	Preliminary	Zhu ziqiang Shi bo	Chenhui	Liu jiaying
1.0	2023-08-24	Official version Add Tape and Marking	Zhu ziqiang	Chenhui	Liu jiaying
1.1	2026-06-10	Update Format, Package and Tape	Xu tao	Yang xiaoxu	Liu jiaying