Dual Buffer Driver With 3-State Outputs

General Description

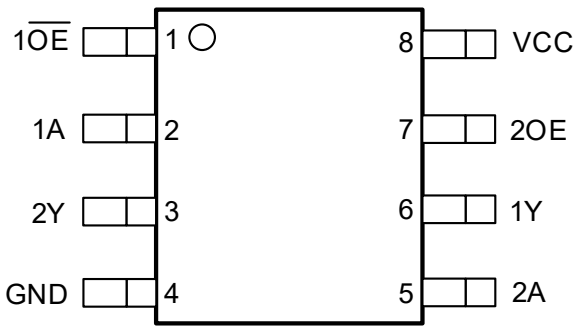
The ET74HC2G241 is a dual buffer driver with 3-state outputs operating from a 1.65V to 5.5V supply. This device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive.

Features

- Designed for 2V to 6V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 6V
- ±5.2mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±2000V Pass (JEDEC JS-001)
  -- CDM: ±1000V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74HC2G241U	VSSOP8 (2.0mm × 2.3mm)	Tape and Reel, 3K/Reel	3

Pin Configuration



VSSOP8

Figure1. Pin Configuration

Pin Function

Pin No.	Pin Name	Function
1	$1\overline{OE}$	Channel 1, Enable Input
2	1A	Channel 1, Input A
3	2Y	Channel 2, Output Y
4	GND	Ground
5	2A	Channel 2, Input A
6	1Y	Channel 1, Output Y
7	2OE	Channel 2, Enable Input
8	VCC	Supply Voltage

Block Diagram

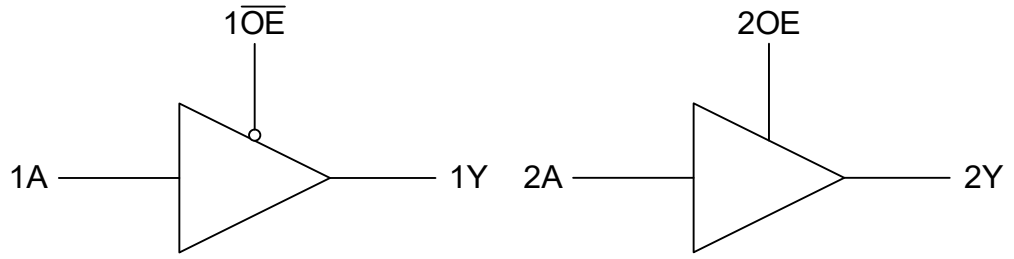


Figure2. Logic Symbol

Functional Table

Input		Output
$1\overline{OE}$	**1A**	**1Y**
L	L	L
L	H	H
H	H	Z
H	L	Z
2OE	**2A**	**2Y**
H	L	L
H	H	H
L	L	Z
L	H	Z

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 7.0	V
I_{IK}	DC Input Diode Current, V_I < GND		-50	mA
V_I	DC Input Voltage (1)		-0.5 ≤ V_I ≤ 7.0	V
I_{OK}	DC Output Diode Current, V_O < GND		±50	mA
V_O	DC Output Voltage Output in Higher or Low State		-0.5 to V_{CC} + 0.5	V
I_O	DC Output Sink Current, V_O = -0.5 to V_{CC} + 0.5		±50	mA
I_{CC}	DC Supply Current per Supply Pin		100	mA
I_{GND}	DC Ground Current per Supply Pin		-100	mA
T_J	Max Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to 150	°C
V_{ESD}	ESD Classification	Human Body Model (2)	±2000	V
		Charged Device Model (3)	±1000	
I_{LU}	Max Latch Up Current Above V_{CC} and GND at 125°C (4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage Operating		2	6	V
V_I	DC Input Voltage		0	V_{CC}	V
V_O	DC Output Voltage (High or Low State)		0	V_{CC}	V
T_A	Operating Temperature Range		-40	125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V		625	ns/V
		V_{CC} = 4.5V		139	
		V_{CC} = 6.0V		83	

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0	1.5	1.2		1.5		V
			4.5	3.15	2.4		3.15		
			6.0	4.2	3.2		4.2		
V_{IL}	Low-Level Input Voltage		2.0		0.8	0.5		0.5	V
			4.5		2.1	1.35		1.35	
			6.0		2.8	1.8		1.8	
V_{OH}	High-Level Output Voltage	I_{OH} = -20uA	2.0	1.9	2.0		1.9		V
		I_{OH} = -20uA	4.5	4.4	4.5		4.4		
		I_{OH} = -20uA	6.0	5.9	6.0		4.4		
		I_{OH} = -4.0mA	4.5	3.84	4.32		3.7		
		I_{OH} = -5.2mA	6.0	5.34	5.81		5.2		
V_{OL}	Low-Level Output Voltage	I_{OL} = 20uA	2.0		0	0.1		0.1	V
		I_{OL} = 20uA	4.5		0	0.1		0.1	
		I_{OL} = 20uA	6.0		0	0.1		0.1	
		I_{OL} = 4.0mA	4.5		0.15	0.33		0.4	
		I_{OL} = 5.2mA	6.0		0.16	0.33		0.4	
I_I	Input Leakage Current	V_I = 6.0V or GND	6.0			±1		±1	uA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	6.0			±5		±10	uA
I_{CC}	Quiescent Supply Current	Per Pin: V_I = 6.0V or GND; I_O = 0mA	6.0			10		20	uA

AC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay (xA to xY; See Figure3)	C_L = 50pF	2.0		12	15.6		16	ns
		C_L = 50pF	4.5		3	3.9		4.1	
		C_L = 15pF	5.0		3				
		C_L = 50pF	6.0		2.8	3.6		3.8	
t_{PZL}, t_{PZH}	Output Enable Time (1$\overline{OE}$ to 1Y; See Figure4)	C_L = 50pF	2.0		11.4	14.8		15.2	ns
		C_L = 50pF	4.5		3.3	4.3		4.5	
		C_L = 50pF	6.0		2.9	3.8		4.0	
	Output Enable Time (2OE to 2Y; See Figure5)	C_L = 50pF	2.0		11.3	14.7		15.1	ns
		C_L = 50pF	4.5		3.2	4.2		4.4	
		C_L = 50pF	6.0		2.8	3.7		3.9	
t_{PLZ}, t_{PHZ}	Output Enable Time (1$\overline{OE}$ to 1Y; See Figure4)	C_L = 50pF	2.0		10.3	13.4		13.8	ns
		C_L = 50pF	4.5		2.9	3.8		4.0	
		C_L = 50pF	6.0		2.7	3.5		3.7	
	Output Enable Time (2OE to 2Y; See Figure5)	C_L = 50pF	2.0		10.2	13.3		13.7	ns
		C_L = 50pF	4.5		2.8	3.7		3.9	
		C_L = 50pF	6.0		2.6	3.4		3.6	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 6V, V_I = 0V or V_{CC}	5	pF
C_{PD}	Power Dissipation Capacitance [(5)]	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

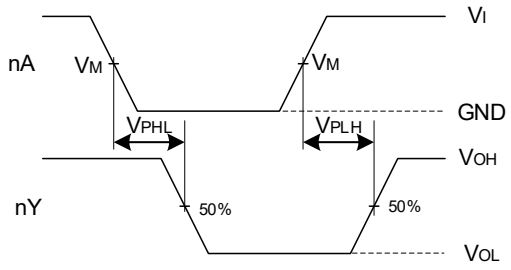
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of outputs.

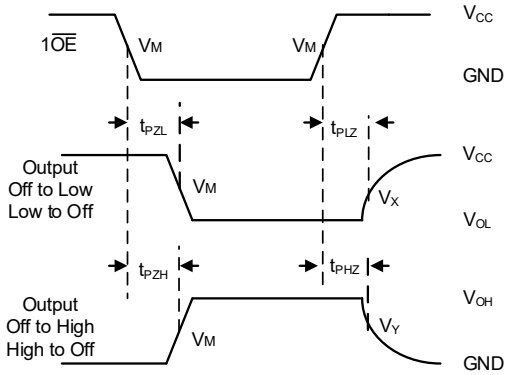
Test Waveform



Measurement points are given in Table1.

V_{OL} and V_{OH} is typical output voltage levels that occur with the output load.

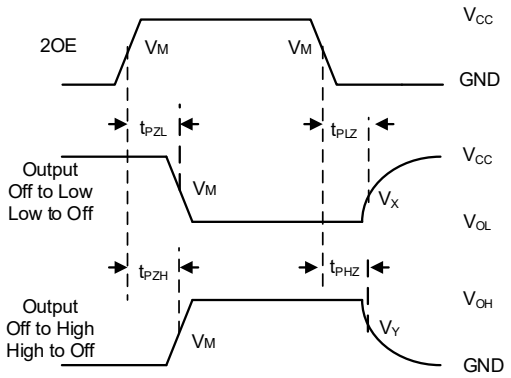
Figure3. Input xA to Output xY Propagation Delay Times



Measurement points are given in Table2.

V_{OL} and V_{OH} is typical output voltage levels that occur with the output load.

Figure4. Enable and Disable Times for Input $1\overline{OE}$



Measurement points are given in Table2.

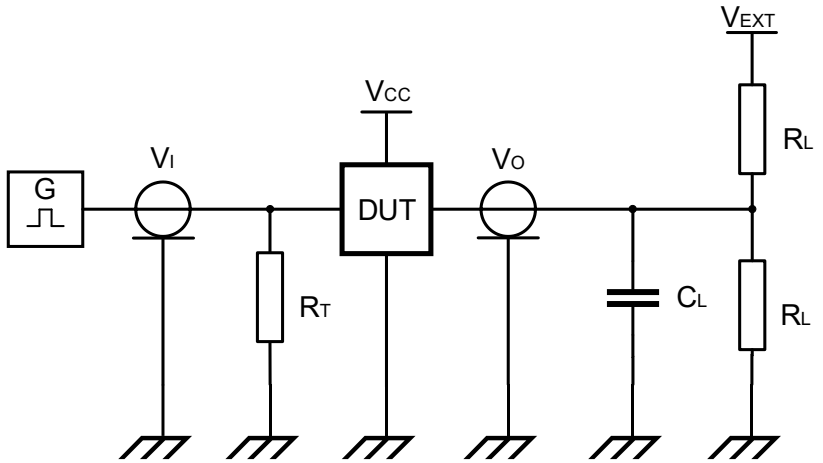
V_{OL} and V_{OH} is typical output voltage levels that occur with the output load.

Figure5. Enable and Disable Times for 2OE

Table1. Measurement Points

Supply Voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
2V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3V	V_{OH} - 0.3V
4.5V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3V	V_{OH} - 0.3V
5V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3V	V_{OH} - 0.3V
6V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3V	V_{OH} - 0.3V

Test Circuit



Measurement points are given in Table 2.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

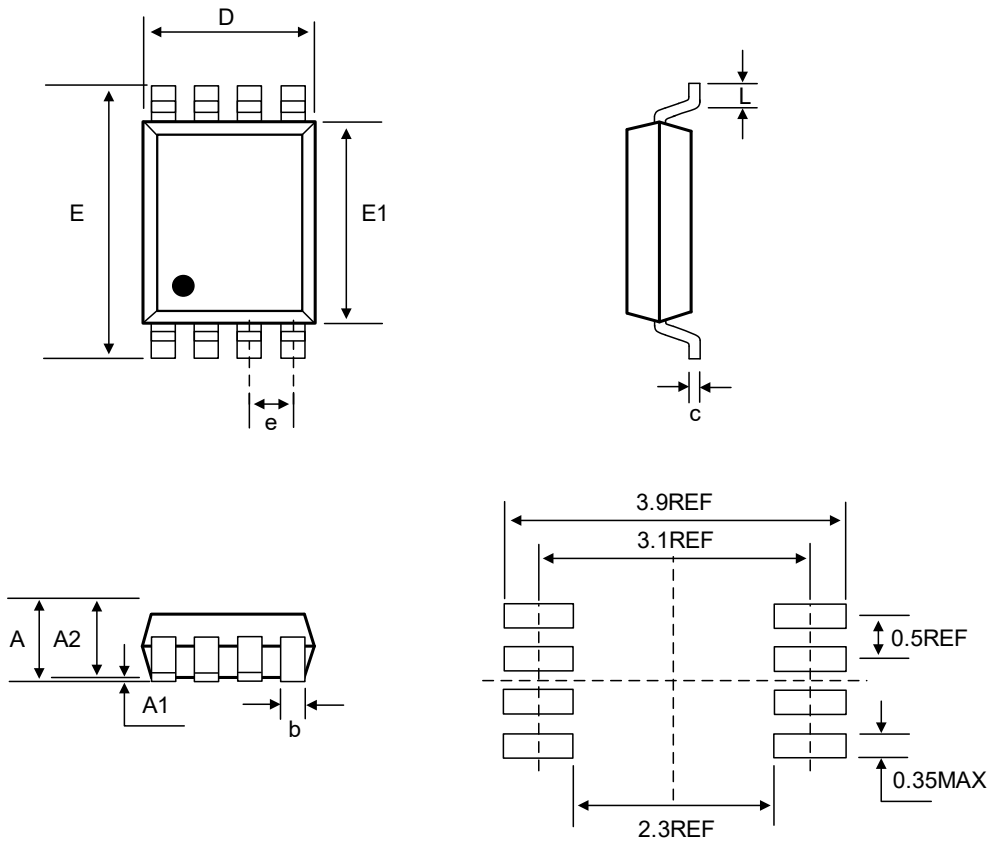
Figure6. Test Circuit for Measuring Switching Times

Table2. Test Data

Supply Voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2V	V_{CC}	3.0ns	50pF	1kΩ	OPEN	GND	V_{CC}
4.5V	V_{CC}	3.0ns	50pF	1kΩ	OPEN	GND	V_{CC}
5V	V_{CC}	3.0ns	15pF	1kΩ	OPEN	GND	V_{CC}
6V	V_{CC}	3.0ns	50pF	1kΩ	OPEN	GND	V_{CC}

Package Dimension

VSSOP8 (2.0mm × 2.3mm)



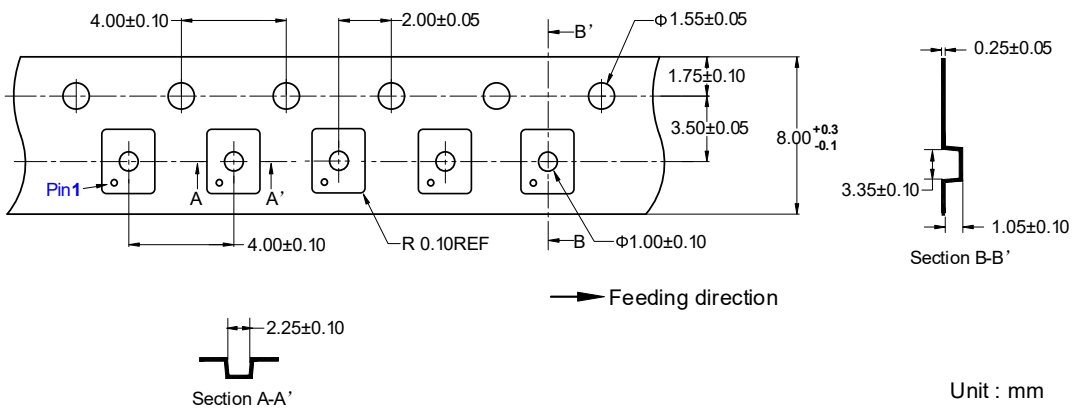
COMMON DIMENSIONS

(Unit: mm)

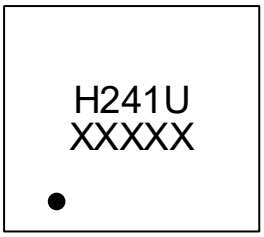
SYMBOL	MIN	NOM	MAX
A	-	-	0.90
A1	0.00	-	0.10
A2	0.65	0.75	0.80
b	0.17	-	0.27
c	0.08	-	0.20
D	1.90	2.00	2.10
E	3.00	3.10	3.20
E1	2.20	2.30	2.40
e	0.50BSC		
L	0.20	-	0.35

Tape Information

VSSOP8 (2.0mm × 2.3mm)



Marking Information



ET74HC2G241U

H241U = Part Number

XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-11-17	Official Version	Xu tao	Yang xiaoxu	Liu jiaying