

Quadruple 2-Input XOR Gates

General Description

This device contains four independent 2-input XOR gates. Each gate performs the Boolean function $Y = A \oplus B$ in positive logic.

Features

- Designed for 2V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- $\pm 8\text{mA}$ Balanced Output Sink and Source Capability
- Buffered Inputs: CMOS Level
- Supports Fan-Out Up to 10 LSTTL Loads
- Significant Power Reduction Compared to LSTTL Logic ICs
- ESD Protection Complies with JESD22 Standard
 - HBM: $\pm 2000\text{V}$ Pass (JEDEC JS-001)
 - CDM: $\pm 1000\text{V}$ Pass (JEDEC JS-002)
- Latch-up Performance Exceeds $\pm 200\text{mA}$ per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74AHCT86M	SOP14 (3.9mm × 8.65mm)	Tape and Reel, 4K/Reel	3
ET74AHCT86V	TSSOP14 (4.4mm × 5.0mm)	Tape and Reel, 4K/Reel	3

Applications

- Detect Phase Differences In Input Signals
- Create a Select-able Inverter / Buffer

Pin Configuration

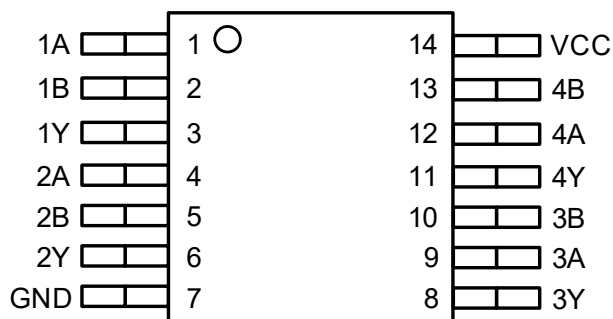


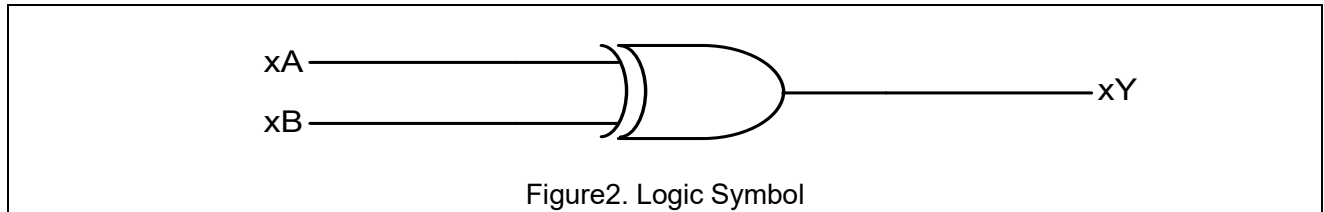
Figure1. Pin Configuration

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Pin Functions

Pin		I/O	Description
Name	No.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
VCC	14	—	Positive Supply

Block Diagram



Functional Table

Input		Output
xA	xB	xY
L	L	L
L	H	H
H	L	H
H	H	L

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Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (V _{CC} Pin)	-0.5 to 6.5	V
V _I	DC Input Voltage ⁽¹⁾	-0.5 ≤ V _I ≤ 6.5	V
V _O	DC Output Voltage Output in Higher or Low State	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current, V _I < GND	-20	mA
I _{OK}	DC Output Diode Current, V _O < GND, V _O > V _{CC}	±20	mA
I _O	DC Output Sink Current	±25	mA
I _{CC}	DC Supply Current Per Supply Pin	50	mA
I _{GND}	DC Ground Current Per Supply Pin	-50	mA
T _{STG}	Storage Temperature Range	-65 to 150	°C
T _L	Lead Temperature, Soldering 10 Seconds	260	°C
T _J	Max Junction Temperature	150	°C
V _{ESD}	ESD Classification	Human Body Model ⁽²⁾	V
		Charged Device Model ⁽³⁾	
I _{LU}	Max Latch Up Current Above V _{CC} and GND at 125°C ⁽⁴⁾	±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Thermal Characteristics

Symbol	Ratings	Package		Unit
		SOP14	TSSOP14	
R _{θJA}	Thermal Characteristics, Thermal Resistance, Junction-to-Air	90	125	°C/W

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	2	5.5	V
V _I	Input Voltage	0	V _{CC}	V
V _O	Output Voltage	0	V _{CC}	V
T _A	Operating Free Air Temperature	-40	125	°C

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Electrical Characteristics

DC Electrical Characteristics

Over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

Symbol	Parameter	Condition	$V_{CC}(V)$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0	1.5			1.5		V
			3.0	2.1			2.1		
			5.5	3.85			3.85		
V_{IL}	Low-Level Input Voltage		2.0			0.5		0.5	V
			3.0			0.9		0.9	
			5.5			1.65		1.65	
V_{OH}	High-Level Output Voltage	$I_{OH} = -50\mu\text{A}$	2~5.5	$V_{CC} - 0.1$	V_{CC}		$V_{CC} - 0.1$		V
		$I_{OH} = -4\text{mA}$	3	2.58			2.4		
		$I_{OH} = -8\text{mA}$	4.5	3.54			3.7		
V_{OL}	Low-Level Output Voltage	$I_{OL} = 50\mu\text{A}$	2~5.5			0.1		0.1	V
		$I_{OL} = 4\text{mA}$	3			0.36		0.55	
		$I_{OL} = 8\text{mA}$	4.5			0.36		0.55	
I_I	Input Leakage Current	$V_I = 5.5\text{V}$ or GND	0~5.5			0.1		2.0	μA
I_{OFF}	Power Off Leakage Current	$V_I = 5.5\text{V}$ or $V_O = 5.5\text{V}$	0			1		10	μA
I_{CC}	Quiescent Supply Current	$V_I = 5.5\text{V}$ or GND	5.5			1		40	μA

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Switching Characteristics

$t_r = t_f = 3\text{ns}$;

Over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

Symbol	Parameter	Condition	$V_{CC}(\text{V})$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure3 and 4)	$C_L = 15\text{pF}$	2~3.6		10	18	1	30	ns
		$C_L = 50\text{pF}$	2~3.6		12	23	1	35	
		$C_L = 15\text{pF}$	4.5~5.5		6.4	8.4	1	9.9	
		$C_L = 50\text{pF}$	4.5~5.5		7.9	10.4	1	12.4	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5\text{V}$, $V_I = 0\text{V}$ or V_{CC}	5	pF
C_{PD}	Power Dissipation Capacitance ⁽⁵⁾	10MHz, $V_{CC} = 5\text{V}$, $V_I = 0\text{V}$ or V_{CC}	12	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

AC Test Circuit

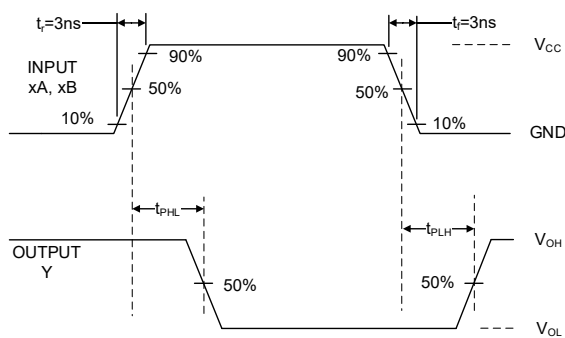


Figure3. Switching Waveform

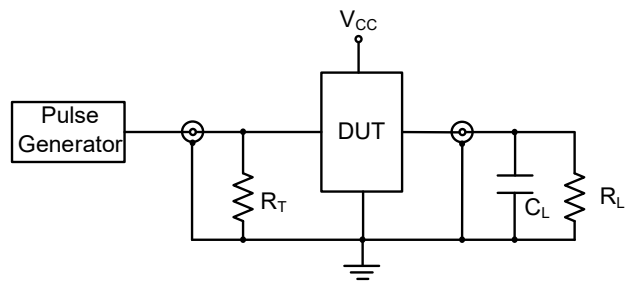
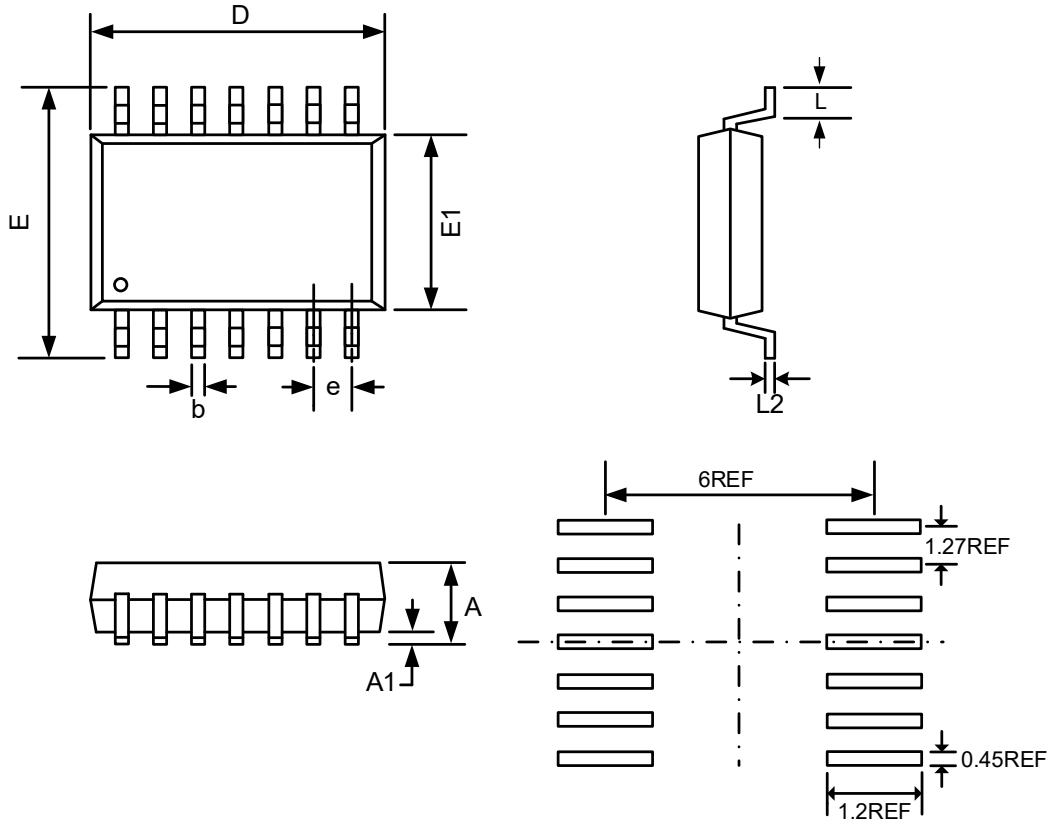


Figure4. Test Circuit

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Package Dimension

SOP14 (3.9mm × 8.65mm)



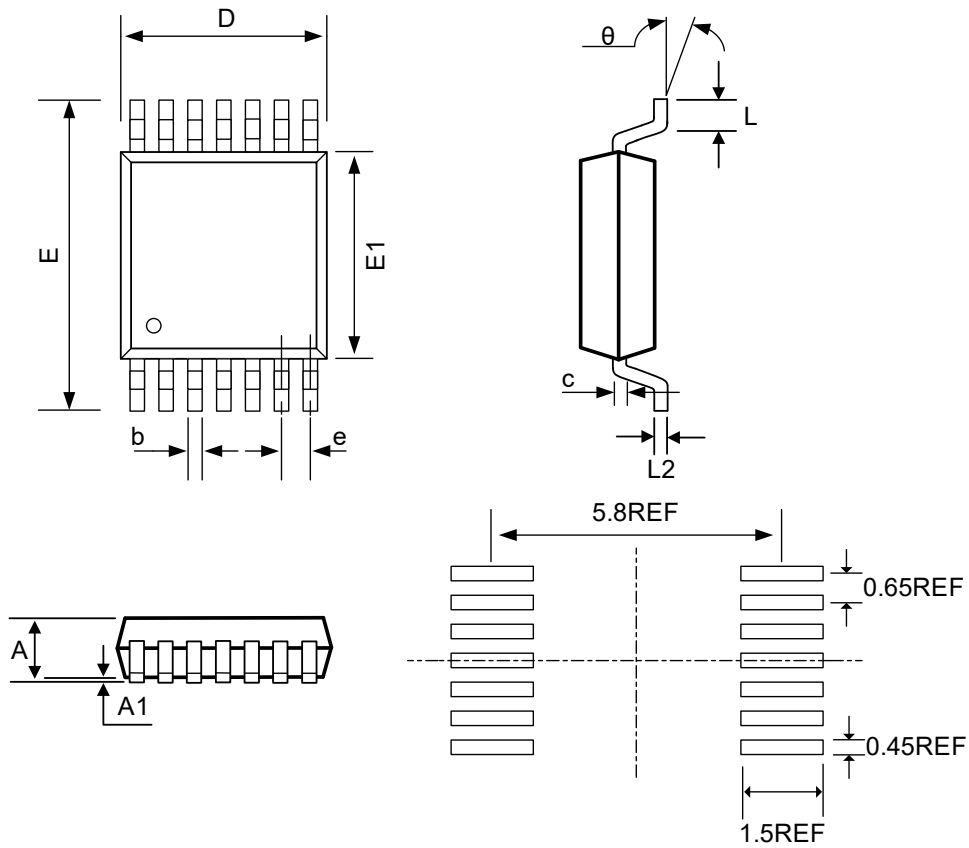
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	MAX
A	--	1.75
A1	0.10	0.25
b	0.36	0.51
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.22	1.32
L	0.45	0.75
L2	0.25 BSC	

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TSSOP14 (4.4mm × 5.0mm)



COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	MAX
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 REF	
D	4.90	5.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.50	0.72
L2	0.25 REF	
θ	0°	8°

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Marking Information

HC86M

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ET74AHC86M

HC86M = Part Number

HC86V

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ET74AHC86V

HC86V = Part Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-12-02	Official Version	Wang anran	Yang xiaoxu	Liu jiaying
1.1	2026-05-15	Update Format, Add Tape and Marking	Xu tao	Yang xiaoxu	Liu jiaying