

Dual Buffer Driver With 3-State Outputs

General Description

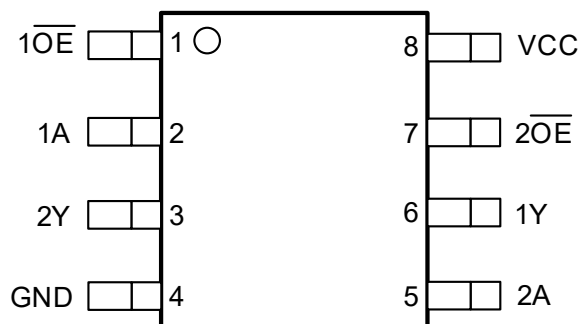
The ET74AHC2G240 is a dual buffer driver with 3-state outputs operating from a 2.0V to 5.5V supply. This device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive.

Features

- Designed for 2.0V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- $\pm 8\text{mA}$ Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- ESD Protection Complies with JESD22 Standard
 - HBM: $\pm 2000\text{V}$ Pass (JEDEC JS-001)
 - CDM: $\pm 1000\text{V}$ Pass (JEDEC JS-002)
- Latch-up Performance Exceeds $\pm 100\text{mA}$ per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74AHC2G240U	VSSOP8 (2.0mm × 2.3mm)	Tape and Reel, 3K/Reel	3

Pin Configuration



VSSOP8

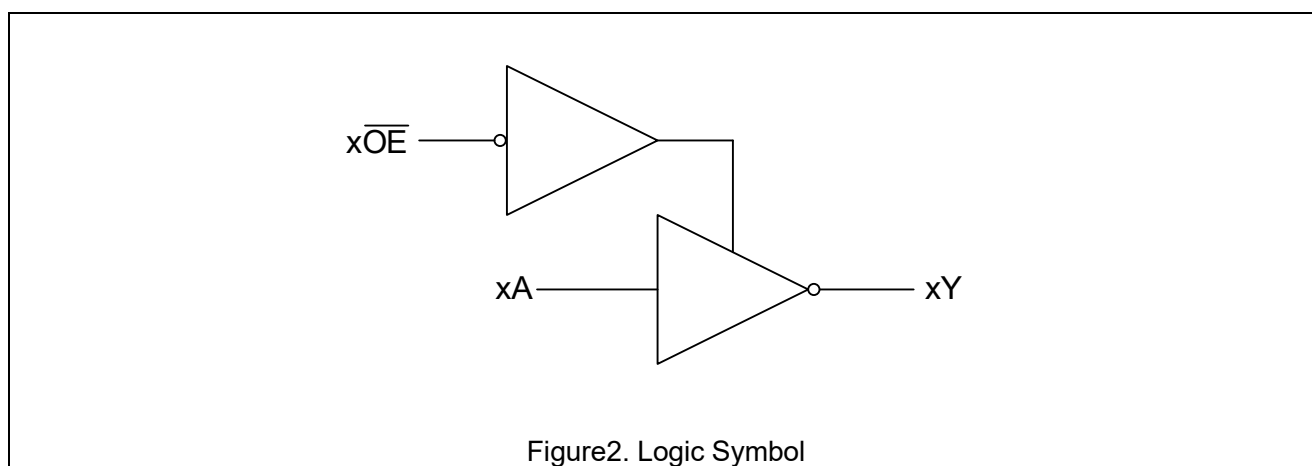
Figure1. Pin Configuration

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Pin Function

Pin No.	Pin Name	Function
1	$\overline{1OE}$	Channel 1, Enable Input
2	1A	Channel 1, Input A
3	2Y	Channel 2, Output Y
4	GND	Ground
5	2A	Channel 2, Input A
6	1Y	Channel 1, Output Y
7	$\overline{2OE}$	Channel 2, Enable Input
8	VCC	Supply Voltage

Block Diagram



Functional Table

Input		Output
$\overline{xOE}$	xA	xY
L	L	H
L	H	L
H	L	Z
H	H	Z

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Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 7.0	V
I _{IK}	DC Input Diode Current, V _I < GND		-20	mA
V _I	DC Input Voltage ⁽¹⁾		-0.5 ≤ V _I ≤ 7.0	V
I _{OK}	DC Output Diode Current, V _O < GND		±20	mA
V _O	DC Output Voltage Output in Higher or Low State		-0.5 to V _{CC} + 0.5	V
I _O	DC Output Sink Current, V _O = 0V to V _{CC}		±25	mA
I _{CC}	DC Supply Current per Supply Pin		50	mA
I _{GND}	DC Ground Current per Supply Pin		-50	mA
T _J	Max Junction Temperature		150	°C
T _{STG}	Storage Temperature Range		-65 to 150	°C
V _{ESD}	ESD Classification	Human Body Model ⁽²⁾	±2000	V
		Charged Device Model ⁽³⁾	±1000	
I _{LU}	Max Latch Up Current Above V _{CC} and GND at 125°C ⁽⁴⁾		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage Operating		2.0	5.5	V
V _I	DC Input Voltage		0	V _{CC}	V
V _O	DC Output Voltage (High or Low State)		0	V _{CC}	V
T _A	Operating Temperature Range		-40	125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 3.3V ± 0.3V		100	ns/V
		V _{CC} = 5.0V ± 0.5V		20	

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Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2	1.5			1.5		V
			3	2.1			2.1		
			5.5	3.85			3.85		
V _{IL}	Low-Level Input Voltage		2			0.5		0.5	V
			3			0.9		0.9	
			5.5			1.65		1.65	
V _{OH}	High-Level Output Voltage	I _{OH} = -50uA	2	1.9	2		1.9		V
		I _{OH} = -50uA	3	2.9	3		2.9		
		I _{OH} = -50uA	4.5	4.4	4.5		4.4		
		I _{OH} = -4mA	3	2.58			2.4		
		I _{OH} = -8mA	4.5	3.94			3.7		
V _{OL}	Low-Level Output Voltage	I _{OL} = 50uA	2		0	0.1		0.1	V
		I _{OL} = 50uA	3		0	0.1		0.1	
		I _{OL} = 50uA	4.5		0	0.1		0.1	
		I _{OL} = 4mA	3			0.36		0.55	
		I _{OL} = 8mA	4.5			0.36		0.55	
I _I	Input Leakage Current	V _I = 5.5V or GND	5.5			±0.1		±2	uA
I _{oz}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = 5.5V or GND	5.5			±0.25		±10	uA
I _{CC}	Quiescent Supply Current	V _I = 5.5V or GND	5.5			1		10	uA

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AC Electrical Characteristics

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t _{PHL} , t _{PLH}	Propagation Delay (x $\overline{A}$ to xY; See Figure3)	C _L = 15pF	3.0~3.6		3.1	4.0	1.0	4.2	ns
		C _L = 50pF	3.0~3.6		3.8	4.9	1.0	5.1	
		C _L = 15pF	4.5~5.5		2.4	3.1	1.0	3.3	
		C _L = 50pF	4.5~5.5		2.9	3.8	1.0	4.0	
t _{PZL} , t _{PZH}	Output Enable Time (x $\overline{OE}$ to xY; See Figure4)	C _L = 15pF	3.0~3.6		3.3	4.3	1.0	4.5	ns
		C _L = 50pF	3.0~3.6		4.1	5.3	1.0	5.5	
		C _L = 15pF	4.5~5.5		2.7	3.5	1.0	3.7	
		C _L = 50pF	4.5~5.5		3.2	4.2	1.0	4.4	
t _{PLZ} , t _{PHZ}	Output Disable Time (x $\overline{OE}$ to xY; See Figure4)	C _L = 15pF	3.0~3.6		3.8	4.9	1.0	5.1	ns
		C _L = 50pF	3.0~3.6		4.3	5.6	1.0	5.8	
		C _L = 15pF	4.5~5.5		2.5	3.3	1.0	3.5	
		C _L = 50pF	4.5~5.5		2.8	3.6	1.0	3.8	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5V, V _I = 0V or V _{CC}	5	pF
C _{PD}	Power Dissipation Capacitance ⁽⁵⁾	10MHz, V _{CC} = 3.3V, V _I = 0V or V _{CC}	25	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

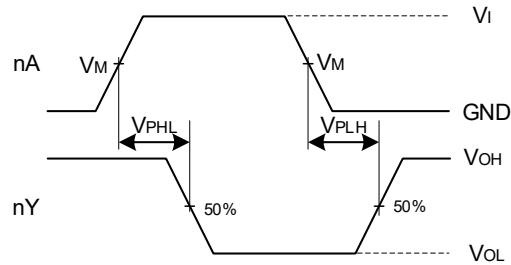
V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of outputs.

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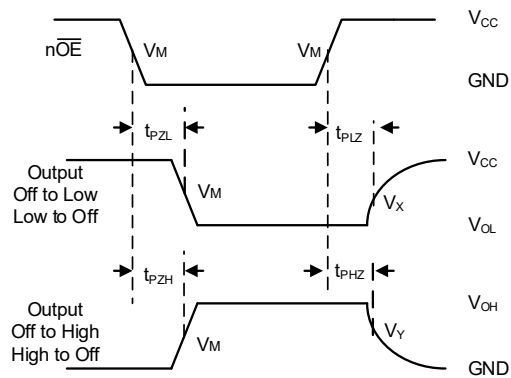
Test Waveform



Measurement points are given in [Table1](#).

V_{OL} and V_{OH} is typical output voltage levels that occur with the output load.

Figure3. Input xA to Output xY Propagation Delay Times



Measurement points are given in [Table1](#).

V_{OL} and V_{OH} is typical output voltage levels that occur with the output load.

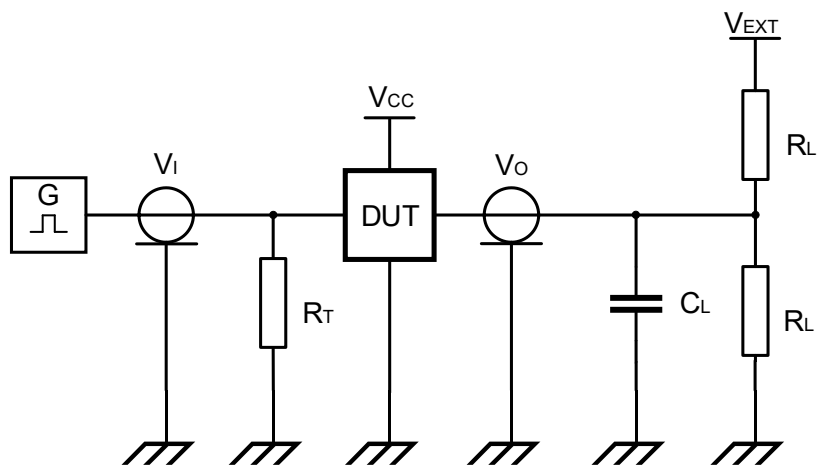
Figure4. 3-state Output Enable and Disable Times

Table1. Measurement Points

Supply Voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
3.0V to 3.6V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3V$	$V_{OH} - 0.3V$
4.5V to 5.5V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3V$	$V_{OH} - 0.3V$

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Test Circuit



Measurement points are given in [Table 2](#).

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Figure5. Test Circuit for Measuring Switching Times

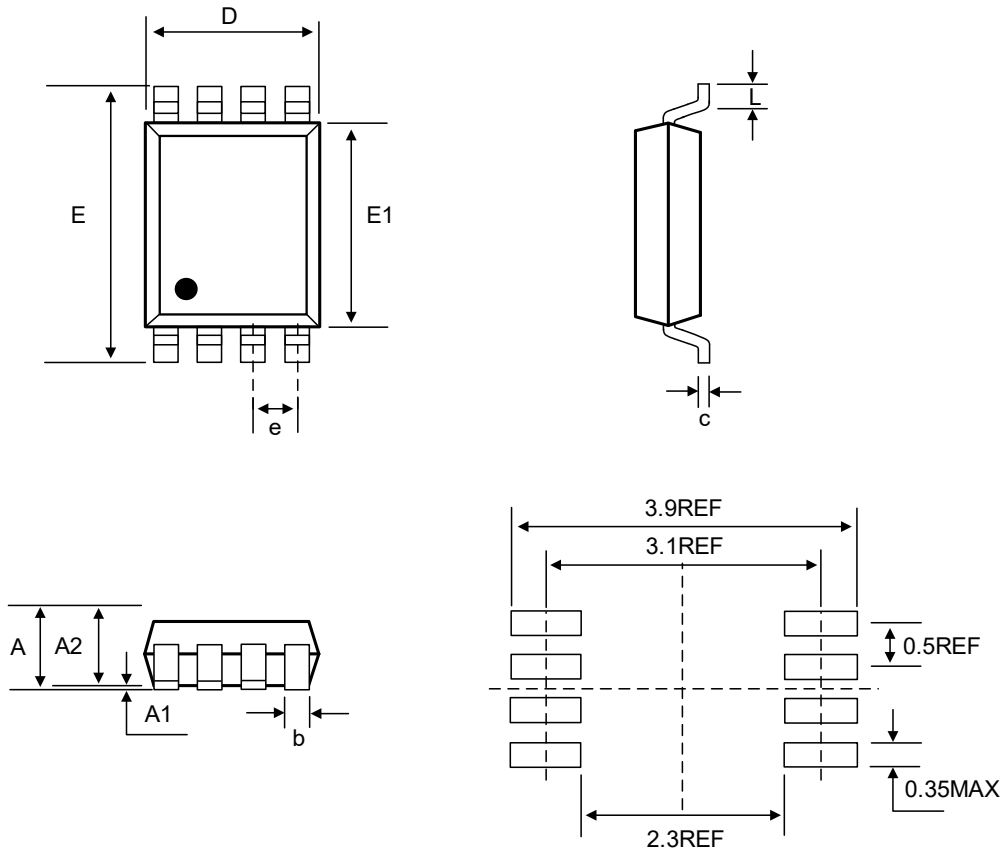
Table2. Test Data

Supply Voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0V to 3.6V	V_{CC}	3.0ns	15pF, 50pF	1k Ω	OPEN	GND	V_{CC}
4.5V to 5.5V	V_{CC}	3.0ns	15pF, 50pF	1k Ω	OPEN	GND	V_{CC}

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Package Dimension

VSSOP8 (2.0mm × 2.3mm)



COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	0.90
A1	0.00	-	0.10
A2	0.65	0.75	0.80
b	0.17	-	0.27
c	0.08	-	0.20
D	1.90	2.00	2.10
E	3.00	3.10	3.20
E1	2.20	2.30	2.40
e	0.50BSC		
L	0.20	-	0.35

