8-Bit Parallel-Out Serial Shift Registers

General Description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear $\overline{CLR}$ input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop.

Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

Features

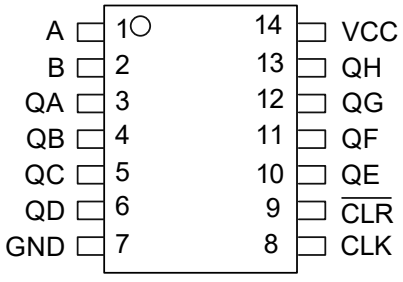
- Designed for 2V to 6V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 6V
- ±5.2mA Balanced Output Sink and Source Capability
- AND-Gated (Enable/Disable) Serial Inputs
- Direct Clear
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±2000V Pass (JEDEC JS-001)
  -- CDM: ±2000V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA per JEDEC JESD78F
- Part No. and Package Information

Port No.	Package	MSL
74HC164M	SOP14 (3.90mm × 8.65mm)	3
74HC164V	TSSOP14 (4.40mm × 5.50mm)	3

Applications

- Memory Chip Select Decoding
- Data Transmission System

Pin Configuration



SOP14/TSSOP14

Figure1. Pin Configuration

Pin Function

Pin Number	Pin Name	Function
1	A	Serial Data Input
2	B	Serial Data Input
3	QA	Data Output
4	QB	Data Output
5	QC	Data Output
6	QD	Data Output
7	GND	Ground
8	CLK	Clock Pulse - Positive Edge Triggered
9	$\overline{CLR}$	Master Reset - Asynchronous
10	QE	Data Output
11	QF	Data Output
12	QG	Data Output
13	QH	Data Output
14	VCC	Supply Voltage

Function Table

Input Pin				Output Pin			
$\overline{CLR}$	**CLK**	**A**	**B**	**QA**	**QB**	**…**	**QH**
L	X	X	X	L	L		L
H	L	X	X	QA0	QB0		QH0
H	↑	H	H	H	QAn		QGn
H	↑	L	X	L	QAn		QGn
H	↑	X	L	L	QAn		QGn

QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.

QAn, QGn = the level of QA or QG before the most recent ↑ transition of CLK: indicates a 1-bit shift.

Block Diagram

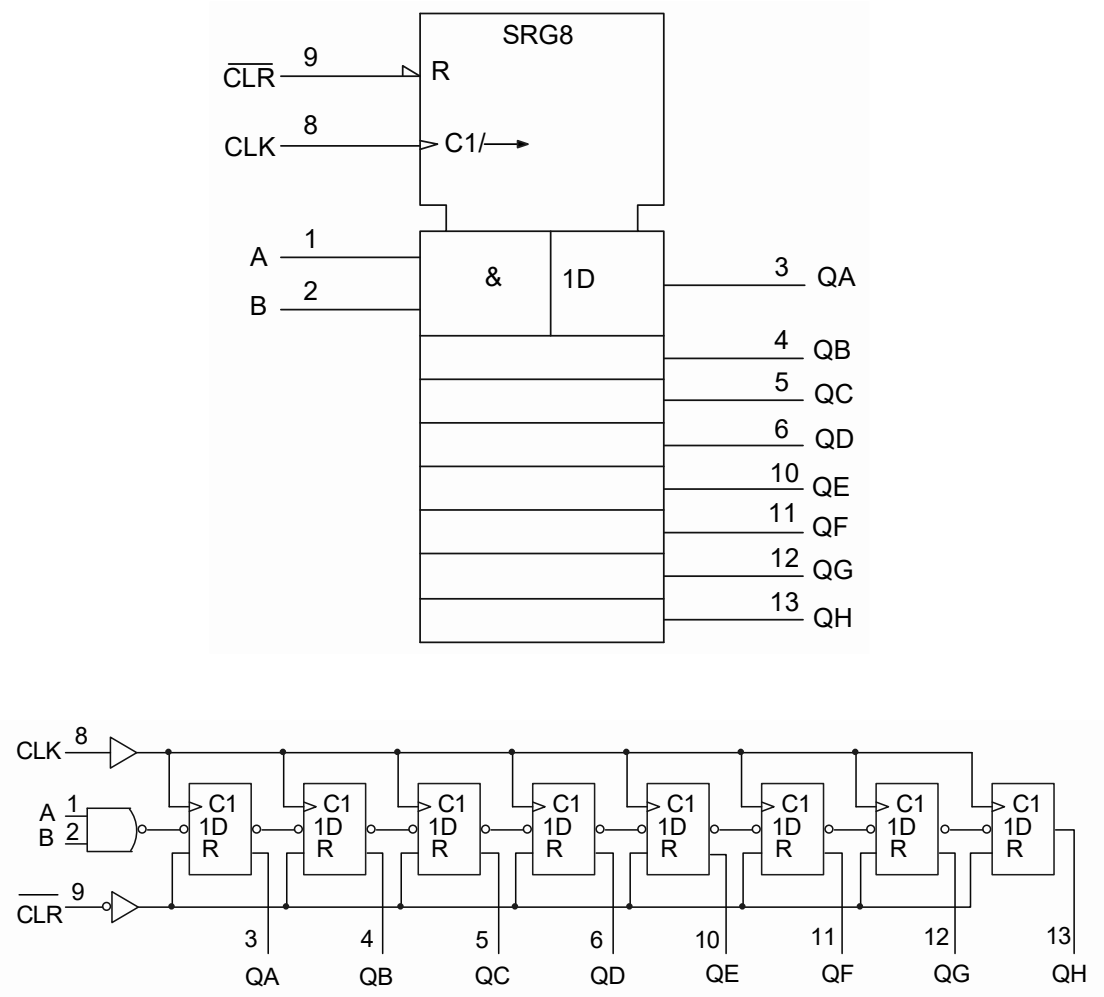


Figure2. Logic Symbol

Functions Description

Typical Clear, Shift, and Clear Sequence

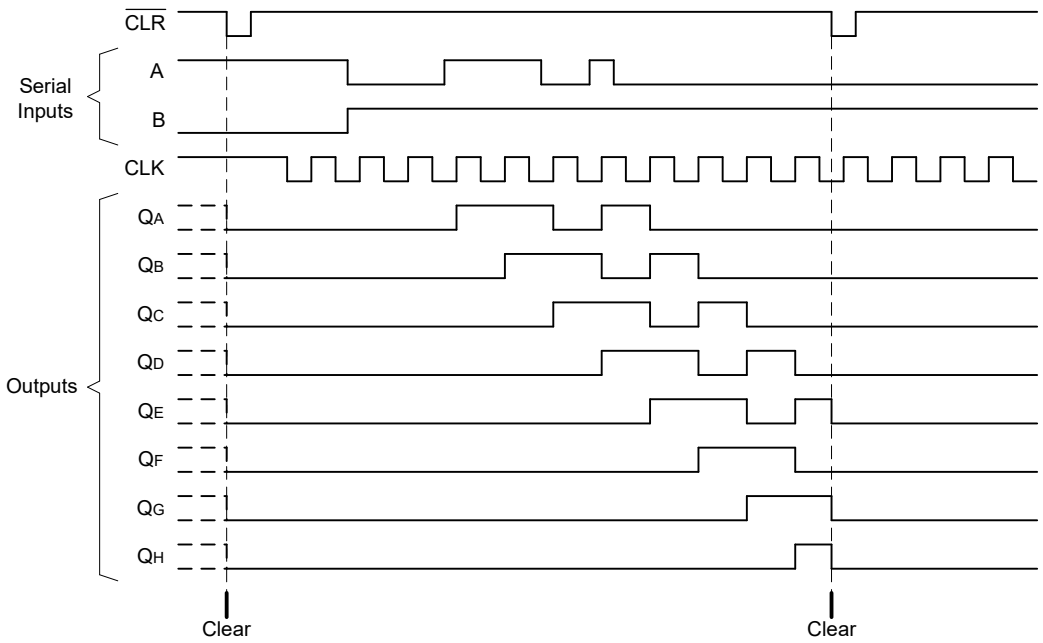


Figure3. Typical Sequence

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage(VCC Pin)		-0.5 to 6.5	V
V_I	DC Input Voltage (1)		-0.5 to 6.5	V
V_O	DC Output Voltage		-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current, V_I < GND		±20	mA
I_{OK}	DC Output Diode Current, V_O < GND		±20	mA
I_O	DC Output Sink Current, V_O = 0V to V_{CC}		±25	mA
I_{CC}	DC Supply Current per Supply Pin		50	mA
I_{GND}	DC Ground Current per Supply Pin		-50	mA
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to 150	°C
V_{ESD}	ESD Classification	Human Body Model (2)	±2000	V
		Charged Device Model (3)	±2000	
I_{LU}	Max Latch Up Current Above V_{CC} and GND (4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended operating conditions

Symbol	Parameter	Condition	Rating			Unit
			Min	Typ	Max	
V_{CC}	Supply Voltage		2	5	6	V
V_{IH}	High-Level Input Voltage	V_{CC} = 2V	1.5			V
		V_{CC} = 4.5V	3.15			
		V_{CC} = 6V	4.2			
V_{IL}	Low-Level Input Voltage	V_{CC} = 2V	0		0.5	V
		V_{CC} = 4.5V	0		1.35	
		V_{CC} = 6V	0		1.8	
V_I	Input Voltage		0		V_{CC}	V
V_O	Output Voltage		0		V_{CC}	V
t_t	Input Transition (Rise And Fall) Time	V_{CC} = 2V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6V	0		400	
T_A	Operating Free-Air Temperature		-40		85	°C

If this device is used in the threshold region (from V_{IL_MAX} = 0.5V to V_{IH_MIN} = 1.5V), there is a potential to go into the wrong state from induced grounding, causing double clocking.

Operating with the inputs at tt = 1000ns and V_{CC} = 2V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

Electrical Characteristics

Symbol	Test Condition		V_{CC} (V)	T_A = 25°C			T_A = -40°C to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{OH}	V_I = V_{IH} or V_{OH}	I_{OH} = 20μA	2	1.9	1.998		1.9		V
			4.5	4.4	4.499		4.4		
			6	5.9	5.999		5.9		
		I_{OH} = -4mA	4.5	3.98	4.3		3.84		
		I_{OH} = -5.2mA	6	5.48	5.8		5.34		
V_{OL}	V_I = V_{IH} or V_{OH}	I_{OL} = 20μA	2		0.002	0.1		0.1	V
			4.5		0.001	0.1		0.1	
			6		0.001	0.1		0.1	
		I_{OL} = 4mA	4.5		0.17	0.26		0.33	
		I_{OL} = 5.2mA	6		0.15	0.26		0.33	
I_I	V_I = V_{CC} or 0V		6		±0.1	±100		±1000	nA
I_{CC}	V_I = V_{CC} or 0V, I_O = 0mA		6			8		80	μA

Time Characteristics

Symbol	Characteristic		V_{CC} (V)	T_A = 25°C			T_A = -40°C to 85°C		Unit
				Min	Typ	Max	Min	Max	
F_{CLOCK}	Clock Frequency		2	0		6	0	5	MHz
			4.5	0		31	0	25	
			6	0		36	0	28	
t_W	Pulse Duration	$\overline{CLR}$ Low	2	100			125		ns
			4.5	20			25		
			6	17			21		
		CLK High or Low	2	80			100		
			4.5	16			20		
			6	14			18		
t_{SU}	Setup Time Before CLK	Data	2	100			125		ns
			4.5	20			25		
			6	17			21		
I_{CC}		$\overline{CLR}$ Inactive	2	100			125		
			4.5	20			25		
			6	17			21		
t_h	Hold Time, Data After CLK		2	5			5		ns
			4.5	5			5		
			6	5			5		

Switching characteristics (C_L = 50pF)

Symbol	From (Input)	To (Output)	V_{CC} (V)	T_A = 25°C			T_A = -40°C to 85°C		Unit
				Min	Typ	Max	Min	Max	
F_{MAX}			2	6	10		5		MHz
			4.5	31	54		25		
			6	36	62		28		
t_{PHL}	$\overline{CLR}$	Any Q	2		140	205		255	ns
			4.5		28	41		51	
			6		24	35		46	
t_{pd}	CLK	Any Q	2		115	175		220	
			4.5		23	35		44	
			6		20	30		38	
t_t			2		38	75		95	ns
			4.5		8	15		19	
			6		6	13		16	

Capacitance characteristics

Symbol	Parameter	Test Conditions	Typ	Unit
C_I	Input Capacitance	V_{CC} = 6V, V_I = V_{CC} or GND	3	pF
C_{pd}	Power Dissipation Capacitance	No Load	135	pF

Parameter Measurement Information

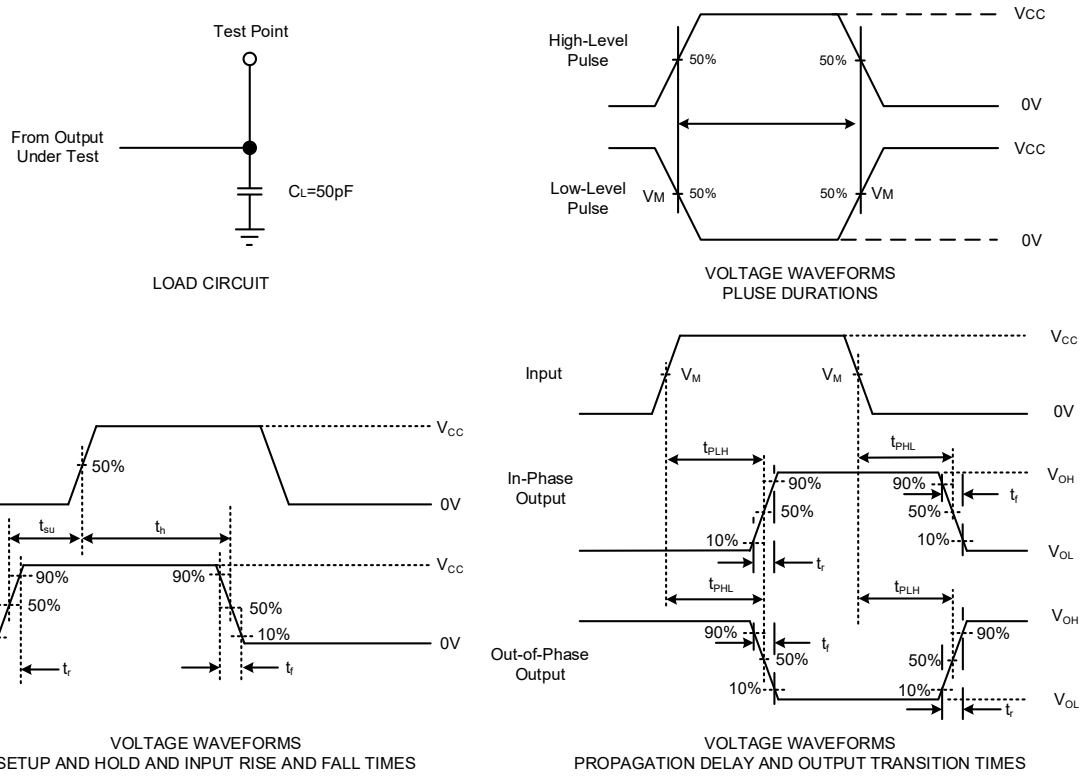
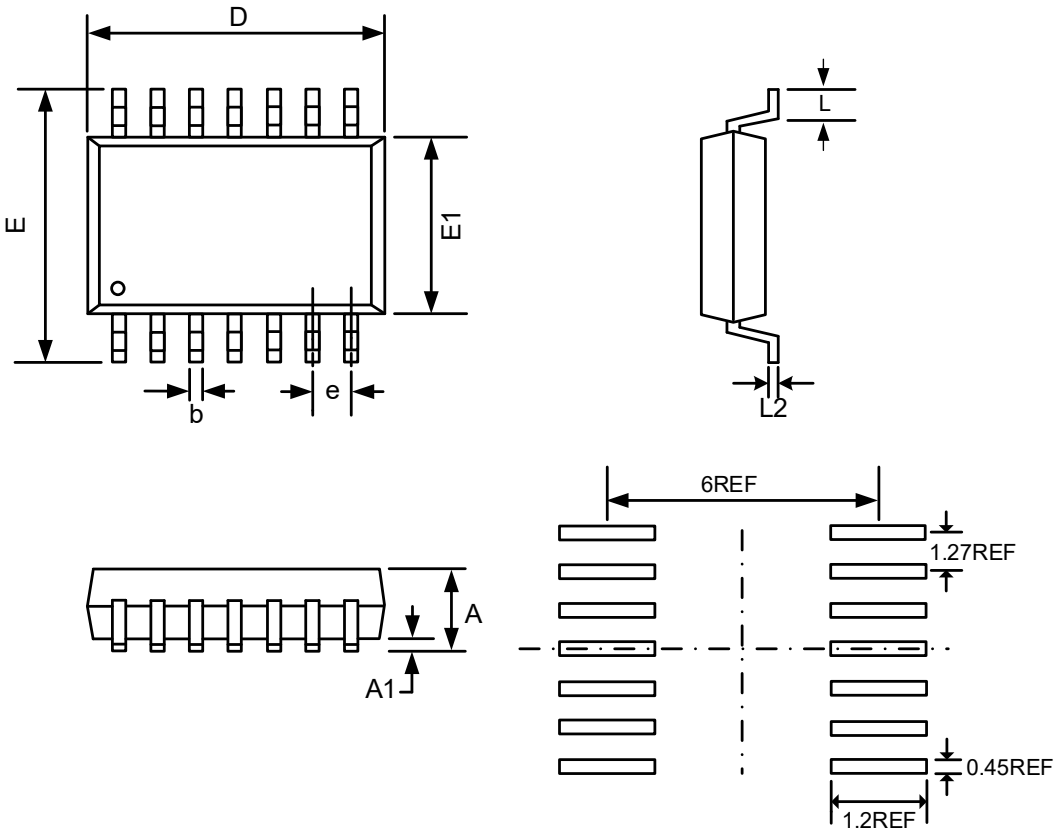


Figure4. Input to output propagation delay times

When using the circuit, in order to strengthen the anti-jamming ability, a capacitor of 100pF should be connected between the $\overline{CLR}$ and VCC or GND.

Package Dimension

SOP14 (3.9mm × 8.65mm)

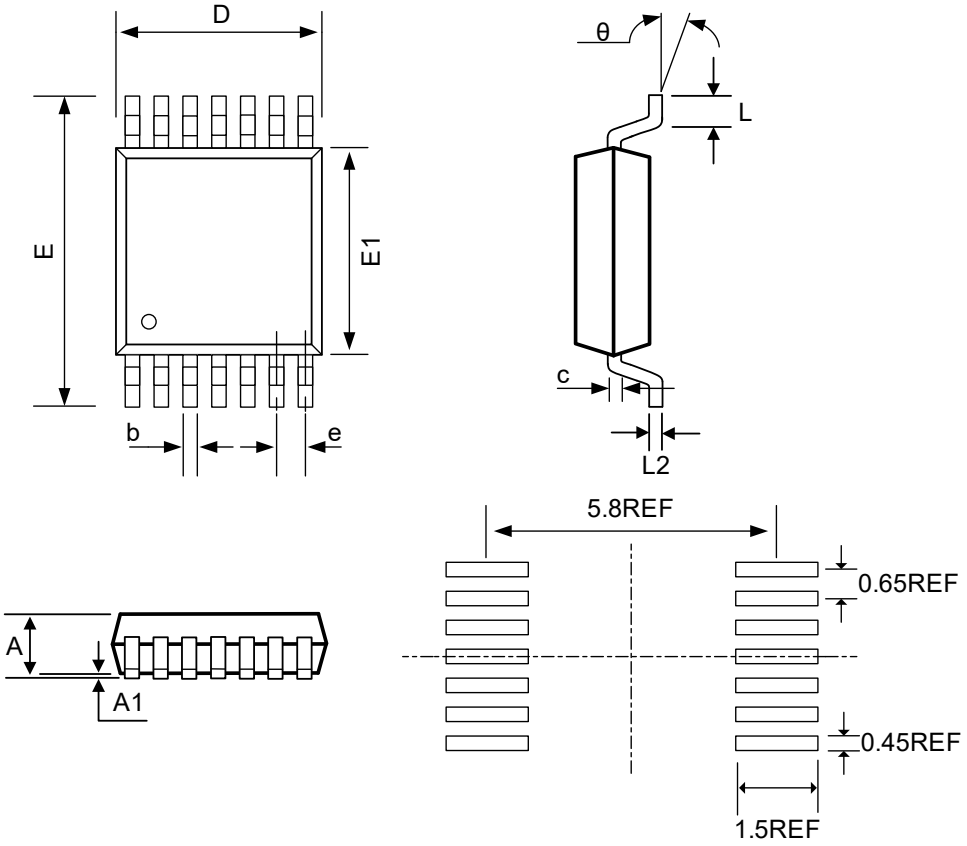


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	MAX
A	--	1.75
A1	0.10	0.25
b	0.36	0.51
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.22	1.32
L	0.45	0.75
L2	0.25 BSC	

TSSOP14 (4.4mm × 5.0mm)

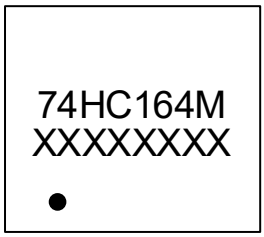


COMMON DIMENSIONS

(Unit: mm)

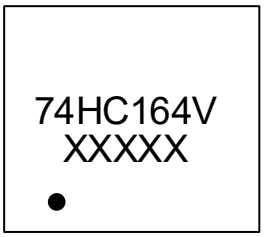
SYMBOL	MIN	MAX
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 REF	
D	4.86	5.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L2	0.25 REF	
θ	0°	8°

Marking Information



74HC164M = Part Number

XXXXXXXX = Tracking Number



74HC164V = Part Number

XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2022-07-19	Original Version	Shi bo	Shi liangjun	Shi bo
1.1	2023-07-24	Update EC Table	Shi bo	Ge hao	Shi bo
1.2	2024-08-12	Update EC Table	Shi bo	Ge hao	Shi bo
1.2.a	2025-11-19	Add Marking	Yang xiaoxu	Ge hao	Liu jiaying
1.3	2025-12-15	Update Format and Package	Xu tao	Yang xiaoxu	Liu jiaying