

1A, High PSRR, Low Dropout LDO

General Description

The ET5A7ADJY1B is a 1A low-dropout linear regulators (LDOs) offering high power-supply ripple rejection (PSRR) and Power Good open collector output. This LDO uses an advanced BiCMOS process to achieve very good electrical performance. It is an ideal choice for noise sensitive Analog RF Front-Ends used in Telecom Equipment.

The ET5A7ADJY1B is available in the DFN8 (3mm x 3mm) package.

Features

- Wide Input Voltage Range: 2.2V ~ 5.5V
- Output Voltage Range: 0.8V ~ 5.0V (adjustable)
- Ground Pin Current: 60 μ A (Typ) at 0.1mA
- Low Dropout: 160mV (Typ) at 1A, $V_{OUT} = 3.3V$
- Built-in Current Limiting and Thermal Shutdown Circuit
- Built-in Under Voltage Lock-out
- With Auto Discharge Function
- Part No. and Package Information

Part No.	Package	MSL
ET5A7ADJY1B	DFN8 (3mm x 3mm)	Level 1

Applications

- Constant-Voltage Power Supply for Battery-Powered Device
- Constant-Voltage Power Supply for Smartphones, Tablets
- Constant-Voltage Power Supply for Cameras, DVRs, STB and Camcorders

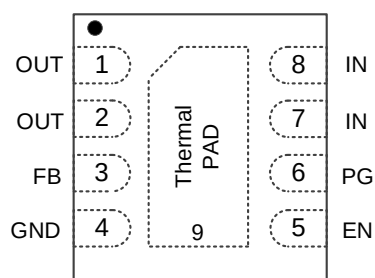
ET5A7ADJY1B

Device information

ET 5A7 ADJ Y1 B

<u>ADJ</u> Output Voltage		<u>Y1</u> Package		<u>B</u>
ADJ	Adjust Output	Y1	DFN8 (3mm x 3mm)	With Auto Discharge Function

Pin Configuration



ET5A7ADJY1

Figure1. Top View

Pin Function

Pin No.	Pin Name	Pin Function
1,2	OUT	The Power Output of The Device.
3	FB	Adjustable Output Feedback Pin.
4	GND	Ground Pin.
5	EN	Enable Input. Driving EN high turns on the regulator. Driving EN low turns off the regulator. This pin must be pulled high by an external resistor connected to IN pin if EN pin is not used.
6	PG	Power Good, Open Collector. Use 10 kΩ to 100 kΩ pull-up resistor connected to output or input voltage.
7,8	IN	Input Voltage Pin. Large bulk capacitance should be placed closely to this pin. A 4.7μF ceramic capacitor is recommended at this pin.
9	Thermal Pad	Thermal Pad. Connect to GND plane for better power dissipation.

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Block Diagram

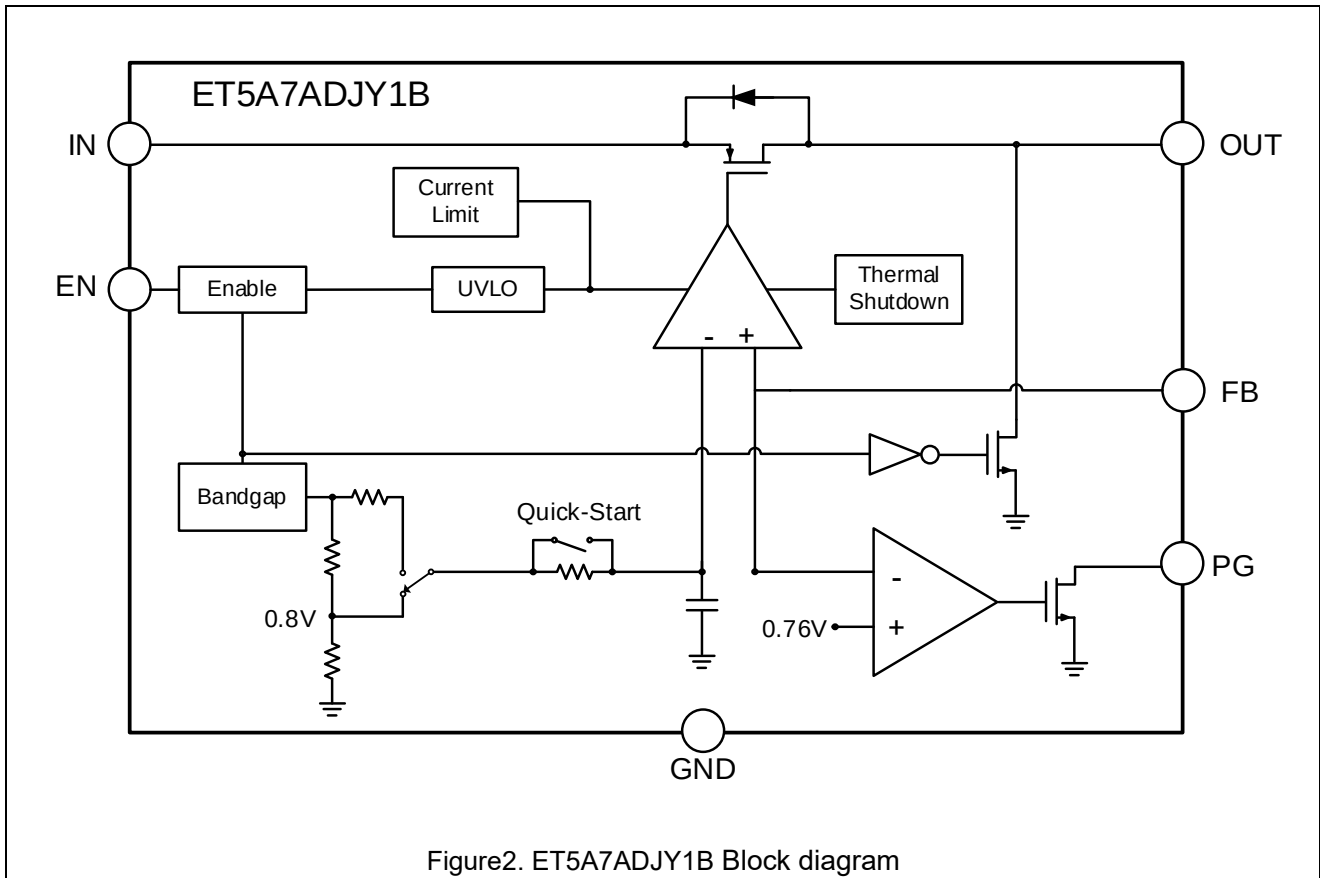


Figure2. ET5A7ADJY1B Block diagram

Functional Description

The ET5A7ADJY1B is the member of new family of high output current and low dropout regulators which delivers low quiescent and ground current consumption, good noise and power supply ripple rejection ratio performance. The ET5A7ADJY1B incorporates EN pin and power good output for simple controlling by MCU or logic. Standard features include current limiting, soft-start feature and thermal protection.

Capacitors Selection

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1 μ F to 1.0 μ F low equivalent series resistance (ESR) capacitor across the input supply near the regulator. The ET5A7ADJY1B is designed to be stable with standard ceramic output capacitors of capacitance values 4.7 μ F up to 10 μ F.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool down. When the junction temperature reduces to approximately +130°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

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Power Dissipation

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C.

Under-Voltage Lock-Out (UVLO)

The ET5A7ADJY1B uses an under-voltage lock-out circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that it typically ignores undershoot transients on the input if they are less than 50µs duration.

Enable Pin Operation

The ET5A7ADJY1B is turned on by setting the EN pin to “H”. The threshold limits are covered in the electrical characteristics table in this datasheet. When the EN pin is not used, connect the EN pin with IN to keep the LDO in operating mode.

Input Power Supply

The input power supply range is from 2.2V to 5.5V. VIN must be larger than (V_{OUT} + V_{DROP}) in application. The input ceramic capacitor must be placed as close as possible to the IN pin, this C_{IN} can help improve the output noise performance of LDO.

Current Limit Protection

When output current of OUT pin is higher than current limit threshold or the OUT pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

Output Voltage Setting

The required output voltage of Adjustable devices can be adjusted from V_{REF} to 5V using two external resistors. Typical application schematics is shown blow.

$$V_{OUT} = V_{REF} * (1 + R1 / R2)$$

Typical value of V_{REF} is 0.8V. It is recommended to keep the total serial resistance of resistors (R1 + R2) no greater than 100kΩ.

The output voltage needs to take into account the error caused by the resistance accuracy.

Power Good Output Connection

The ET5A7ADJY1B has a power-good function that works by toggling the state of the PG output pin. When the output voltage falls below the PG threshold voltage, the PG pin open-drain output engages (low impedance to GND). When the output voltage exceeds the PG threshold voltage by an amount greater than VHYS (PG), the PG pin becomes high-impedance. By connecting a pull-up resistor to an external supply, any downstream device can receive PG as a logic signal. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices.

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Absolute Maximum Ratings

Symbol	Parameters (Items)	Value	Unit
V _{IN}	Input Voltage (IN Pin) ⁽¹⁾	-0.3 to 6.0	V
V _{EN}	Input Voltage (EN Pin)	-0.3 to 6.0	V
V _{FB}	Feedback Voltage (FB Pin)	-0.3 to 6.0	V
V _{PG}	Power Good Voltage (PG Pin)	-0.3 to 6.0	V
V _{OUT}	Output Voltage (OUT Pin)	-0.3 to (V _{IN} +0.3) ≤6.0	V
I _{MAX}	Maximum Load Current	Internally Limited	mA
P _{D_MAX}	Maximum Power Consumption	2000	mW
T _J ⁽²⁾	Operating Junction Temperature	-40 to 150	°C
T _{STG}	Storage Temperature	-55 to 150	°C
T _{SLOD}	Lead Temperature (Soldering, 10 sec)	300	°C
V _{ESD} ⁽³⁾	HBM Capability	±4000	V
	CDM Capability	±1500	V
I _{LU} ⁽³⁾	Latch up Current Maximum Rating	±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: Refer to Electrical Characteristics and Application Information for Safe Operating Area and IN port needs to be powered on before the EN port.

Note2: When T_J > 125°C, there will be a large deviation in voltage accuracy.

Note3: This device series incorporates ESD protection and is tested by the following methods:

HBM tested per JEDEC JS-001.

CDM tested per JEDEC JS-002.

Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameters	Rating	Unit
V _{IN}	Input Voltage	2.2 to 5.5	V
V _{OUT}	Output Voltage	0.8 to 5.0	V
I _{OUT}	Output Current	0 to 1000	mA
T _A	Operating Ambient Temperature	-40 to 85	°C
C _{IN}	Effective Input Ceramic Capacitor Value	0.1 to 1	μF
C _{OUT}	Effective Output Ceramic Capacitor Value	4.7 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

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Electrical Characteristics

(Unless otherwise noted, $V_{IN} = V_{OUT} + 0.5V$ or $2.2V$ (whichever is greater), $V_{EN} = 2.2V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 4.7\mu F$. $T_J = -40^{\circ}C$ to $+85^{\circ}C$, typical values are at $T_A = +25^{\circ}C$)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{IN}^{(4)}$	Input Voltage Range		2.2		5.5	V
V_{UVLO}	Under-voltage Lock-out	V_{IN} Rising, $R_L = 1k\Omega$	1.86	2	2.1	V
V_{UVLO_H}		Hysteresis, V_{IN} Falling, $R_L = 1k\Omega$		75		mV
$V_{OUT}^{(5)}$	V_{OUT} Voltage Accuracy	Output Voltage Range	0.8		5	V
		$V_{OUT} + 0.5V \leq V_{IN} \leq 5.5V$, $V_{IN} \geq 2.2V$, $1mA \leq I_{OUT} \leq 1A$, $T_A = 25^{\circ}C$	-0.3		0.3	%
		$V_{OUT} + 0.5V \leq V_{IN} \leq 5.5V$, $V_{IN} \geq 2.2V$, $1mA \leq I_{OUT} \leq 1A$, $-40^{\circ}C \leq T_J \leq 85^{\circ}C$	-2.5		2.5	%
Reg_{LINE}	Line Regulation	$V_{OUT(NOM)} + 0.5V \leq V_{IN} \leq 5.5V$, $V_{IN} \geq 2.2V$, $I_{OUT} = 1mA$		0.0045	0.05	%/V
Reg_{LOAD}	Load Regulation	$1mA \leq I_{OUT} \leq 1A$, $V_{OUT}=3.3V$		2	10	mV
$V_{DROP}^{(6)}$	Dropout Voltage	$V_{OUT(NOM)} + 0.5V \leq V_{IN} \leq 5.5V$, $V_{IN} \geq 2.2V$, $I_{OUT} = 500mA$		80	120	mV
		$V_{OUT(NOM)} + 0.5V \leq V_{IN} \leq 5.5V$, $V_{IN} \geq 2.2V$, $I_{OUT} = 750mA$		120	180	
		$V_{OUT(NOM)} + 0.5V \leq V_{IN} \leq 5.5V$, $V_{IN} \geq 2.2V$, $I_{OUT} = 1A$		160	240	
I_{LIMIT}	Current Limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$, $V_{IN} \geq 3.3V$		1600	260 0	mA
I_{GND}	Ground Pin Current	$I_{OUT} = 0.1mA$		60	100	μA
		$I_{OUT} = 1A$		300	500	μA
I_{SHDN}	Shutdown Current	$V_{EN} \leq 0.4V$, $V_{IN} \geq 2.2V$, $R_L = 1k\Omega$, $-40^{\circ}C \leq T_J \leq 85^{\circ}C$		0.2	2	μA
I_{FB}	FB Pin Current	$V_{IN} = 5.5V$, $V_{FB} = 0.8V$		0.02	1	μA
$PSRR^{(7)}$	Power Supply Rejection Ratio	$V_{IN} = 4.3V$, $V_{OUT} = 3.3V$, $I_{OUT} = 750mA$	$f = 100Hz$		77	dB
			$f = 1kHz$		63	
			$f = 1MHz$		27	
$e_N^{(7)}$	Output Noise	$V_{IN} = 4.3V$, $V_{OUT} = 3.3V$, $f = 100Hz$ to $100kHz$, $I_{OUT} = 100mA$		$15 \times V_{OUT}$		μV_{RMS}
I_{EN}	Enable Input Current	$V_{IN} = V_{EN} = 5.5V$		0.27	1	μA

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Electrical Characteristics(Continued)

(Unless otherwise noted, $V_{IN} = V_{OUT} + 0.5V$ or $2.2V$ (whichever is greater), $V_{EN} = 2.2V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 4.7\mu F$. $T_J = -40^{\circ}C$ to $+85^{\circ}C$, typical values are at $T_A = +25^{\circ}C$)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{PGUP}^{(7)}$	Power Good Threshold Voltage	Output Voltage Raising		95		%
$V_{PGDW}^{(7)}$		Output Voltage Falling		90		
V_{PGLO}	Power Good Output Voltage Low	$I_{PG} = 1mA$, Open Drain		30	100	mV
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage High	1.2			V
V_{ENL}		EN Input Voltage Low			0.4	
T_{ON}	Turn-On Time	$V_{OUT} = 3.3V$, $R_L = 1k\Omega$, From $EN = HIGH$ to $V_{OUT} = 90\% V_{OUT(MON)}$		350		μs
$T_{TSD}^{(7)}$	Thermal Shutdown Threshold	T_J Rising		160		$^{\circ}C$
$T_{HYS}^{(7)}$	Thermal Shutdown Hysteresis	T_J Falling from Shutdown		30		$^{\circ}C$

Note4: Minimum $V_{IN} = V_{OUT} + V_{DO} \geq 2.2 V$.

Note5: The ET5A7ADJY1B does not include external resistor tolerances and it is not tested at this condition:

$V_{OUT} = 0.8 V$, $4.5V \leq V_{IN} \leq 5.5 V$, and $750 mA \leq I_{OUT} \leq 1 A$, because the power dissipation is greater than the maximum rating of the package.

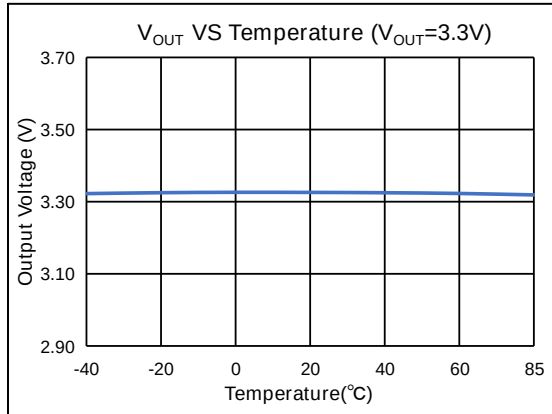
Note6: V_{DROP} is not measured for fixed output voltage devices with $V_{OUT} < 1.7 V$ because minimum $V_{IN} = 2.2 V$. V_{DROP} FT test method: test the V_{OUT} voltage at $V_{set} + V_{DROPMAX}$ with output current.

Note7: Guaranteed by design and characterization. not a FT item.

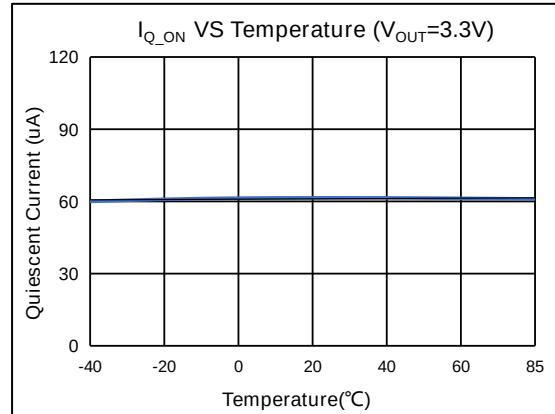
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Typical Characteristics

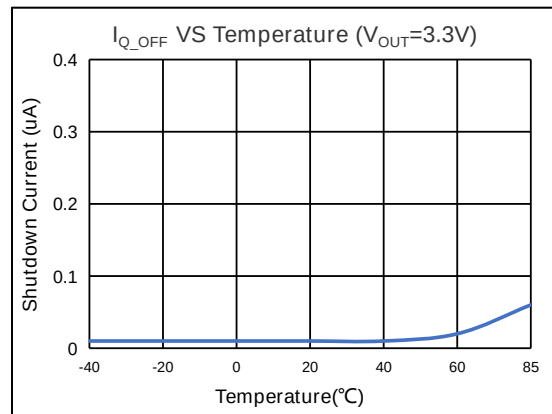
Voltage set 3.3V ($V_{IN} = V_{OUT} + 0.5V$, $V_{EN} = 2.2V$, $I_{OUT} = 1mA$, $R1 = 312.5k\Omega$, $R2 = 100k\Omega$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 4.7\mu F$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$).



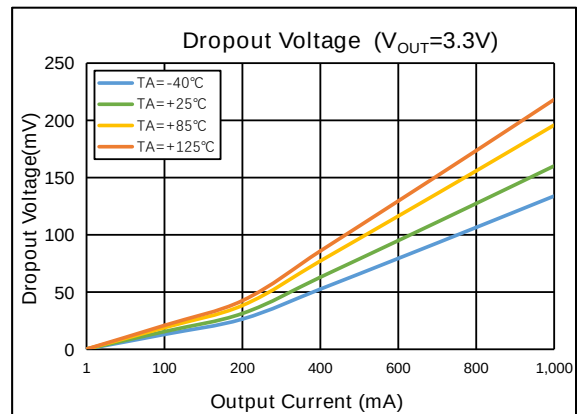
Output Voltage VS Temperature



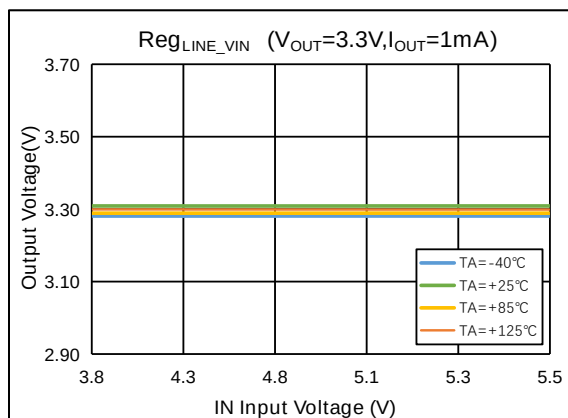
Quiescent Current VS Temperature



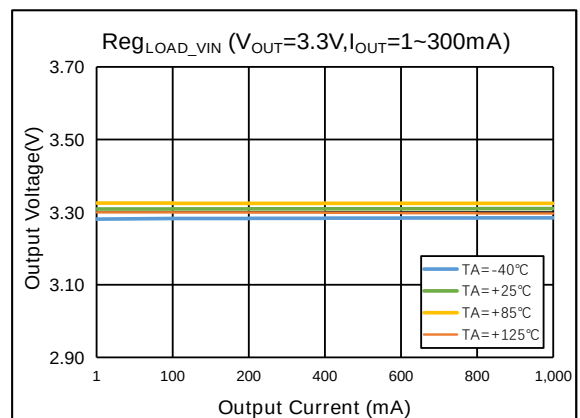
Standby Current VS Temperature



Dropout Voltage VS Output Current



Output Voltage VS Input Voltage

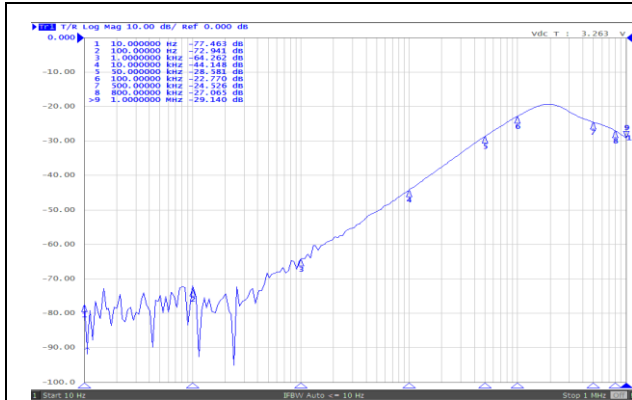


Output Voltage VS Output Current

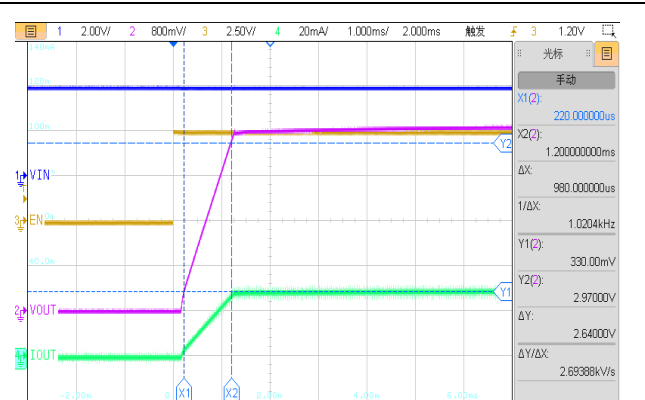
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Typical Characteristics (Continued)

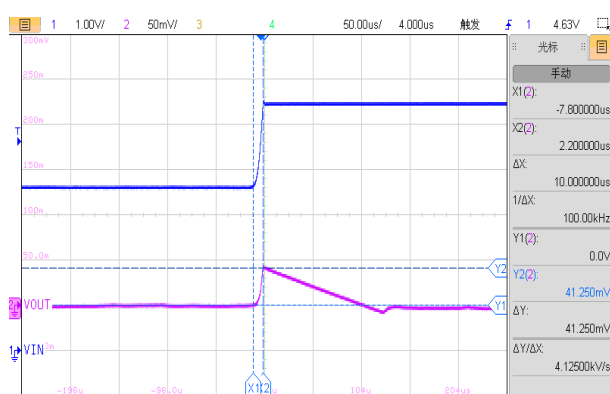
Voltage set 3.3V ($V_{IN} = V_{OUT} + 0.5V$, $V_{EN} = 2.2V$, $I_{OUT} = 1mA$, $R1 = 312.5k\Omega$, $R2 = 100k\Omega$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 4.7\mu F$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$).



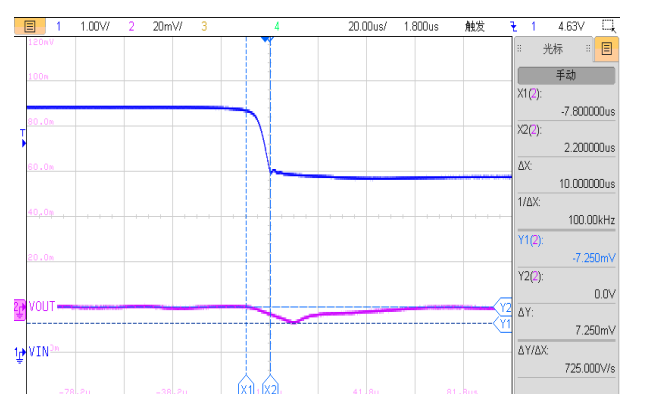
PSRR ($I_{OUT} = 750mA$)



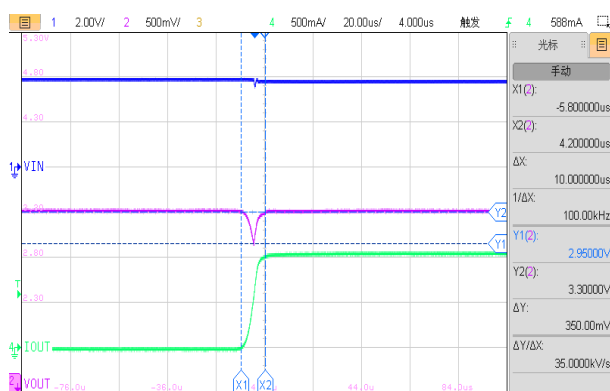
T_{ON} ($I_{OUT} = 30mA$)



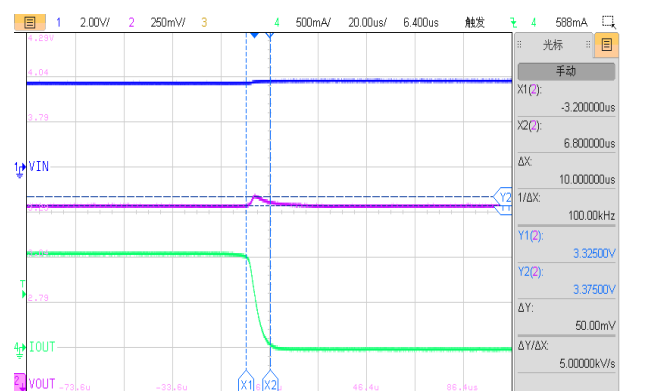
Input-Transient (3.8~5.5V, $t_r = 10\mu s$, $I_{OUT} = 1mA$)



Input-Transient (5.5~3.8V, $t_f = 10\mu s$, $I_{OUT} = 1mA$)



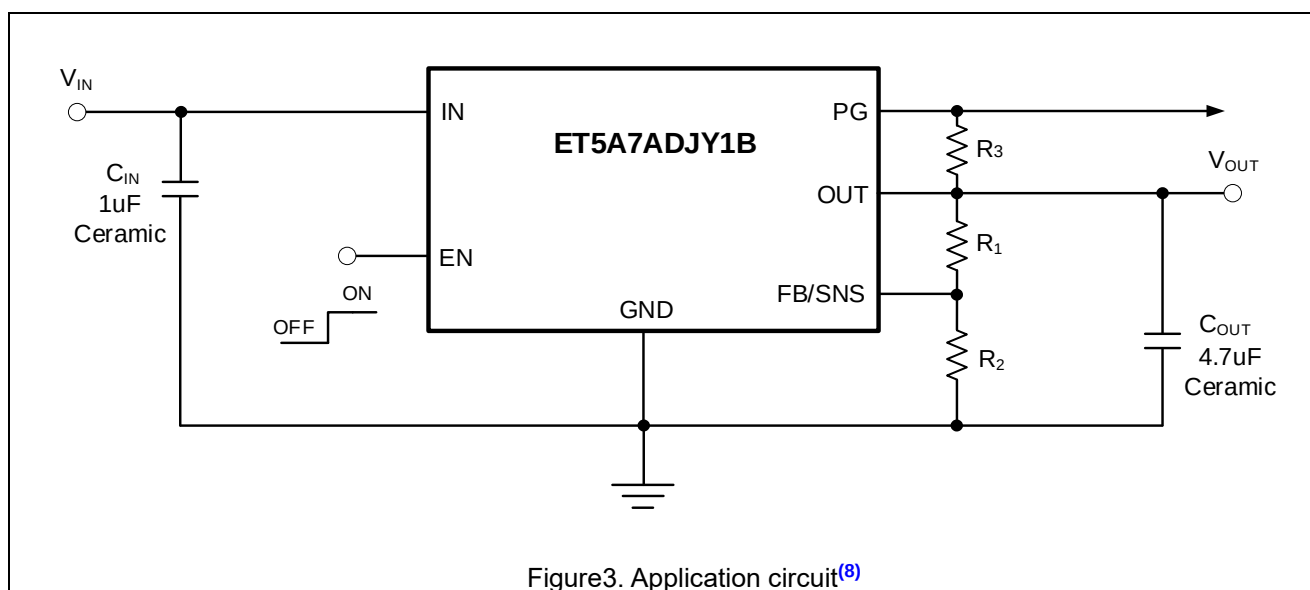
Load-Transient ($V_{IN} = 3.8V$, $I_{OUT} = 1\sim 1000mA$, $t_r = 10\mu s$)



Load-Transient ($V_{IN} = 3.8V$, $I_{OUT} = 1000\sim 1mA$, $t_f = 10\mu s$)

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Application Circuit



Note8: 1): $V_{OUT} = 0.8 * (1 + R1 / R2)$, $(R1 + R2)$ no greater than 100k Ω .

R3: Use a pull-up resistor from 10k Ω to 100k Ω for the best.

2): Recommended Capacitor Values: $C_{IN} = 1\mu F$, $C_{OUT} = 4.7\mu F$.

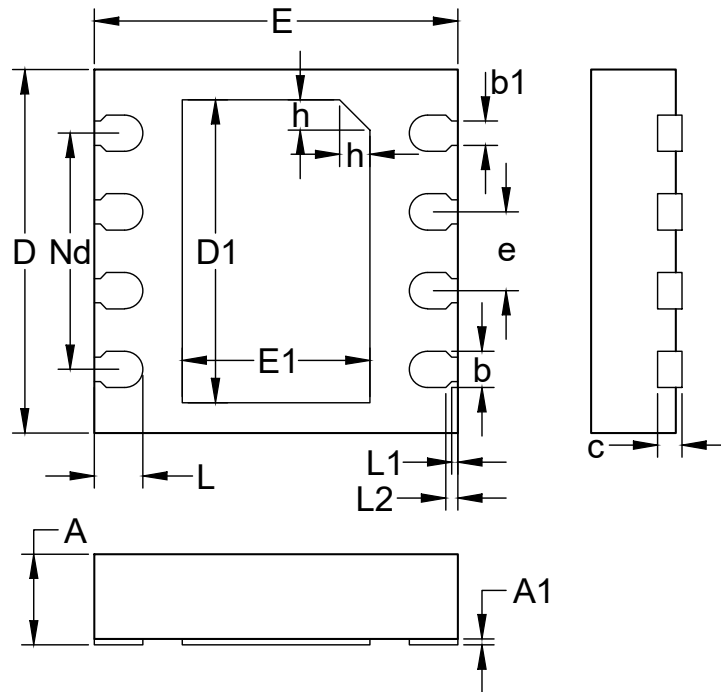
3): Recommended Feedback Resistor Values for Common Output Voltages.

$V_{OUT}(V)$	$R1(K\Omega)$	$R2(K\Omega)$
0.8	0	10
1	2.5	10
1.2	5	10
1.5	8.9	10
1.8	12.5	10
2.5	21	10
3.3	31	10
5	52.3	10

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Package Dimension

DFN8 (3mm x 3mm)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	-	0.95
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
b1	0.20REF		
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D1	2.40	2.50	2.60
e	0.65BSC		
Nd	1.95BSC		
E	2.90	3.00	3.10
E1	1.45	1.55	1.65
L	0.30	0.40	0.50
L1	0.05REF		
L2	0.10REF		
h	0.20	0.25	0.30

