

8:1 CMOS Analog Signal Multiplexer

General Description

The ET74HC4851 is an 8-channel CMOS analog signal multiplexer. It operates from 2.5V to 5.5V single power supply and all digital inputs support 1.8V logic control.

The ET74HC4851 features low voltage, low on-resistance and low off-leakage current. The high performances make it very suitable for multiple applications, such as cellular phones, audio and video signal routing, etc.

The ET74HC4851 is available in Green SOP16, TSSOP16 and QFN16-3×3 packages. It operates over an ambient temperature range of -40°C to +125°C.

Features

- Single Supply Voltage Range: 2.5V to 5.5V
- On-Resistance: 44Ω(TYP) with 5V Supply
- 1.8V Logic Compatible
- Low On-Resistance Flatness
- High Off-Isolation: -85dB (f = 1MHz)
- Low Distortion: 0.7% (R_L = 600Ω, f = 20Hz to 20kHz)
- Package information:

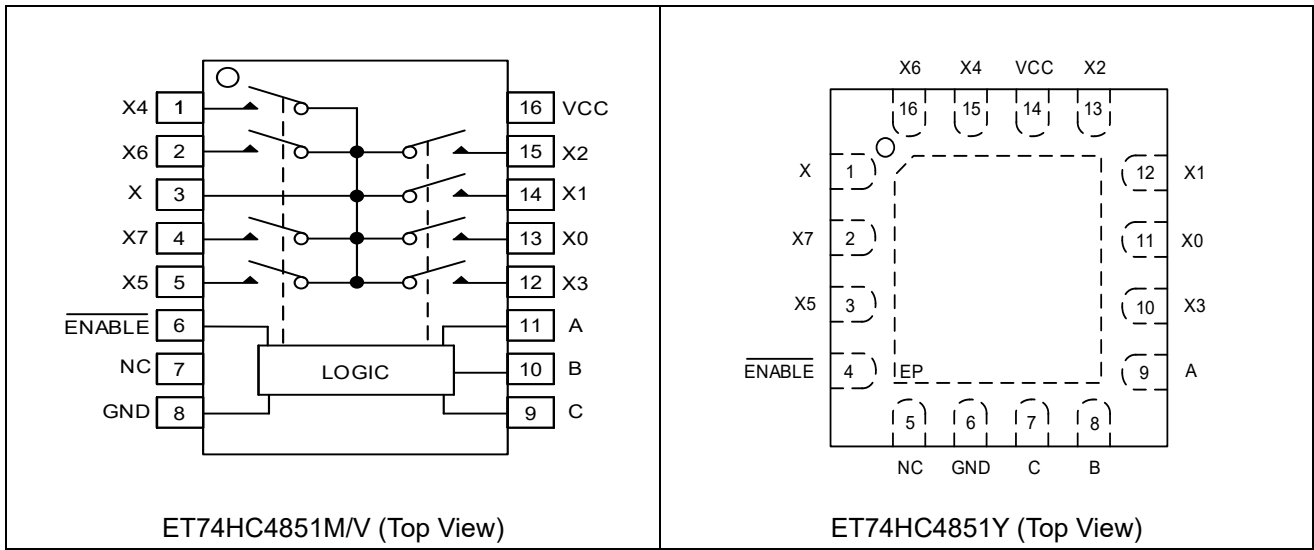
Part No.	Package	Packing Option	MSL
ET74HC4851M	SOP16 (10mm×6mm)	Tape and Reel , 4K	Level 3
ET74HC4851V	TSSOP16 (5mm×6.4mm)	Tape and Reel , 4K	Level 3
ET74HC4851Y	QFN16 (3mm×3mm)	Tape and Reel , 5K	Level 3

Application

- Automotive
- Portable Equipment
- Sample-and-Hold Circuits
- Data-Acquisition Systems
- Battery-Powered Systems
- Audio and Video Signal Routing

ET74HC4851

Pin Configuration



Pin Function

Pin No.		Pin Name	Description
ET74HC4851M/V	ET74HC4851Y		
13, 14, 15, 12, 1, 5, 2, 4	11, 12, 13, 10, 15, 3, 16, 2	X0-X7	Analog Switch Inputs X0-X7.
3	1	X	Analog Switch “X” Output Pin.
6	4	$\overline{\text{ENABLE}}$	Digital Enable Control Pin. Normally connected to GND.
7	5	NC	No Connect.
8	6	GND	Ground. Connect to digital ground.
9	7	C	Digital Address “C” Input Pin.
10	8	B	Digital Address “B” Input Pin.
11	9	A	Digital Address “A” Input Pin.
16	14	VCC	Positive Analog and Digital Supply Voltage Input Pin.
—	Exposed Pad	EP	Exposed Pad. Connect exposed pad to GND.

Note: Any input terminal can be used as an output terminal, and any output terminal can also be used as an input terminal. Signal transmission in both directions is equally well.

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Truth Table

$\overline{\text{ENABLE}}$	Select Inputs			On Switches
	C	B	A	
H	X	X	X	All Switches OFF
L	L	L	L	X-X0
L	L	L	H	X-X1
L	L	H	L	X-X2
L	L	H	H	X-X3
L	H	L	L	X-X4
L	H	L	H	X-X5
L	H	H	L	X-X6
L	H	H	H	X-X7

Note: X Don't care.

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

Symbol	Characteristic	Value	Unit
V_{CC}	Input voltage range ⁽¹⁾	-0.3~6	V
$V_{(X0\sim X7)}$		-0.3~ $V_{CC}+0.3$	V
$V_A, V_B, V_C, V_{ENABLE}$		-0.3~ $V_{CC}+0.3$	V
T_J	Junction Temperature	150	°C
T_L	Lead Temperature (Soldering, 10s)	260	°C
T_{STG}	Storage temperature range	-65~150	°C
V_{ESD}	ESD HBM Susceptibility ⁽²⁾	±4000	V
	ESD CDM Susceptibility ⁽³⁾	±1000	V

Note1: Voltages exceeding V_{CC} or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Recommended Operating Conditions

Symbol	Characteristic	Min	Max	Unit
V_{CC}	Supply Voltage Range	2.5	5.5	V
T_A	Operating Temperature Range	-40	125	°C

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DC Electrical Characteristics

$V_{CC} = 5.0V$, Full = $-40^{\circ}C$ to $+125^{\circ}C$, typical values are at $T_A = +25^{\circ}C$, unless otherwise noted.)

Parameter	Symbol	Conditions	Temp	Min	Typ	Max	Unit
ANALOG SWITCH							
Analog Signal Range	$V_{X_}, V_X$		Full	GND		V_{CC}	V
On-Resistance	R_{ON}	$V_{CC} = 5.0V, I_X = 1mA$	25°C		44	65	Ω
			Full			85	
On-Resistance Match Between Channels	ΔR_{ON}	$V_{CC} = 5.0V, I_X = 1mA$	25°C		1	5	Ω
			Full			6	
On-Resistance Flatness	$R_{FLAT(ON)}$	$V_{CC} = 5.0V, I_X = 1mA$	25°C		14	26	Ω
			Full			35	
X_Off Leakage Current	$I_{X(OFF)}$	$V_{CC} = 5.0V, V_{X_} = 4.5V$ or $0V, V_X = 4.5V$ or $0V$	Full		10	1000	nA
X Off Leakage Current	$I_{X(OFF)}$	$V_{CC} = 5.0V, V_{X_} = 4.5V$ or $0V, V_X = 4.5V$ or $0V$	Full		10	1000	nA
X On Leakage Current	$I_{X(ON)}$	$V_{CC} = 5.0V, V_X = 4.5V$ or $0V$	Full		10	1000	nA
DIGITAL I/O							
Logic Input Logic Threshold High	$V_{AH}, V_{BH},$ V_{CH}, V_{ENH}		Full	1.8			V
Logic Input Logic Threshold Low	$V_{AL}, V_{BL},$ V_{CL}, V_{ENL}		Full			0.5	V
Input-Current High	$I_{AH}, I_{BH},$ I_{CH}, I_{ENH}	$V_A, V_B, V_C, V_{EN} = V_{CC}$	Full		10	1000	nA
Input-Current Low	$I_{AL}, I_{BL},$ I_{CL}, I_{ENL}	$V_A, V_B, V_C, V_{EN} = 0V$	Full		10	1000	nA
DYNAMIC CHARACTERISTICS							
Address Transition Time	t_{TRANS}	$V_{X_} = 3V/0V,$ $R_L = 300\Omega, C_L = 35pF,$ Figure 1	25°C		85		ns
ENABLE Turn-On Time	t_{ON}	$V_{X_} = 3V, R_L = 300\Omega,$ $C_L = 35pF,$ Figure 2	25°C		60		ns
ENABLE Turn-Off Time	t_{OFF}	$V_{X_} = 3V, R_L = 300\Omega,$ $C_L = 35pF,$ Figure 2	25°C		20		ns
Break-Before-Make Time Delay	t_D	$V_{X_} = 3V, R_L = 300\Omega,$ $C_L = 35pF,$ Figure 3	25°C		50		ns
Charge Injection	Q	$R_S = 0\Omega, C_L = 1nF,$ Figure 4	25°C		6		pC
Off Isolation	V_{ISO}	$R_L = 50\Omega, f = 1MHz,$ Figure 5	25°C		-85		dB

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DC Electrical Characteristics(Continued)

$V_{CC} = 5.0V$, Full = $-40^{\circ}C$ to $+125^{\circ}C$, typical values are at $T_A = +25^{\circ}C$, unless otherwise noted.)

Parameter	Symbol	Conditions	Temp	Min	Typ	Max	Unit
Input Off-Capacitance	$C_{X(OFF)}$	$V_{X_{-}} = 0V$, $f = 1MHz$, Figure 6	$25^{\circ}C$		4		pF
Output Off-Capacitance	$C_{X(OFF)}$	$V_{X_{-}} = 0V$, $f = 1MHz$, Figure 6	$25^{\circ}C$		12		pF
Output On-Capacitance	$C_{X(ON)}$	$V_{X_{-}} = 0V$, $f = 1MHz$, Figure 6	$25^{\circ}C$		16		pF
-3dB Bandwidth	BW	$R_L = 50\Omega$	$25^{\circ}C$		180		MHz
Total Harmonic Distortion	THD	$R_L = 600\Omega$, $5V_{P-P}$, $f = 20Hz$ to $20kHz$	$25^{\circ}C$		0.7		%
POWER SUPPLY							
Power Supply Range	V_{CC}		Full	2.5		5.5	V
Power Supply Current	I_{CC}	$V_{CC} = 5.0V$, V_A , V_B , V_C , $V_{EN} = V_{CC}$ or 0	Full		0.01	1	μA

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DC Electrical Characteristics

$V_{CC} = 3.3V$, Full = $-40^{\circ}C$ to $+125^{\circ}C$, typical values are at $T_A = +25^{\circ}C$, unless otherwise noted.)

Parameter	Symbol	Conditions	Temp	Min	Typ	Max	Unit
ANALOG SWITCH							
Analog Signal Range	$V_{X_}, V_X$		Full	GND		V_{CC}	V
On-Resistance	R_{ON}	$I_X = 1mA$	25°C		80	140	Ω
			Full			160	
X_Off Leakage Current	$I_{X_ (OFF)}$	$V_{X_} = 1V, 3V,$ $V_X = 3V, 1V$	Full		10	1000	nA
X Off Leakage Current	$I_{X(OFF)}$	$V_{X_} = 1V, 3V,$ $V_X = 3V, 1V$	Full		10	1000	nA
X On Leakage Current	$I_{X(ON)}$	$V_X = 3V, 1V$	Full		10	1000	nA
DIGITAL I/O							
Logic Input Logic Threshold High	$V_{AH}, V_{BH},$ V_{CH}, V_{ENH}		Full	1.8			V
Logic Input Logic Threshold Low	$V_{AL}, V_{BL},$ V_{CL}, V_{ENL}		Full			0.5	V
Input-Current High	$I_{AH}, I_{BH},$ I_{CH}, I_{ENH}	$V_A, V_B, V_C, V_{EN} = V_{CC}$	Full		10	1000	nA
Input-Current Low	$I_{AL}, I_{BL},$ I_{CL}, I_{ENL}	$V_A, V_B, V_C, V_{EN} = 0V$	Full		10	1000	nA
DYNAMIC CHARACTERISTICS							
Address Transition Time	t_{TRANS}	$V_{X_} = 3V/0V,$ $R_L = 300\Omega, C_L = 35pF,$ Figure 1	25°C		150		ns
ENABLE Turn-On Time	t_{ON}	$V_{X_} = 3V, R_L = 300\Omega,$ $C_L = 35pF$, Figure 2	25°C		110		ns
ENABLE Turn-Off Time	t_{OFF}	$V_{X_} = 3V, R_L = 300\Omega,$ $C_L = 35pF$, Figure 2	25°C		50		ns
Break-Before-Make Time Delay	t_D	$V_{X_} = 3V, R_L = 300\Omega,$ $C_L = 35pF$, Figure 3	25°C		80		ns
-3dB Bandwidth	BW	$R_L = 50\Omega$	25°C		180		MHz
Charge Injection	Q	$R_S = 0\Omega, C_L = 1nF,$ $V_S = 2.5V$, Figure 4	25°C		4		pC
POWER SUPPLY							
Power Supply Current	I_{CC}	$V_A, V_B, V_C,$ $V_{EN} = V_{CC}$ or 0	Full		0.01	1	μA

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Test Circuit and Waveform

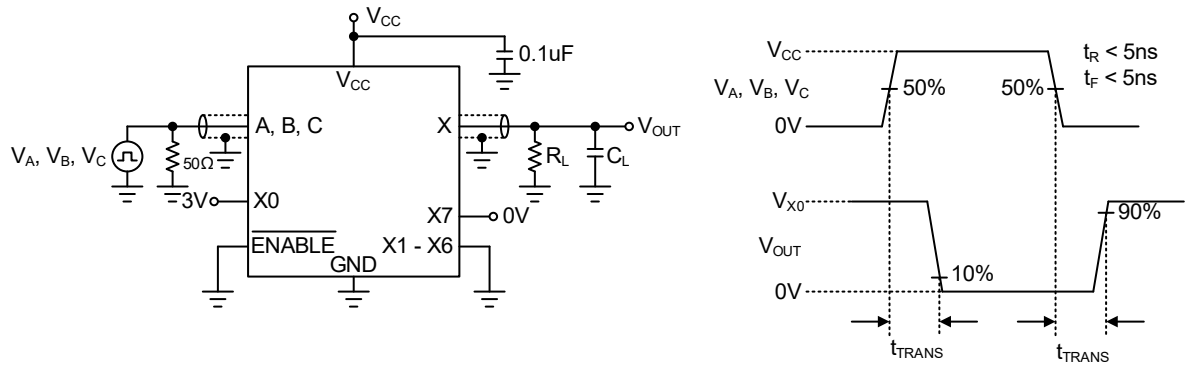


Figure 1. Address Transition Times (t_{TRANS})

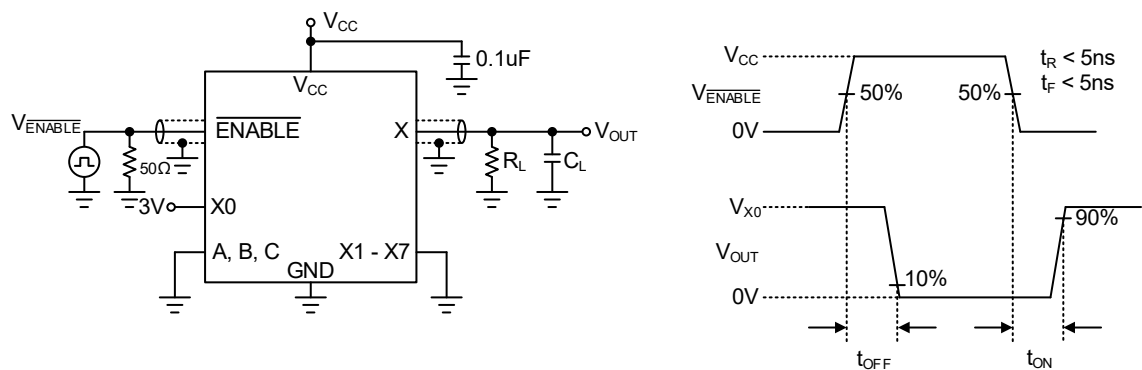


Figure 2. Switching Times (t_{ON}, t_{OFF})

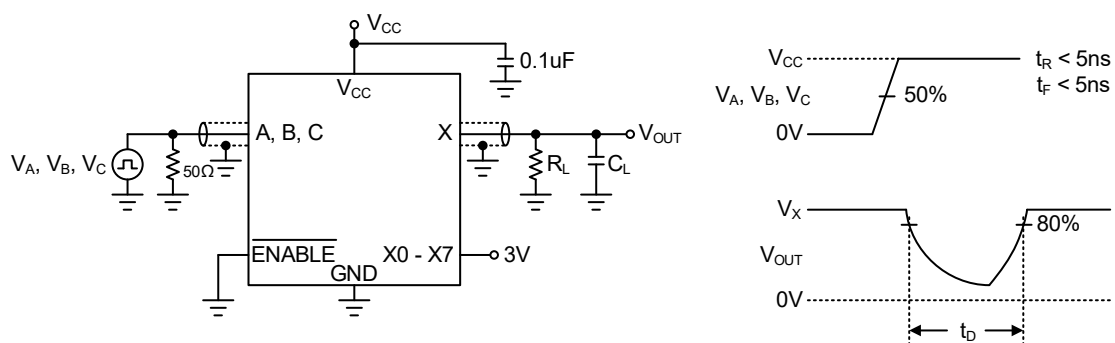


Figure 3. Break-Before-Make Time Delay (t_D)

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Test Circuit and Waveform(Continued)

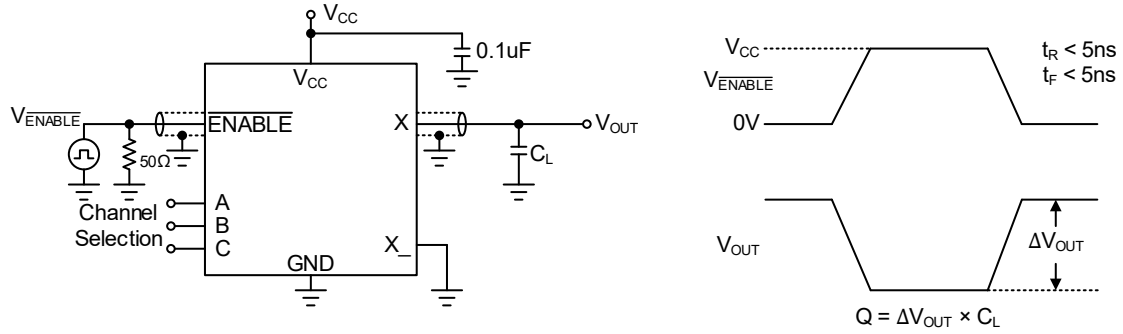


Figure 4. Charge Injection (Q)

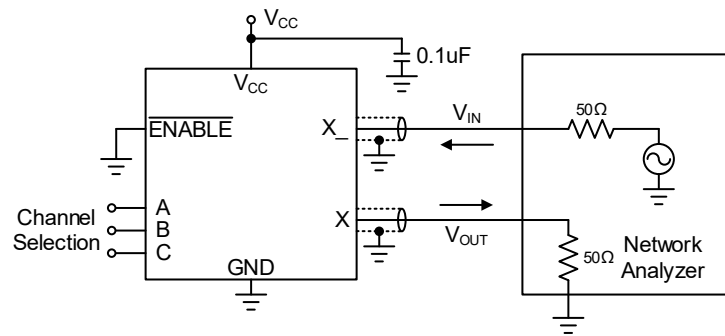


Figure 5. Off Isolation

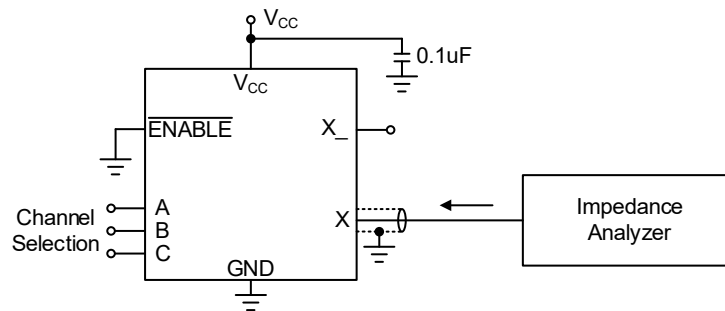


Figure 6. Capacitance

Typical Characteristics

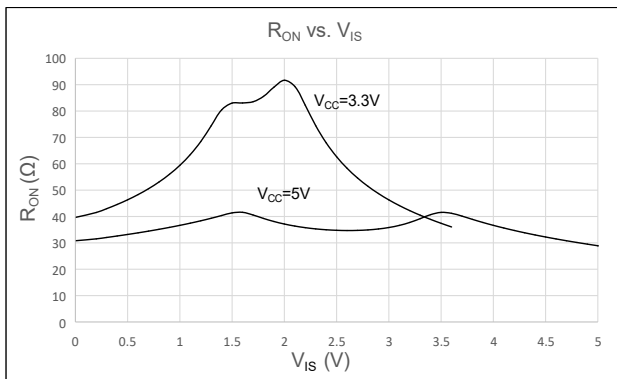


Figure 7. On-Resistance vs. V_{IS}

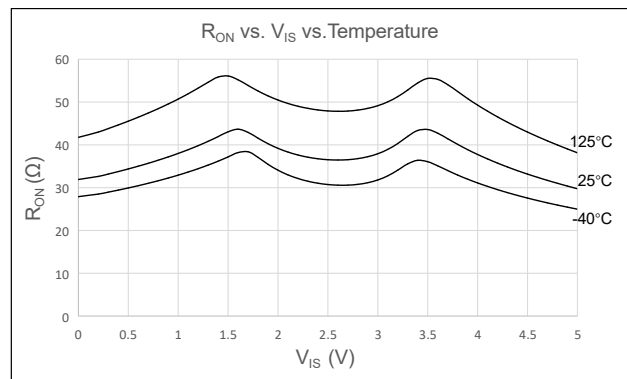


Figure 8. On-Resistance vs. V_{IS} vs. Temp (V_{CC} = 5.0V)

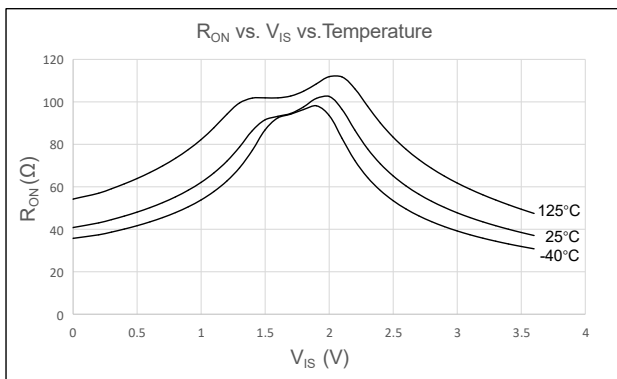


Figure 9. On-Resistance vs. V_{IS} vs. Temp (V_{CC} = 3.3V)

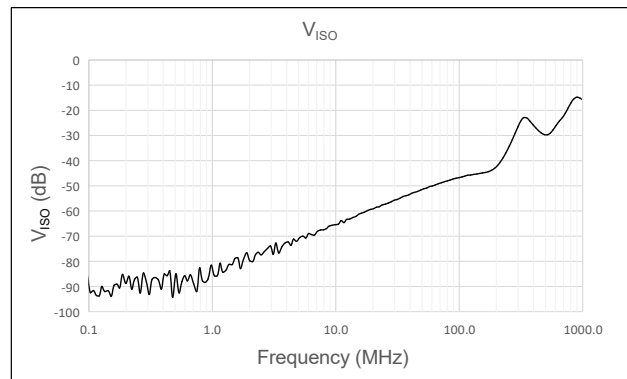
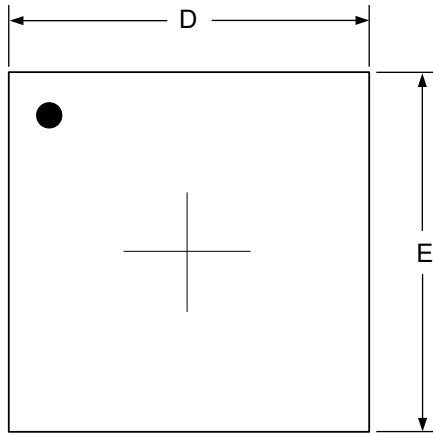


Figure 10. V_{ISO} vs. Frequency

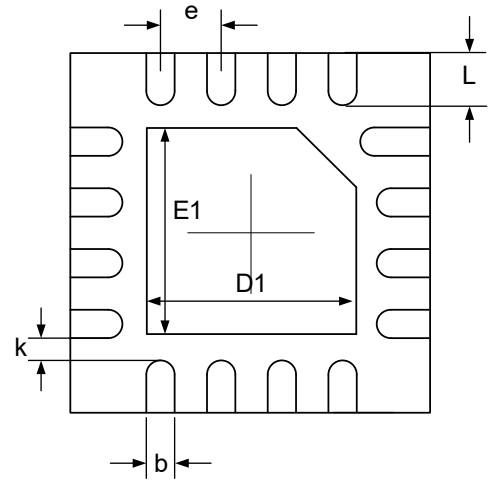
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Package Dimension

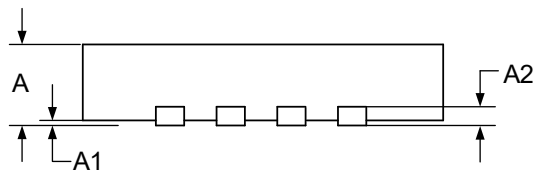
QFN16 (3mm×3mm)



TOP VIEW



BOTTOM VIEW



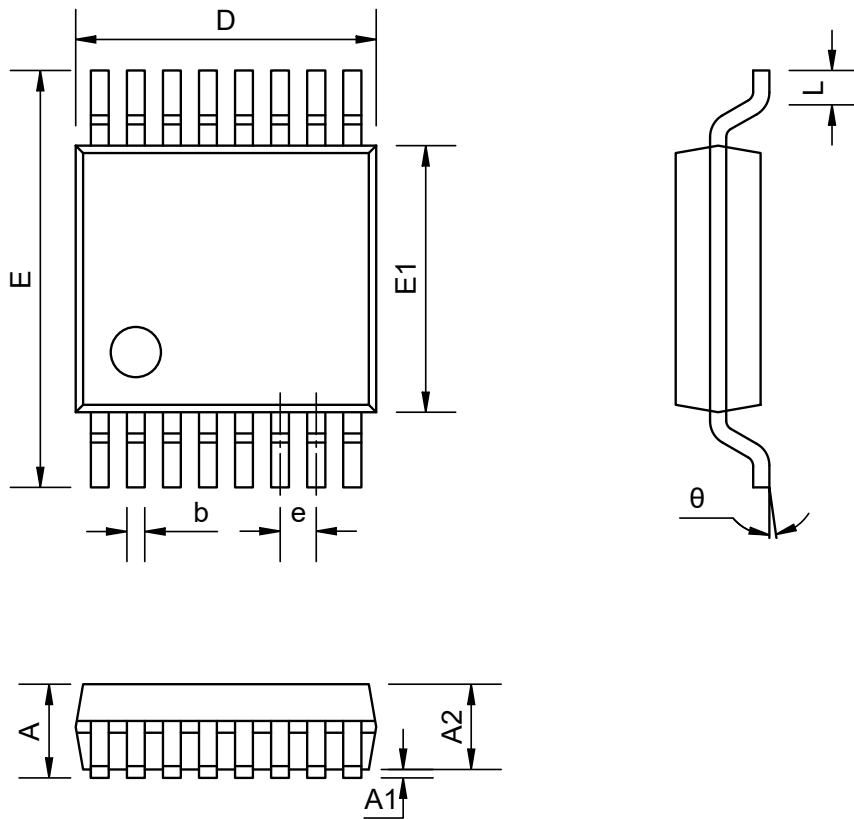
SIDE VIEW

Dimensions Table (Units:mm)

Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203 REF		
b	0.19	0.24	0.29
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.50 TYP		
L	0.30	0.40	0.50
k	0.20 MIN		
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80

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TSSOP16 (5mm×6.4mm)

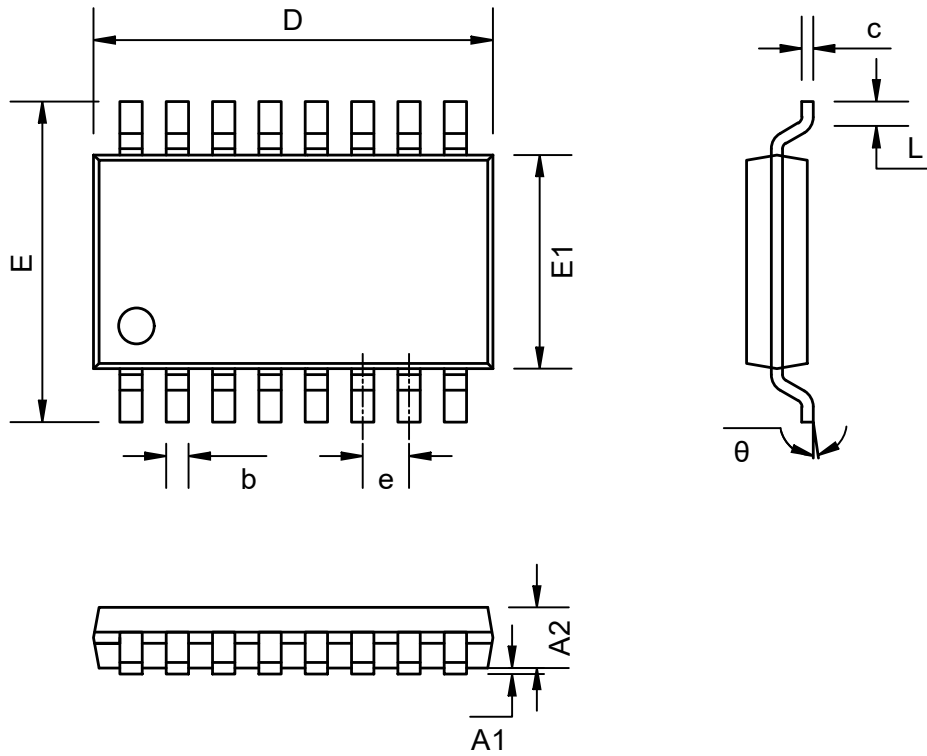


Dimensions Table (Units:mm)

Symbol	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.80	--	1.05
b	0.19	--	0.30
D	4.86	4.98	5.1
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.50	0.60	0.70
θ	1°	--	7°

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SOP16 (6mm×10mm)



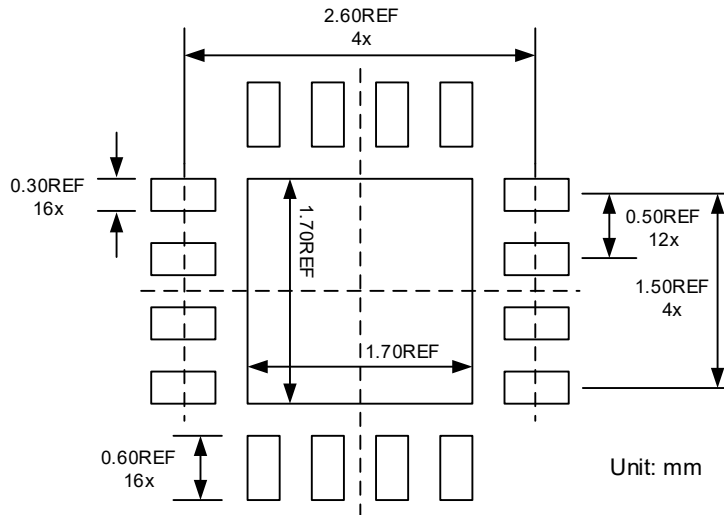
Dimensions Table (Units:mm)

Symbol	Min	Nom	Max
A1	0.10	--	0.25
A2	1.35	1.45	1.55
b	0.33	0.42	0.51
c	0.17	--	0.25
D	9.80	10.00	10.20
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	--	1.27
θ	0°	--	8°

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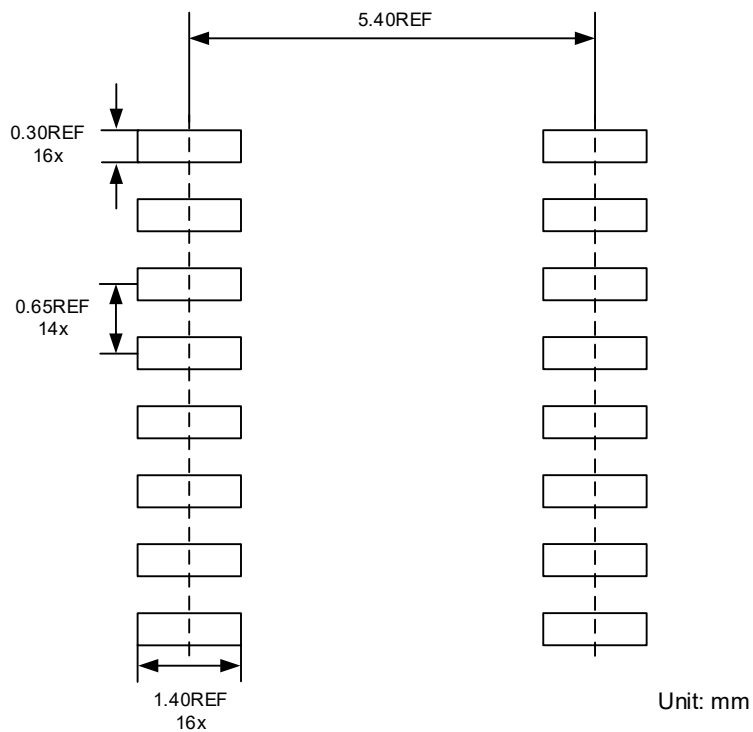
PCB Land Pattern

QFN16 (3mm×3mm)



Recommend Land Pattern

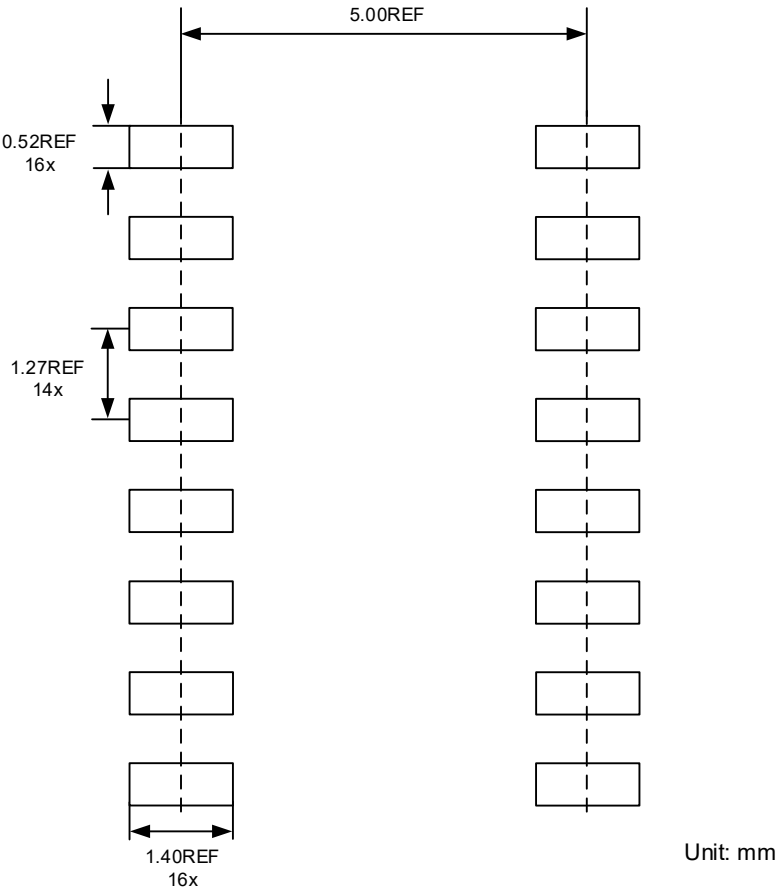
TSSOP16 (5mm×6.4mm)



Recommend Land Pattern

ET74HC4851

SOP16 (6mm×10mm)

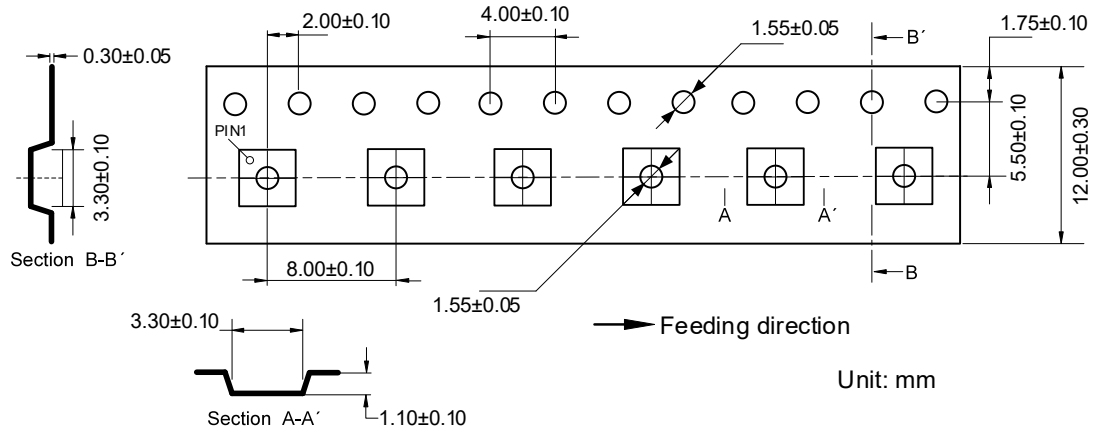


Recommend Land Pattern

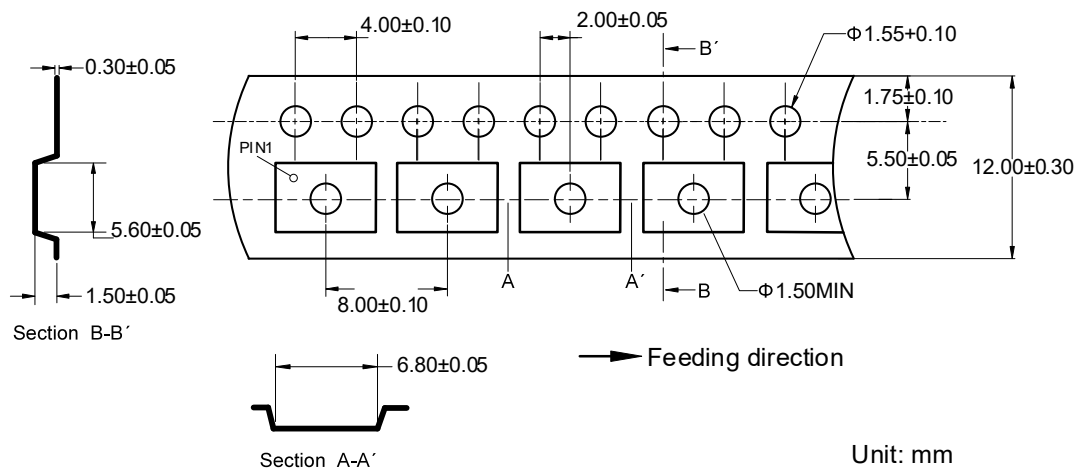
ET74HC4851

Tape Information

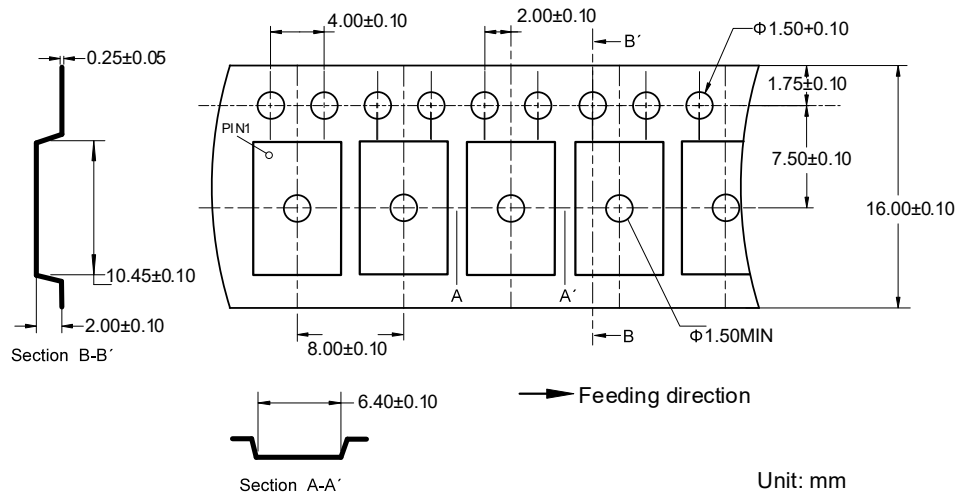
ET74HC4851Y



ET74HC4851V



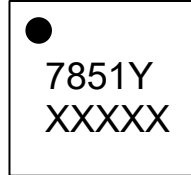
ET74HC4851M



ET74HC4851

Marking Information

ET74HC4851Y

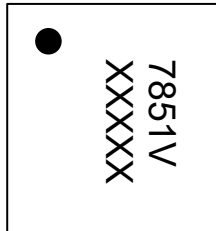


7851Y - Part Number

XXXXX - Tracking Number

Note: X (Tracking Number) is variable, according to the wafer lot number.

ET74HC4851V

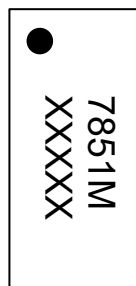


7851V - Part Number

XXXXX - Tracking Number

Note: X (Tracking Number) is variable, according to the wafer lot number.

ET74HC4851M



7851M - Part Number

XXXXX - Tracking Number

Note: X (Tracking Number) is variable, according to the wafer lot number.

ET74HC4851

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2022-11-01	Preliminary Version	Gong Ling Feng	Gong Ling Feng	Gong Ling Feng
1.1	2023-01-05	Update Typeset	Yin Peng	Gong Ling Feng	Yin Peng
1.2	2025-06-11	Update R_{ON} , V_{IH} / V_{IL} spec Add Tape and Marking Information	Gong Ling Feng	Gong Ling Feng	Gong Ling Feng
1.2.a	2025-10-16	Update words	Shib		
1.3	2025-11-18	Update EC table spec Add ESD-CDM Information	Qin Pei Long	Gong Ling Feng	Liu Jia Ying
1.4	2026-05-25	Add PCB Land Pattern	Yin Peng	Gong Ling Feng	Liu Jia Ying