4-Channel LDO PMIC for Camera Applications

General Description

The ET5954 is CMOS-based low-dropout, low-power linear regulator. It's a 4-channel integrated LDOs for camera applications. One channel offering max 1500mA with NMOS pass transistor, three channels offering max 400mA with PMOS pass transistor. ET5954 include 1MHz high speed I²C interface, the function setting is flexible such as output voltage, output discharge, current limit per channel.

The ET5954 is available in WLCSP12 (1.06mm*1.41mm,0.35mm pitch) package.

Features

- LDO1
  - -- VIN1 Input Voltage Range: 0.6V to 2.0V
  - -- LDO1 Output: 0.496V~1.8V@8mV/Step
  - -- Max 1500mA Output Current Capability
  - -- Ultra-Low Dropout: Typ.100mV at 1500ma, 1.2V Output
- LDO2~LDO4
  - -- VIN2/VIN34 Input Voltage Range: 1.8V to 5.5V
  - -- LDO2~LDO4 Output: 1.2V~3.75V@ 10mV/Step
  - -- Max 400mA Output Current Capability
  - -- Less Than 20uV(Typ) Noise
  - -- Ultra-Low Dropout: Typ.110mV at 400mA, 2.8V Output
- Very Low Input Quiescent Current of Typ. 60 μA
- Operation Guaranteed with Battery Voltage Down To 2.5V
- Built-In Thermal Global Shutdown Protection (OTP)
- Built-In Over Current Protection (OCP) and Auto-Discharging Circuit
- Built-In VSYS Under Voltage Lockout (UVLO)
- I²C Serial Control to Program Output Voltage and Features

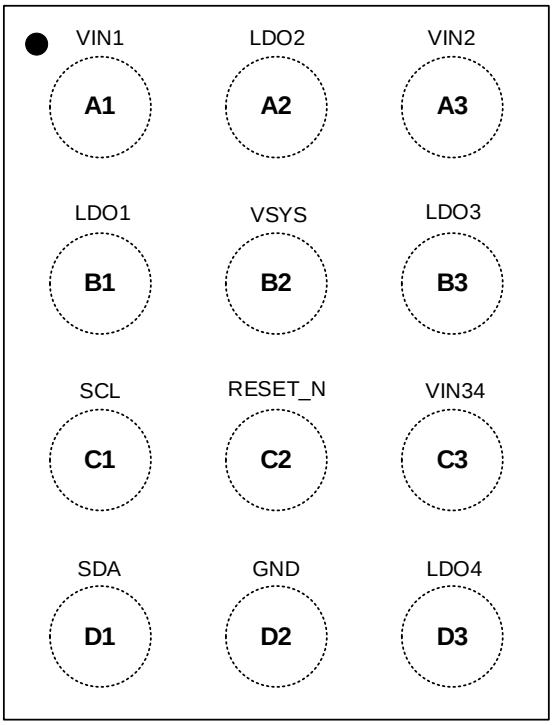
Device Information

Part No.	Package	MSL
ET5954	WLCSP12	1

Applications

- Constant-Voltage Power Supply for Battery-Powered Device
- Constant-Voltage Power Supply for Smartphones, Tablets
- Constant-Voltage Power Supply for Cameras, Dvrs, STB and Camcorders

Pin Configuration

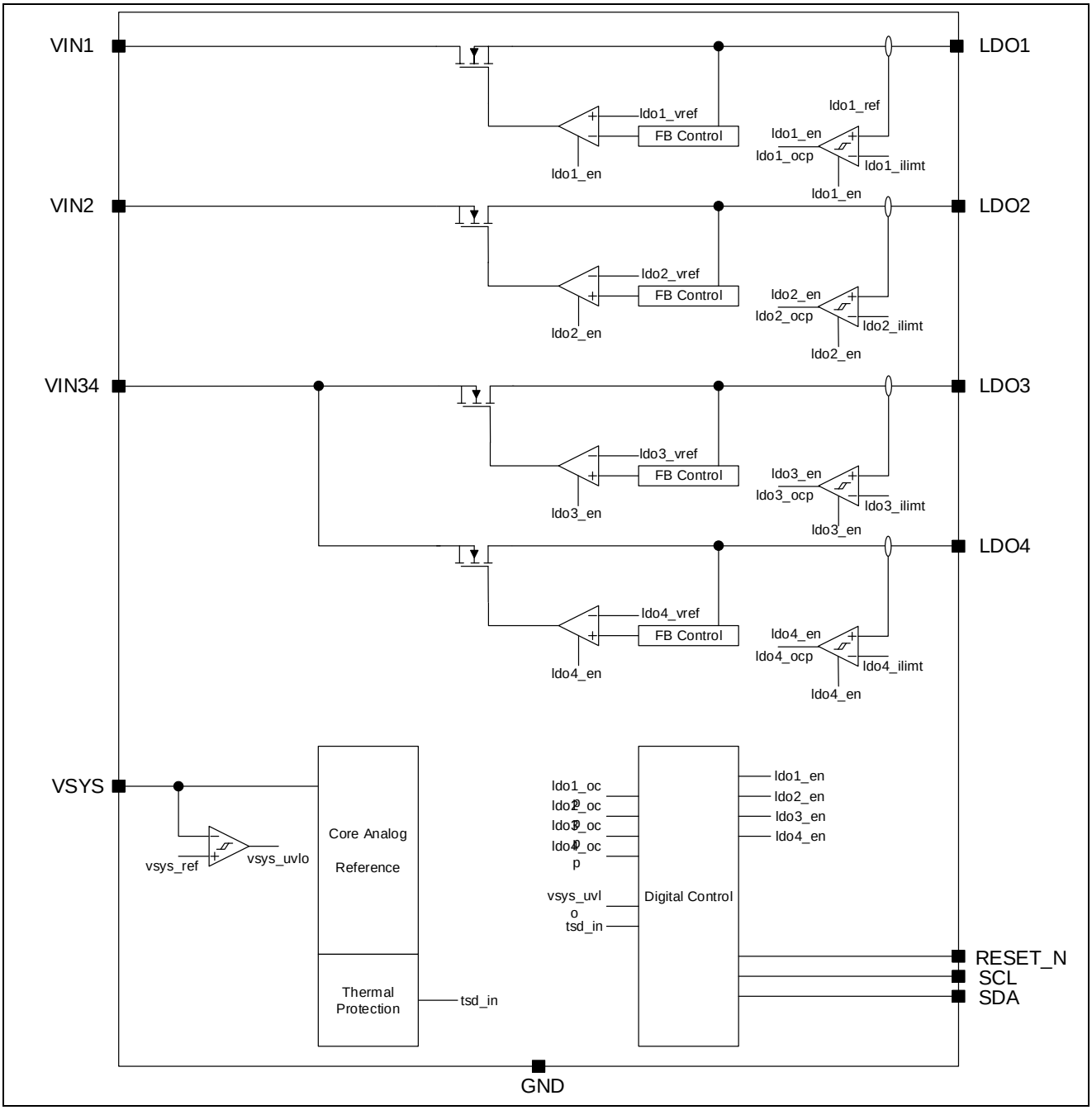


TOP View (Bumps Down) WLCSP12

Pin Function

Pin No.	Pin Name	Pin Function
A1	VIN1	Input Power Pin for LDO1.
A2	LDO2	LDO2 Regulator Output
A3	VIN2	Input Power Pin for LDO2.
B1	LDO1	LDO1 Regulator Output
B2	VSYS	System Power Pin. Route trace from system to this pin.
B3	LDO3	LDO3 Regulator Output
C1	SCL	I^2C Clock Pin. Node should be tied high through a pull up resistor.
C2	RESET_N	RESET_N Pin. Used to enable basic circuits necessary for controlling the PMIC and reset all the digital block. The RESET_N pin has an internal pull-down and should always be connected to a logic high or low.
C3	VIN34	Input Power Pin for LDO3 and LDO4
D1	SDA	I^2C Data Pin. Node should be tied high through a pull up resistor.
D2	GND	Ground Pin.
D3	LDO4	LDO4 Regulator Output

Block Diagram



Functional Description

ET5954 has 4 LDO regulators. LDO1 are using NMOS pass transistor for output voltage regulation. The others LDOs are using PMOS pass transistor for output voltage regulation. The ET5954 LDO1 output voltages can be programmed via I^2C from 0.496V to 1.8V in 8mV steps and LDO2-LDO4 can programmed from 1.2V to 3.75V in 10mV steps using the associated I^2C registers. The voltage transition going from a lower to a higher voltage is a single step with transition time dependent on output current and output capacitance. The output current drives the voltage slew rate from higher to lower voltage transitions.

The device is in reset when the RESET_N is low and will power up the device's main control circuits when RESET_N is pulled high.

If LDOx_EN bits are set to 1 prior to VSYS_EN bit being asserted to 1, the LDOs will power up a short time after VSYS_EN is set to 1. When the VSYS_EN bit is set to 0, all LDOs will be shut off.

When RESET_N is pulled high and VSYS_EN bit is set to 1, each LDO can be accomplished using I^2C register LDOx_EN bit in register 0x03 or LDOx_EN_BK bit in register 0x0B~0x0E.

RESET_N pin, VSYS_EN Bit and ENABLE BITS and ENABLE BACKUP BITS

The tables below provide the states of the LDOs based on the combination of the RESET_N pin, register bit VSYS_EN and enable register bits.

RESET_N	VSYS_EN	LDOX_EN	LDOX_EN_BK	On/Off
0	Reset to 0	Reset to 0	Reset to 0	Off
1	0	0	0	Off
1	0	x	x	Off
1	1	0	0	Off
1	1	1	x	ON
1	1	x	1	ON

Power Up/down Sequence Control

The recommended power on sequence of ET5954 is to power on VSYS first, then power on input power VINx, then set RESET_N to high level, and then enable LDOx. The corresponding power off sequence is to turn off LDOx first, then set RESET_N to low level, then power off input power VINx, and finally power off VSYS.

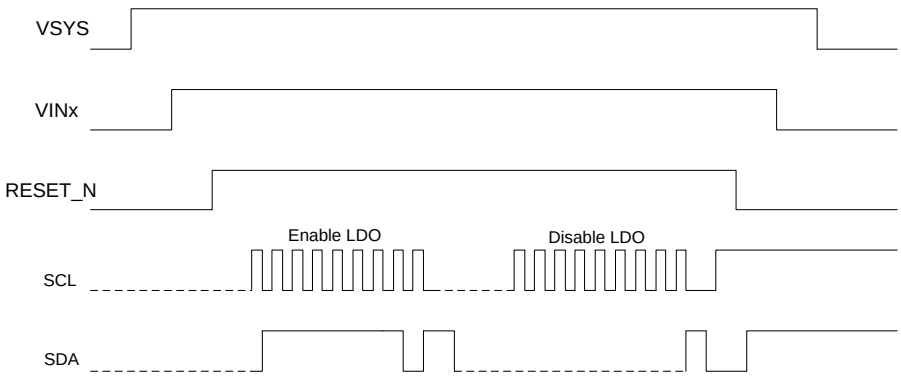


Figure 1. Power up/down sequence control

ET5954 LDOs have internal soft-start which limits the battery current to the setting LDOX_ILIM in register 0x02.

Power-up and shut down of each regulator can be controlled by an I²C register. ldox_en is an internal signal to enable one of regulators. LDOX_VSET[7:0] can set output voltage of each channel.

Shutdown

To disable the ET5954 LDO(s), set the register bit ldox_en to 0 in register 0x03 and ldox_en_bk bit to 0 in register 0x0B~0x0E or set vsys_en bit to 0 in register 0x03. To do a global shutdown of all LDOs, it also can set the RESET_N pin to low, and all registers will reset to default value.

VSYS UVLO

All LDOs use VSYS to power their analog and control circuitry. For proper operation the VSYS input is monitored for under voltage conditions. LDO1 use VIN1, LDO2 uses VIN2, LDO3 and LDO4 use VIN34 to power their outputs.

If VSYS is greater than the POR threshold (~2.0V), but did not reach VSYS_UVLO_RISE when RESET_EN is high. When the LDO(s) are commanded to start or are running when VSYS falls below the UVLO threshold, but above VPOR, Device in shutdown, I²C registers not reliable.

PMIC Operation in VSYS UVLO

VSYS State	RESET_N	VSYS_EN	Results
VSYS < VPOR	Low	1	Device in Shutdown, I²C Registers not Reliable
VPOR < VSYS < UVLO	Low	1	Device in Shutdown, I²C Registers not Reliable
VSYS > UVLO	Low	1	Device in Shutdown, I²C Registers not Reliable
VSYS < VPOR	High	1	Device in Shutdown, I²C Registers not Reliable
VPOR < VSYS < UVLO	High	1	Band Gap On, I²C Registers Readable.
VPOR < VSYS < UVLO	High	0	Band Gap Off, I²C Registers Readable.
VSYS > UVLO	High	1	Band Gap On. Device Can Enable by I²C.

When an over-temperature or a VSYS UVLO event occurs, all ET5954 LDOs are disabled.

Current Limit Protection

For each channel, when output current of LDO output pin is higher than current limit threshold or the output pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage. Set related bits to select Current limit threshold register.

The LDO output current is short-circuit protected and the short-circuit current level can be programmed using the settings in register 0x02, LDO_ILIMT. When a short occurs(VLDO1<35%VSET, VLDO2~4<0.5V) on the LDOx output, the current is automatically limited to the programmed current limit and Vout may drop, depending on the difference between the input and target output voltage. The resultant VOUT is the product of current limit setting in register 0x02 LDO_ILIMT and the load impedance.

Inrush Current Limit

After enable the LDOs, the inrush current limit circuit is in operation, LDO1 inrush time is approximately 2ms, and LDO2~4 inrush time is approximately 700us. Therefore, the load current should be drawn after the output

voltage reached the preset value.

If the load current is drawn during the start-up, it should be within the following values:

$I_{OUT}x \leq 2/3 *$ Normal current limit

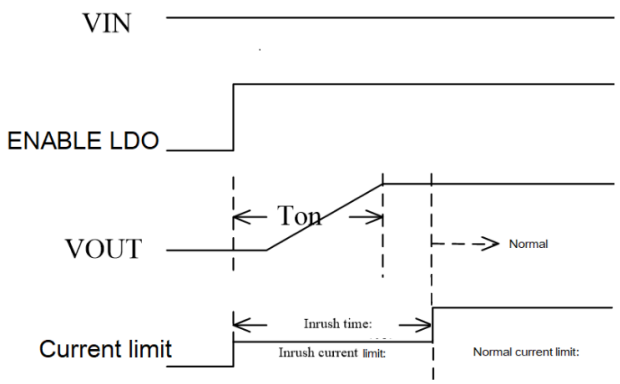


Figure 7.

Thermal Shutdown Protection

If the die temperature continues to rise above the Thermal Shutdown level, a Thermal Shutdown event is activated at a nominally 145°C. When the Thermal Shutdown level is reached, all power outputs are disabled without shutdown sequencing, but I²C communications remain. The device remains in thermal shutdown until the die temperature falls to approximately +120°C.

Auto Discharging

For each channel, when shut down the output, the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of output pin in very short time. The Auto-Discharging function is optional. Set related bits to select output discharge function for Discharge Resistor (LDO_DIS Register), “1”: Enable. “0”: Disable.

Input and output Capacitor

The LDO1 are designed to be stable for ceramic output capacitors with Effective capacitance in the range from 3μF to 22μF. The LDO2~LDO4 are designed to be stable for ceramic output capacitors with Effective capacitance in the range from 0.68μF to 10μF.

The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range. In applications where no low input supplies impedance available, the recommended C_{VSYS}, C_{VIN2}, C_{VIN34} Capacitance ≥0.68uF and C_{VIN1}≥3uF.

Serial Port Interface (I²C)

Bus Interface

Baseband Processor can transmit data with ET5954 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the

level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET5954 will send a low-level response signal with one period width to the SDA port. During the reading mode, ET5954 will not send response signal and the host will send a high response signal one period width to the SDA.

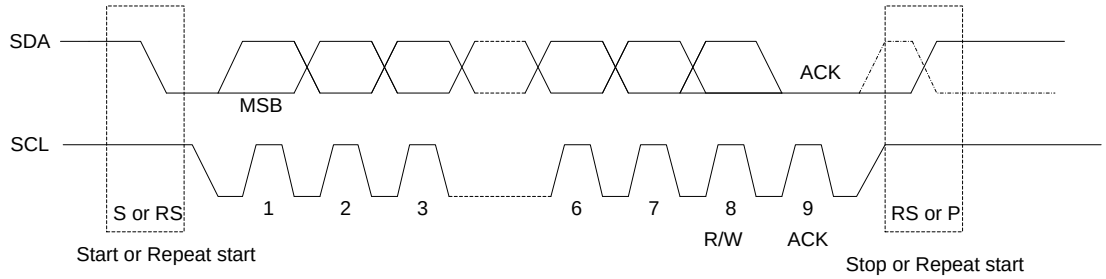


Figure 10. I²C write mode

- ACK = Acknowledge
- MSB = Most Significant Bit
- S = Start Conditions RS = Restart Conditions P = Stop Conditions
- Fastest Transmission Speed = 1000KBITS/S
- Restart: SDA-level turnover as expressed by the dashed line waveform

I²C Slave Address

The default 7bit I²C slave address is 1100110b(0x66), and 8bit address for the writing register mode is 11001100b(0xCC), the reading register mode is 11001101b(0xCD).

I²C Writing Command Register Interface Protocol (continuous)：

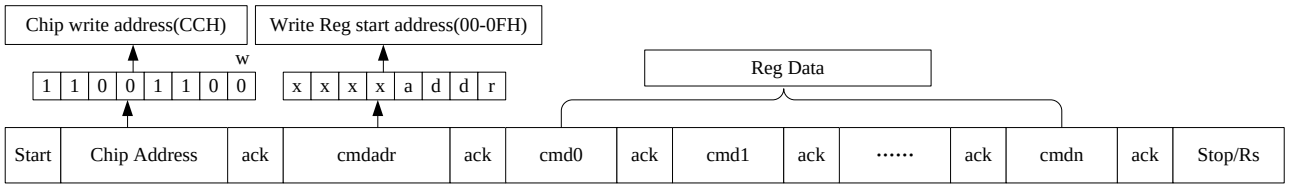


Figure 11. I²C Writing Command Register(continuous)

- Start = Start Conditions
- Chip address = Write register address = 1100110 + 0(w)b
- ack=Acknowledge from ET5954
- Write Reg start address byte = cmdadr(xxxx + REG's 4bit addr)
- ack = Acknowledge from ET5954
- Reg data 0 = cmd0(Command data0)
- ack = Acknowledge from ET5954
- ……
- Reg data n = cmdn(Command datan)
- ack = Acknowledge from ET5954
- Stop/Rs = Stop Condition/Restart Condition

I²C Writing Command Register Interface Protocol (single)：

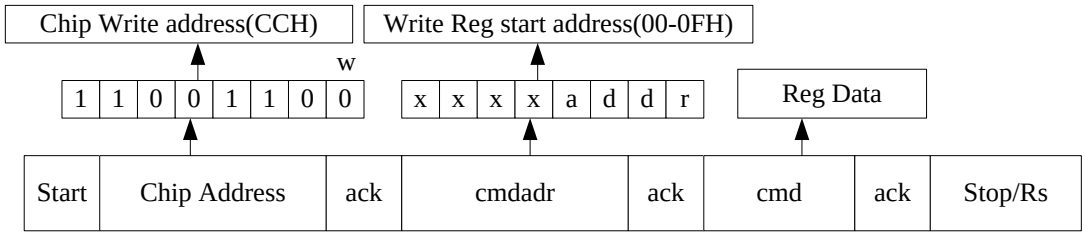


Figure 12. I²C Writing Command Register(single)

- Start = Start Conditions
- Chip address = Write register address = 1100110 + 0(w)b
- ack = Acknowledge from ET5954
- Write Reg start address byte = cmdadr(xxxx + REG's 4bit addr)
- ack=Acknowledge from ET5954
- Reg data = cmd(Command data)
- ack = Acknowledge from ET5954
- Stop/Rs = Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol(continuous)

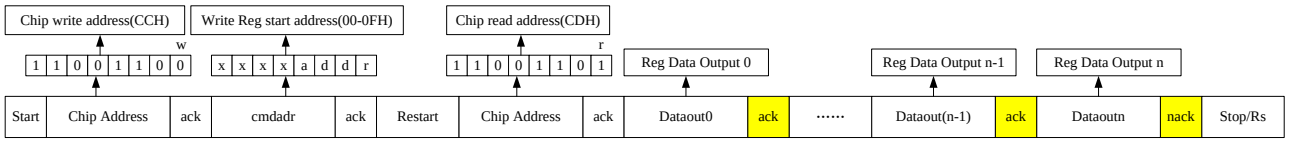


Figure 13. I²C Reading Command Register(continuous)

- Start = Start Conditions
- Chip address = Write register address = 1100110 + 0(w)b
- ack = Acknowledge from ET5954
- Write Reg start address byte = cmdadr(xxxx + REG's 4bit addr)
- ack = Acknowledge from ET5954
- Restart = Restart condition
- Chip address Read register address = 1100110 + 1(r)b
- ack = Acknowledge from ET5954
- Dataout0 = Register data output 0
- ack = Acknowledge from Host
- ……
- Dataoutn = Register data output n
- nack = No Acknowledge from Host
- Stop/Rs = Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol(single)

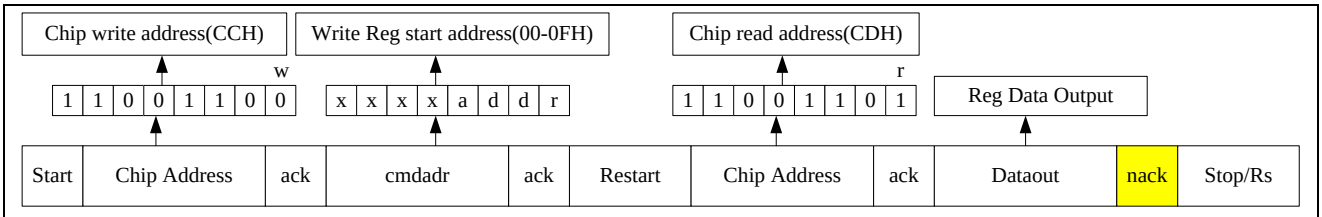


Figure 14. I²C Reading Command Register(single)

- Start = Start Conditions
- Chip address = Write register address = 1100110 + 0(w)b
- ack = Acknowledge from ET5954
- Write Reg start address byte = cmdadr(xxxx + REG's 4bit addr)
- ack = Acknowledge from ET5954
- Restart = Restart condition
- Chip address Read register address = 1100110 + 1(r)b
- ack = Acknowledge from ET5954
- Dataout = Register data output
- nack = No Acknowledge from Host
- Stop/Rs = Stop Condition/Restart Condition

Register Map

Addr	Name	RST	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	CHIPID	0x54	010101						chip_id[1:0]	
0x01	VERID	0x00	Rev.						ver_id[1:0]	
0x02	LDO_ILIMIT	0x55	ldo4_ilimt[1:0]		ldo3_ilimt[1:0]		ldo2_ilimt[1:0]		ldo1_ilimt[1:0]	
0x03	LDO_DIS	0x0F	0	0	0	0	ldo4_dis	ldo3_dis	ldo2_dis	ldo1_dis
0x04	LDO_EN	0x80	vsys_en	0	0	0	ldo4_en	ldo3_en	ldo2_en	ldo1_en
0x05	LDO1_VSET	0x95	ldo1_vset[7:0]							
0x06	LDO2_VSET	0xA0	ldo2_vset[7:0]							
0x07	LDO3_VSET	0xA0	ldo3_vset[7:0]							
0x08	LDO4_VSET	0xA0	ldo4_vset[7:0]							
0x09	SOFT_RESET	0x00	Rev.				soft_reset[3:0]			
0x0A	LDO_FLT _MASK	0x00	Rev.				ldo4_flt _mask	ldo3_flt _mask	ldo2_flt _mask	ldo1_flt _mask
0x0B	LDO1_EN_BK	0x00	ldo1_en_bk	Rev.						
0x0C	LDO2_EN_BK	0x00	ldo2_en_bk	Rev.						
0x0D	LDO3_EN_BK	0x00	ldo3_en_bk	Rev.						
0x0E	LDO4_EN_BK	0x00	ldo4_en_bk	Rev.						
0x0F	STATU	0x00	tsd	vsys_uvlo			ldo4_ocp	ldo3_ocp	ldo2_ocp	ldo1_ocp

- **0x00 CHIPID Register---- Indicates the product ID with revision. Default = 0x54 Type: Read only**

chip_id[1:0] Indicates the product ID with revision. Read only.

- **0x01 VERID Register---- Indicates the device ID with revision. Default = 0x00 Type: Read only**

ver_id[1:0] Indicates the device ID with revision. Read only.

- **0x02 LDO_ILIMIT Register ----LDO Current Limit Selection. Default = 0x55**

The detail current limit threshold value is shown in the table as below:

Bit	Name	Default	Type	Description
7:6	ldo4_ilimt	01	R/W	LDO4 Current Limit Threshold Value: **00b:** current limit~450mA short current limit~45mA **01b:** current limit~600mA short current limit~60mA **10b:** current limit~750mA short current limit~75mA **11b:** current limit~900mA short current limit~90mA
5:4	ldo3_ilimt	01	R/W	LDO3 Current Limit Threshold Value: **00b:** current limit~450mA short current limit~45mA **01b:** current limit~600mA short current limit~60mA **10b:** current limit~750mA short current limit~75mA **11b:** current limit~900mA short current limit~90mA
3:2	ldo2_ilimt	01	R/W	LDO2 Current Limit Threshold Value: **00b:** current limit~450mA short current limit~45mA **01b:** current limit~600mA short current limit~60mA **10b:** current limit~750mA short current limit~75mA

				11b: current limit~900mA short current limit~90mA
1:0	ldo1_ilimt	01	R/W	LDO1 Current Limit Threshold Value: **00b:** current limit~1900mA short current limit~430mA **01b:** current limit~2500mA short current limit~550mA **10b:** current limit~3100mA short current limit~680mA **11b:** current limit~3700mA short current limit~820mA

- **0x03 LDO_DIS Register ----Discharge Resistor Selection. Default = 0x0F**

Each LDO regulators output discharge resistor enable control.

Bit	Name	Default	Type	Description
7:4	Rev.	0000	R	Reserved
3	ldo4_dis	1	R/W	LDO4 Discharge Enabled/Disabled Control: **0b:** Disable Pull down will not be activated when LDO4 is disabled by any event **1b:** Enable Pull down will be activated when LDO4 is disabled by RESET_N going low or ldo4_en = 0 or TSD or VSYS_UVLO event
2	ldo3_dis	1	R/W	LDO3 Discharge Enabled/Disabled Control: **0b:** Disable Pull down will not be activated when LDO3 is disabled by any event **1b:** Enable Pull down will be activated when LDO3 is disabled by RESET_N going low or ldo3_en = 0 or TSD or VSYS_UVLO event
1	ldo2_dis	1	R/W	LDO2 Discharge Enabled/Disabled Control: **0b:** Disable Pull down will not be activated when LDO2 is disabled by any event **1b:** Enable Pull down will be activated when LDO2 is disabled by RESET_N going low or ldo2_en = 0 or TSD or VSYS_UVLO event
0	ldo1_dis	1	R/W	LDO1 Discharge Enabled/Disabled Control: **0b:** Disable Pull down will not be activated when LDO1 is disabled by any event **1b:** Enable Pull down will be activated when LDO1 is disabled by RESET_N going low or ldo1_en = 0 or TSD or VSYS_UVLO event

- **0x04 LDO_EN Register ----LDOs Chip enable control register. Default = 0x80**

This register can be written to enable or disable the corresponding LDO regulator.

Bit	Name	Default	Type	Description
7	vsys_en	1	R/W	Enable Bit for System. The system bias will be getting ready for enabling individual LDO if bit7 = 1 and RESET_N is pulled high Please ensure individual LDO in the off state before bit7 = 0
6:4	Rev.	000	R	Reserved
3	ldo4_en	0	R/W	LDO4 Enable Control: **0b:** Disable **1b:** Enable
2	ldo3_en	0	R/W	LDO3 Enable Control: **0b:** Disable **1b:** Enable
1	ldo2_en	0	R/W	LDO2 Enable Control: **0b:** Disable **1b:** Enable
0	ldo1_en	0	R/W	LDO1 Enable Control: **0b:** Disable **1b:** Enable

- **0x05 LDO1 Register ---- LDO1 output voltage setting register. Default = 0x95 Type: R/W**

The register LDO1_VSET[7:0] set the voltage of LDO1, it have about 164 steps, shown as below table, the formula is VOUT = 0.496V + (d - 61) * 0.008V;

Output Voltage set by LDO1_VSET[7:0]		
Dec	**Binary**	**Output Voltage(V)**
0	00000000	Reserved
1	00000001	Reserved
2~60	…..	Reserved
61	00111101	0.496
62	00111110	0.504
63	00111111	0.512
64~148	……	……
149	**10010101(default)**	**1.200**
150	10010110	1.208
151	10010111	1.216
152~222	……	……
223	11011111	1.792
224	11100000	1.800
225~255	11100001~11111111	Reserved

- **0x06~0x08 LDO2~4 Register ---- LDO2~4 output voltage setting register. Default = 0xA0 Type: R/W**

The registers LDO2~4_VSET[7:0] set the voltage of LDO2~LDO4, each voltage have 256 steps, shown as below table, the formula is V_{OUT} = 1.2V + d * 0.01V.

Output Voltage set by LDO2~4_VSET[7:0]		
Dec	**Binary**	**Output Voltage(V)**
0	00000000	1.20
1	00000001	1.21
2	00000010	1.22
3~14	……	……
15	00001111	1.35
16	00010000	1.36
17	00010001	1.37
18	00010010	1.38
19	00010011	1.39
……	……	……
160	**10100000(default)**	**2.80**
161	10100001	2.81
162	10100010	2.82
……	……	……
255	11111111	3.75

- **0x09 SOFT_RESET Register ----LDOs reset control register. Default = 0x00**

Bit	Name	Default	Type	Description
7:4	Rev.	0000	R	Reserved
3:0	soft_reset	0000	W/C	Writing a "1011" begins a soft reset of the device I^2C registers to their default values. This bit is cleared upon execution of the Reset function. Any other value than "1011" will be ignored.

- **0x0A LDO_FLT_MASK Register ----LDO Filter Capacitor Mask Control register. Default = 0x00**

Each LDO Filter Capacitor Mask enable control.

Bit	Name	Default	Type	Description
7:4	Rev.	0000	R	Reserved
3	ldo4_flt_mask	0	R/W	LDO4 Filter Capacitor Mask Enabled/Disabled Control: **0b:** Disable Don't mask LDO4 filter capacitor **1b:** Enable Mask LDO4 filter capacitor, it will accelerate the response speed of dynamic voltage regulation.
2	ldo3_flt_mask	0	R/W	LDO3 Filter Capacitor Mask Enabled/Disabled Control: **0b:** Disable Don't mask LDO3 filter capacitor **1b:** Enable Mask LDO3 filter capacitor, it will accelerate the response speed of dynamic voltage regulation.
1	ldo2_flt_mask	0	R/W	LDO2 Filter Capacitor Mask Enabled/Disabled Control: **0b:** Disable Don't mask LDO2 filter capacitor **1b:** Enable Mask LDO2 filter capacitor, it will accelerate the response speed of dynamic voltage regulation.
0	ldo1_flt_mask	0	R/W	LDO1 Filter Capacitor Mask Enabled/Disabled Control: **0b:** Disable Don't mask LDO1 filter capacitor **1b:** Enable Mask LDO1 filter capacitor, it will accelerate the response speed of dynamic voltage regulation.

- **0x0B LDO1_EN_BK Register ----LDO1 enable backup control register. Default = 0x00**

Bit	Name	Default	Type	Description
7	ldo1_en_bk	0	R/W	LDO1 Backup Enable Control Signal **0b:** Disable LDO1 Output. **1b:** Enable LDO1 Output.
6:0	Rev	7'h00	R	Reserved

- **0x0C LDO2_EN_BK Register ----LDO2 enable backup control register. Default = 0x00**

Bit	Name	Default	Type	Description
7	ldo2_en_bk	0	R/W	LDO2 Backup Enable Control Signal **0b:** Disable LDO2 Output. **1b:** Enable LDO2 Output.
6:0	Rev.	0000000	R	Reserved

- **0x0D LDO3_EN_BK Register ----LDO3 enable backup control register. Default = 0x00**

Bit	Name	Default	Type	Description
7	ldo3_en_bk	0	R/W	LDO3 Backup Enable Control Signal **0b:** Disable LDO3 Output. **1b:** Enable LDO3 Output.
6:0	Rev.	0000000	R	Reserved

- **0x0E LDO4_EN_BK Register ----LDO4 enable backup control register. Default = 0x00**

Bit	Name	Default	Type	Description
7	ldo4_en_bk	0	R/W	LDO4 Backup Enable Control Signal **0b:** Disable LDO4 Output. **1b:** Enable LDO4 Output.
6:0	Rev	0000000	R	Reserved

Note: ldox_en_bk and ldox_en(x = 1~4) are OR relation, such as when ldo1_en or ldo1_en_bk set to high, then LDO1 will be enable, when ldo1_en and ldo1_en_bk set to low, then LDO1 will be disable. Other three LDOs enable signal relation is the similar with LDO1. Recommend using only one control method to control LDO.

- **0x0F STATU Register ----Chip status register. Default = 0x00**

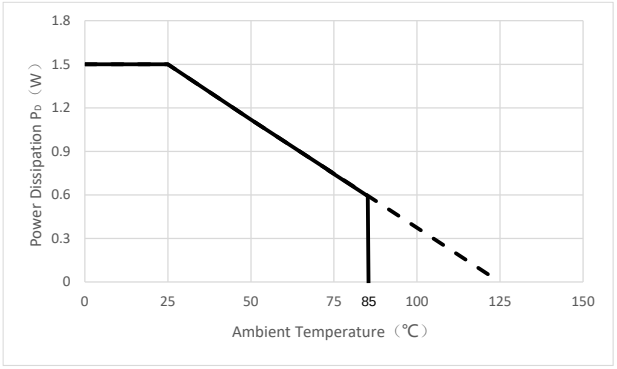
Bit	Name	Default	Type	Description
7	tsd	0	R	Thermal Shutdown Status: **0b:** Normal operation **1b:** A Thermal Shutdown event detected
6	vsys_uvlo	0	R	VSYS Under-Voltage-Lock-Out Status: **0b:** Normal operation **1b:** Indicates that the VSYS power fell below the UVLO input threshold.
5:4	Rev.	00	R	Reserved
3	ldo4_ocp	0	R	LDO4 OCP Status: **0b:** Clear **1b:** Over current event detected on the LDO4 output while LDO4 is been commanded to be enabled.
2	ldo3_ocp	0	R	LDO3 OCP Status: **0b:** Clear **1b:** Over current event detected on the LDO3 output while LDO3 is been commanded to be enabled.
1	ldo2_ocp	0	R	LDO2 OCP Status: **0b:** Clear **1b:** Over current event detected on the LDO2 output while LDO2 is been commanded to be enabled.
0	ldo1_ocp	0	R	LDO1 OCP Status: **0b:** Clear **1b:** Over current event detected on the LDO1 output while LDO1 is been commanded to be enabled.

Absolute Maximum Ratings

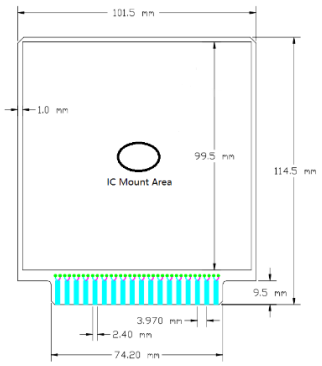
Symbol	Parameters (Items)	Value	Unit
V_{POWER}	V_{SYS}, V_{IN1}, V_{IN2}, V_{IN34} Pins Voltage	-0.3 to 6	V
V_{OUT}	$V_{LDO1\sim4}$ Pins Voltage	-0.3 to V_{INX}+0.3	
$V_{CONTROL}$	SDA, SCL and RESET_N Pins Voltage	-0.3 to 6	V
P_D (1)(2)	Maximum Power Consumption, T_A = 25°C	1500	mW
$R_{\theta JA}$ (1)	Thermal Resistance, Junction−to−Ambient, T_A = 25°C	67	°C/W
T_J	Operating Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SLOD}	Lead Temperature (Soldering, 10 sec)	300	°C
V_{ESD} (3)	HBM	±2000	V
	CDM	±1000	V

Note (1): P_D and $R_{\theta JA}$ are measured under natural convection (still air) at T_A = 25°C with the component mounted on 101.5*114.5mm FR-4, 4layer, Top and Bottom layer 1.5oz, both two inner layer 1oz. Meet JEDEC (JESD51-9) standard.

Note (2): Recommended operating conditions are only used to limit the reasonable use range of the single condition of the product, and the circuit use must comply with other instructions in the manual. For parameter performance indicators, please refer to the EC table and the test condition specification in the table.



Power Dissipation



Measurement Board pattern

Note (3): This device series incorporates ESD protection and is tested by the following methods:

HBM tested per JEDEC JS-001

CDM tested per JEDEC JS-002

Recommended Power Delivery Network for PCB

Channel	Inductance	Resistance	Spec Selection criteria
VIN1	< 16nH	≤ 33mohm	W > 1.2mm; L < 20mm; 1oz
LDO1	< 16nH	≤ 33mohm	W > 1.2mm; L < 20mm; 1oz
VIN2/VIN34	< 19nH	≤ 20mohm	W > 0.5mm; L < 20mm; 1oz
LDO2~4	< 19nH	≤ 20mohm	W > 0.5mm; L < 20mm; 1oz
VSYS	< 20nH	≤ 20mohm	W > 0.5mm; L < 20mm; 1oz

Note *: The ground of the chip and capacitor do not need to be isolated.

Recommended Operating Conditions

Symbol	Parameters		Rating	Unit
V_{VSYS}	Supply Input Voltage		2.5 to 5.5	V
V_{VIN1}	Supply Input Voltage		0.6 to 2.0	V
V_{VIN2}	Supply Input Voltage		1.8 to 5.5	V
V_{VIN34}	Supply Input Voltage		1.8 to 5.5	V
I_{LDO1}	Output Current (1500mA LDO)		0 to 1500	mA
$I_{LDO2\sim4}$	Output Current (400mA LDO)		0 to 400	mA
T_A	Operating Ambient Temperature		-40 to 85	ºC
$R_{\_I2C\_PU}$	I2C pull up resistance	1.2V VDD_IO	1.4 to 5.1	KΩ
		1.8V VDD_IO	1.4 to 6.8	
$R_{\_RESET\_N\_PU}$	RESET_N pull up resistance if need		10 to 1000	
C_{VIN1}	Effective Input Ceramic Capacitor Value	I_{OUT} ≤ 750mA	2 to 47	uF
		I_{OUT} > 750mA	3 to 47	
C_{VSYS}/C_{VIN2}/ C_{VIN34}	Effective Input Ceramic Capacitor Value	I_{OUT} ≤ 400mA	0.68 to 10	uF
C_{LDO1}	Effective Output Ceramic Capacitor Value (1500mA LDO)	I_{OUT} ≤ 750mA	2 to 22	uF
		I_{OUT} > 750mA	4.7 to 47	
$C_{LDO2\sim4}$	Effective Output Ceramic Capacitor Value (400mA LDO)	I_{OUT} ≤ 400mA	0.68 to 10	uF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)		5 to 100	mΩ

Electrical Characteristics

(Unless otherwise noted, V_{VIN1} = V_{LDO1} + 0.25V, V_{VSYS} = (V_{LDO1} + 1.6V) or 2.5V whichever greater, I_{OUT} = 1mA, C_{VIN1} = 10μF, $C_{VSYS/VIN2/VIN34}$ = 1uF, C_{LDO1} = 10μF, $C_{LDO2/3/4}$ = 1μF, T_A = -40°C~85°C. Typical values are at T_A = 25ºC, V_{VSYS} = 3.8V; V_{VIN1} = 1.45V; $V_{VIN2/34}$ = 3.8V; V_{LDO1} = 1.2V, $V_{LDO2/3/4}$ = 2.8V.)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{VIN1}	VIN1 Input Voltage Range	V_{VIN1} > (V_{LDO1} + V_{DROP_LDO1})	0.6		2.0	V
V_{VIN2} (4), V_{VIN34} (4),	VIN2, VIN34 Input Voltage Range		1.8		5.5	V
V_{VSYS} (5)	VSYS Voltage Range	V_{LDO1} + 1.6V, V_{VSYS} ≥ 2.5V	2.5		5.5	V
V_{UVLO_VSYS}	VSYS Under-voltage Lock-out	Rising, T_A = 25 ºC	2.1	2.3	2.5	V
		Falling, T_A = 25 ºC	1.9	2.1	2.3	V
I_{Q_ON}(8)	V_{VSYS} Current When all LDO Enabled	V_{RESET_N} = High and Enable all LDO by I^2C, No Load	30	60	120	μA
I_{Q_OFF}(8)(9)	V_{VSYS} Current When all LDO Disabled (System shutdown)	V_{RESET_N} = 0V	0.01	1.5	3	μA
I_{Q_STB}(8) (9)	V_{VSYS} Current When all LDO Disabled (System standby)	V_{RESET_N} = V_{VSYS} and Disable all LDO by I^2C	10	15	45	μA
I_{EN}	RESET_N Pull Down Current	V_{RESET_N} = 5.5V, V_{VSYS} = 5.5V	0.01	0.3	1	μA
V_{ENH}	RESET_N Input Voltage High		0.84			V
V_{ENL}	RESET_N Input Voltage Low				0.4	V
V_{I2CH}(10)	SCL/SDA Input Voltage High		0.84			V
V_{I2CL}	SCL/SDA Input Voltage Low				0.4	V
V_{OL}	SDA Logic Low Output	3mA Sink			0.4	V
T_{TSD}(6)	Thermal Shutdown Threshold	T_J Rising	135	150	165	°C
T_{HYS_TSD}(6)	Thermal Shutdown Hysteresis	T_J Falling from Shutdown		25		°C

Electrical Characteristics (Continued)

1500mA LDO1

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{OUT1}	Output range		0.496		1.8	V
V_{LDO1}	Output Voltage	I_{OUT} = 1mA~1500mA, T_A = 25ºC, V_{OUT} > 0.8V	-1.0		1.0	%
		I_{OUT} = 10mA, T_A = -40°C~85°C V_{OUT} > 0.8V	-1.5		1.5	%
		I_{OUT} = 10mA, T_A = -40°C~85°C V_{OUT} ≤ 0.8V	-12		12	mV
V_{DROP_LDO1}[(7)]	Dropout Voltage	V_{SYS} > 3V, I_{OUT} = 500mA, V_{OUT} = 1.2V		30	50	mV
		V_{SYS} > 3V, I_{OUT} = 1500mA, V_{OUT} = 1.2V		100	180	
$I_{Q\_LDO1\_VSYS}$	V_{VSYS} Current When Only LDO1 Enabled	Only LDO1 on, no load. Current on VSYS		50	90	uA
$I_{Q\_LDO1\_VIN}$	V_{VIN1} Current When Only LDO1 Enabled	Only LDO1 on, No Load. Current on VIN1		10	20	uA
$I_{Q\_OFF\_LDO1}$	V_{VIN1} Current When LDO1 Disabled	V_{VSYS} = 3.8V, V_{VIN1} = 1.45V, V_{RESET_N} = 0V or Shutdown by I^2C		0.1	1	uA
I_{OUT_LDO1}	Output Current		1500			mA
I_{LIM_LDO1}	Current Limit	Default Ilimit Register Value, T_A = 25ºC	1600	2500	3750	mA
I_{SHORT_LDO1}	Short Current Limit	Default Ilimit Register Value V_{LDO1} = 0V, T_A = 25ºC	350	550	1000	mA
Reg_{LOAD_LDO1}	Load Regulation	1mA ≤ I_{OUT} ≤ 1500mA		0.002	0.005	%/mA
Reg_{LINE_LDO1}	V_{VIN1} Line Regulation	V_{LDO1} + 0.25V ≤ V_{VIN1} ≤ 2V (I_{OUT} = 1mA)		0.01	0.5	%/V
	V_{VSYS} Line Regulation	2.5V or (V_{LDO1} + 1.6V) Whichever Greater < V_{VSYS} < 5.5V, V_{VIN1} = V_{LDO1} + 0.25V, I_{OUT} = 1mA		0.01	0.2	%/V
e_{N_LDO1}[(6)]	Output Noise	V_{VIN1} = 1.45V, V_{OUT} = 1.2V, V_{VSYS} = 3.8V, I_{OUT}= 30mA, f = 10Hz to 100kHz		30	100	μV_{RMS}
R_{LOW_LDO1}	Output Auto Discharge Resistance at Off State	V_{RESET_N} = 0V, or Shutdown by I^2C, I_{OUT} = 10mA, T_A = 25ºC, V_{SYS} = 3.8V, VIN1=1.5V	20	50	80	Ω

Electrical Characteristics(Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$PSRR_{LDO1}$[6]	Ripple Rejection (V_{VIN1} to V_{OUT1})	V_{IN} to V_{OUT}, f = 100Hz, Ripple 0.2Vp-p, I_{OUT} = 30mA, V_{OUT} = 1.2V, V_{VSYS} = 3.8V	70	85		dB
		V_{IN} to V_{OUT}, f = 1kHz, Ripple 0.2Vp-p, I_{OUT} = 30mA, V_{OUT} = 1.2V, V_{VSYS} = 3.8V	65	80		
		V_{IN} to V_{OUT}, f = 10kHz, Ripple 0.2Vp-p, I_{OUT} = 30mA, V_{OUT} = 1.2V, V_{VSYS} = 3.8V	46	60		
		V_{IN} to V_{OUT}, f = 100kHz, Ripple 0.2Vp-p, I_{OUT} = 30mA, V_{OUT} = 1.2V, V_{VSYS} = 3.8V	30	40		
		V_{IN} to V_{OUT}, f = 1MHz, Ripple 0.2Vp-p, I_{OUT} = 30mA, V_{OUT} = 1.2V, V_{VSYS} = 3.8V	26	42		
	Ripple Rejection (V_{VSYS} to V_{OUT1})	V_{VSYS} to V_{LDO1}, f = 1kHz, Ripple 0.2Vp-p, I_{OUT} = 30mA, V_{OUT} = 1.2V, V_{VSYS} = 3.8V	70	85		
		V_{VSYS} to V_{LDO1}, f = 1MHz, Ripple 0.2Vp-p, I_{OUT} = 30mA, V_{OUT} = 1.2V, V_{VSYS} = 3.8V	30	40		
V_{TRLN_LDO1}[6]	Line Transient (V_{VIN1} to V_{OUT1})	V_{VIN1} = V_{LDO1} + 0.3V to V_{LDO1} + 1.5V ≤ 2V in 10us, I_{OUT} = 1mA, T_A = 25ºC		5	10	mV
		V_{VIN1} = V_{LDO1} + 1.5V to V_{LDO1} + 0.3V ≤ 2V in 10us, I_{OUT} = 1mA, T_A = 25ºC		5	10	
	Line Transient (V_{VSYS} to V_{OUT1})	V_{SYS} = V_{OUT} + 1.6 or 2.5V to V_{SYS} + 1V, in 10us, T_A = 25°C		5	10	
		V_{SYS} = V_{SYS} + 1V to V_{OUT} + 1.6 or 2.5V, in 10us, T_A = 25°C		5	10	
V_{TRLD_+LDO1}[6]	Load Transient	I_{OUT} = 1mA to 1500mA in 10us V_{VIN1} = V_{LDO1} + 0.5V ≤ 2V, T_A = 25ºC		50	100	mV
		I_{OUT} = 1500mA to 1mA in 10us V_{VIN1} = V_{LDO1} + 0.5V ≤ 2V, T_A = 25ºC		50	100	
t_{ON_LDO1}[6][11]	Turn-On Time	V_{OUT} ≥ 0.8V From assertion of enable to V_{OUT} = 95%$V_{LDO1(NOM)}$		250	900	µs

Electrical Characteristics (Continued)

400mA LDO2

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{OUT2}	Output Range		1.2		3.75	V
V_{DROP_LDO2}[7]	Dropout Voltage	I_{OUT} = 400mA, V_{LDO2} = 1.5V		220	330	mV
		I_{OUT} = 400mA, V_{LDO2} = 1.8V		170	255	
		I_{OUT} = 400mA, V_{LDO2} = 2.2V		140	210	
		I_{OUT} = 400mA, V_{LDO2} = 2.8V		110	165	
		I_{OUT} = 400mA, V_{LDO2} = 3.3V		100	150	
		I_{OUT} = 400mA, V_{LDO2} = 3.4V		100	150	
V_{LDO2}	Regulated Output Voltage	I_{OUT} = 1mA~400mA, T_A = 25°C	-2		2	%
		I_{OUT} = 1mA~400mA, T_A = -40°C~85°C	-2		2	
Reg_{LINE_LDO2}	Output Voltage Line Regulation	V_{LDO2} = 2.8V 3.3V ≤ V_{VIN2} ≤ 5.5V, I_{OUT} = 10mA (ΔV_{LDO2} / ΔV_{VINX} / V_{LDO2})		0.01	0.2	%/V
Reg_{LOAD_LDO2}	Output Voltage Load Regulation	I_{OUT} from 1mA to 400mA ΔV_{LDO2}		0.002	0.005	%/mA
V_{TRLN_LDO2}[6]	Line Transient (The absolute value of the output change) (V_{VIN2} to V_{OUT2})	V_{LDO2} = 2.8V, I_{OUT} = 1mA, V_{VIN2} = 3.8V to 4.8V in 10us, T_A = 25°C		5	20	mV
		V_{LDO2} = 2.8V, I_{OUT} = 1mA, VIN2 = 4.8V to 3.8V in 10us, T_A=25°C		5	20	
		I_{OUT} = 1mA, V_{VIN2} = V_{OUT} + 1V to V_{OUT} + 2V at 10us/V, T_A = 25°C		5	35	
		I_{OUT} = 1mA, V_{VIN2} = V_{OUT} + 2V to V_{OUT} + 1V at 10us/V, T_A=25°C		5	35	
	Line Transient (The absolute value of the output change) (V_{VSYS} to V_{OUT2})	I_{OUT} = 1mA, V_{SYS} = 3.8V to 4.8V in 10us, T_A = 25°C		5	10	
		I_{OUT} = 1mA, V_{SYS} = 4.8V to 3.8V in 10us, T_A = 25°C		5	10	
V_{TRLD_LDO2}[6]	Load Transient (The absolute value of the output change)	V_{LDO2} = 2.8V, V_{VSYS} = 3.8V, I_{OUT} from 1mA to 400mA in 10us, T_A = 25°C		50	100	mV
		V_{LDO2} = 2.8V, V_{VSYS} = 3.8V, I_{OUT} from 400mA to 1mA in 10us, T_A = 25°C		30	60	
$I_{Q\_LDO2\_VSYS}$	V_{VSYS} Current When Only LDO2 Enabled	Only LDO2 on, no load. Current on VSYS		20	60	uA

Electrical Characteristics (Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{Q\_LDO2\_VIN}$	V_{VIN2} Current When Only LDO2 Enabled	Only LDO2, No Load. Current on VIN2		16	30	uA
$I_{Q\_OFF\_LDO2}$	V_{VIN2} Current When LDO2 Disabled	V_{VSYS} = V_{VIN2} = 3.8V, V_{RESET_N} = 0V or Shutdown by I²C		0.1	1	uA
I_{OUT_LDO2}	Output Current		400			mA
I_{LMT_LDO2}	Over Current Limit	Default Ilimit Register Value, V_{VIN2} = V_{LDO2_VSET} + 1V, T_A = 25ºC	400	600	900	mA
I_{SHORT_LDO2}	Short Current Limit	Default Ilimit Register Value, V_{LDO2} = 0V, T_A = 25ºC	20	50	100	mA
e_N[6]	Output Noise	10Hz to 100kHz, I_{OUT} = 30mA, V_{LDO2} = 2.8V, V_{VSYS} = V_{VIN2} = 3.8V, C_{LDO2} = 1μF, T_A = 25°C		10	100	μV_{RMS}
$PSRR_{LDO2}$[6]	Power Supply Rejection Ratio (V_{VIN2} to V_{OUT2})	f = 100Hz, C_{LDO2} = 1μF, I_{OUT} = 0.1A, V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	66	82		dB
		f = 1kHz, C_{LDO2} = 1μF, I_{OUT} = 0.1A, V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	75	90		
		f = 10kHz, C_{LDO2} = 1μF, I_{OUT} = 0.1A, V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	65	80		
		f = 100kHz, C_{LDO2} = 1μF, I_{OUT} = 0.1A, V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	46	60		
		f = 1MHz, C_{LDO2} = 1μF, I_{OUT} = 0.1A, V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	35	45		
	Power Supply Rejection Ratio (V_{VSYS} to V_{OUT2})	V_{VSYS} to V_{LDO2}, f = 1kHz, C_{LDO2} = 1μF, I_{OUT} = 100mA V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	80	105		
		V_{VSYS} to V_{LDO2}, f = 1MHz, C_{LDO2} = 1μF, I_{OUT} = 100mA V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	46	60		
R_{LOW_LDO2}	Output Resistance of Auto Discharge at Off State	V_{SYS} = VIN2 = 3.8V, V_{RESET_N} = 0V, or Shutdown by I²C, I_{OUT} = 10mA, T_A = 25ºC	20	50	80	Ω
t_{ON_LDO2}[6][11]	Output Turn-on Delay Time	From Enable to V_{OUT} = 95% of V_{OUT}(NOM)		250	900	us

Electrical Characteristics (Continued)

400mA LDO3/LDO4

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{OUT3/4}$	Output range		1.2		3.75	V
$V_{DROP\_LDO3/4}$[7]	Dropout Voltage	I_{OUT} = 400mA, $V_{LDO3/4}$ = 1.5V		220	330	mV
		I_{OUT} = 400mA, $V_{LDO3/4}$ = 1.8V		170	255	
		I_{OUT} = 400mA, $V_{LDO3/4}$ = 2.2V		140	210	
		I_{OUT} = 400mA, $V_{LDO3/4}$ = 2.8V		110	165	
		I_{OUT} = 400mA, $V_{LDO3/4}$ = 3.3V		100	150	
		I_{OUT} = 400mA, $V_{LDO3/4}$ = 3.4V		100	150	
$V_{LDO3/4}$	Regulated Output Voltage	I_{OUT} = 1mA~400mA, T_A = 25°C	-2		2	%
		I_{OUT} = 1mA, T_A = -40°C~85°C	-2		2	
$Reg_{LINE\_LDO3/4}$	Output Voltage Line Regulation	$V_{LDO3/4}$ = 2.8V 3.3V ≤ V_{VIN34} ≤ 5.5V, I_{OUT} = 10mA ($\Delta V_{LDO3/4}$ / ΔV_{VIN34} / $V_{LDO3/4}$)		0.01	0.2	%/V
$Reg_{LOAD\_LDO3/4}$	Output Voltage Load Regulation	I_{OUT} from 1mA to 400mA $\Delta V_{LDO3/4}$		0.002	0.005	%/mA
$V_{TRLN\_LDO3/4}$[6]	Line Transient (The absolute value of the output change) (V_{VIN34} to $V_{OUT3/4}$)	$V_{LDO3/4}$ = 2.8V, I_{OUT} = 1mA, V_{VIN34} = 3.8V to 4.8V in 10us, T_A = 25°C		5	20	mV
		$V_{LDO3/4}$ = 2.8V, I_{OUT} = 1mA, V_{VIN34} = 4.8V to 3.8V in 10us, T_A = 25°C		5	20	
		I_{OUT} = 1mA, V_{VIN34} = V_{OUT} + 1V to V_{OUT} + 2V at 10us/V, T_A = 25°C		5	35	
		I_{OUT} = 1mA, V_{VIN34} = V_{OUT} + 2V to V_{OUT} + 1V at 10us/V, T_A = 25°C		5	35	
	Line Transient (The absolute value of the output change) (V_{VSYS} to $V_{OUT3/4}$)	I_{OUT} = 1mA, V_{SYS} = 3.8V to 4.8V in 10us, T_A = 25°C		5	10	
		I_{OUT} = 1mA, V_{SYS} = 4.8V to 3.8V in 10us, T_A = 25°C		5	10	
$V_{TRLD\_LDO3/4}$[6]	Load Transient (The absolute value of the output change)	$V_{LDO3/4}$ = 2.8V, V_{VIN34} = 3.8V, I_{OUT} from 1mA to 400mA in 10us, T_A = 25°C		50	100	mV
		$V_{LDO3/4}$ = 2.8V, V_{VIN34} = 3.8V, I_{OUT} from 400mA to 1mA in 10us, T_A = 25°C		30	60	
$I_{Q\_LDO3/4\_VSYS}$	V_{VSYS} Current When Only LDO3 or LDO4 Enabled	Only LDO3 or LDO4 on, No Load. Current on VSYS		20	60	uA

Electrical Characteristics (Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{Q\_LDO3/4\_VIN}$	V_{VIN34} Current When Only LDO3 or LDO4 Enabled	Only LDO3 or LDO4 on, No Load. Current on VIN34		16	30	uA
$I_{Q\_OFF\_LDO3/4}$	V_{VIN34} Current When LDO3 and LDO4 Disabled	V_{VSYS} = $V_{VIN3/4}$ = 3.8V, V_{RESET_N} = 0V or Shutdown by I^2C		0.1	1	uA
$I_{OUT\_LDO3/4}$	Output Current		400			mA
$I_{LMT\_LDO3/4}$	Over Current Limit	Default Ilimit Register Value, V_{VIN34} = V_{LDOx_VSET} + 1V, T_A = 25ºC	400	600	900	mA
$I_{SHORT\_LDO3/4}$	Short Current Limit	Default Ilimit Register Value, $V_{LDO3/4}$ = 0V, T_A = 25ºC	20	50	100	mA
e_N[(6)]	Output Noise	10Hz to 100kHz, I_{OUT} = 30mA, $V_{LDO3/4}$ = 2.8V, V_{VSYS} = V_{VIN34} = 3.8V, $C_{LDO3\sim4}$ = 1μF, T_A = 25°C		10	100	μV_{RMS}
$PSRR_{\_LDO3/4}$[(6)]	Power Supply Rejection Ratio (V_{VIN34} to $V_{OUT3/4}$)	f = 100Hz, $C_{LDO3/4}$ = 1μF, I_{OUT} = 0.1A, V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	66	82		dB
		f = 1kHz, $C_{LDO3/4}$ = 1μF, I_{OUT} = 0.1A, V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	75	90		
		f = 10kHz, $C_{LDO3/4}$ = 1μF, I_{OUT} = 0.1A, V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	65	80		
		f = 100kHz, $C_{LDO3/4}$ = 1μF, I_{OUT} = 0.1A V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	46	60		
		f = 1MHz, $C_{LDO3/4}$ = 1μF, I_{OUT} = 0.1A, V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	35	45		
	Power Supply Rejection Ratio (V_{VSYS} to $V_{OUT3/4}$)	V_{VSYS} to $V_{LDO3/4}$, f = 1kHz, $C_{LDO3/4}$ = 1μF, I_{OUT} = 100mA V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	80	105		
		V_{VSYS} to $V_{LDO3/4}$, f = 1MHz, $C_{LDO3/4}$ = 1μF, I_{OUT} = 100mA V_{VSYS} = V_{LDOx_VSET} + 1V, T_A = 25°C	46	60		
$R_{LOW\_LDO3/4}$	Output Resistance of Auto Discharge at Off State	V_{SYS} = V_{IN34} = 3.8V, V_{RESET_N} = 0V, or Shutdown by I^2C, I_{OUT} = 10mA, T_A = 25 ºC	20	50	80	Ω
$t_{ON\_LDO3/4}$[(6)(11)]	Output Turn-on Delay Time	From Enable to V_{OUT} = 95% of V_{OUT}(NOM)		250	900	us

Note (4): Here V_{VINx} means internal circuit can work normal. If $V_{VINx} < V_{LDOx}$, Output voltage follow V_{VINx} (I_{OUT} = 1mA), circuit is safety.

Note (5): Here $V_{VSYS} > V_{UVLO\_VSYS}$ means internal control circuit can work normal. If $V_{VSYS} < 2.5V$ or $V_{VSYS} < V_{LDO1}+1.6V$, some performance parameters cannot be guaranteed.

Note (6): Guaranteed by design and characterization. not a FT item.

Note (7): V_{DROP_LDOx} FT test method: test the V_{LDOx} voltage at V_{LDOx_vset} + $V_{DROPMAX}$ with output current. Guaranteed by design and characterization except V_{OUT} = 1.8V and V_{OUT} = 2.8V, not FT items.

Note (8): Since the power on process of VSYS needs a large current, the BIAS should have a current driving capacity of more than 100mA.

Note (9): Please ensure individual LDO in the off state before vsys_en = 0 (0x03 LDO_EN Register: bit7).

Note (10): This parameter requires the I2C communication frequency not higher than 400KHz.

Note (11): T_{ON_LDOx} timing diagram shown as below (x = 1~4)

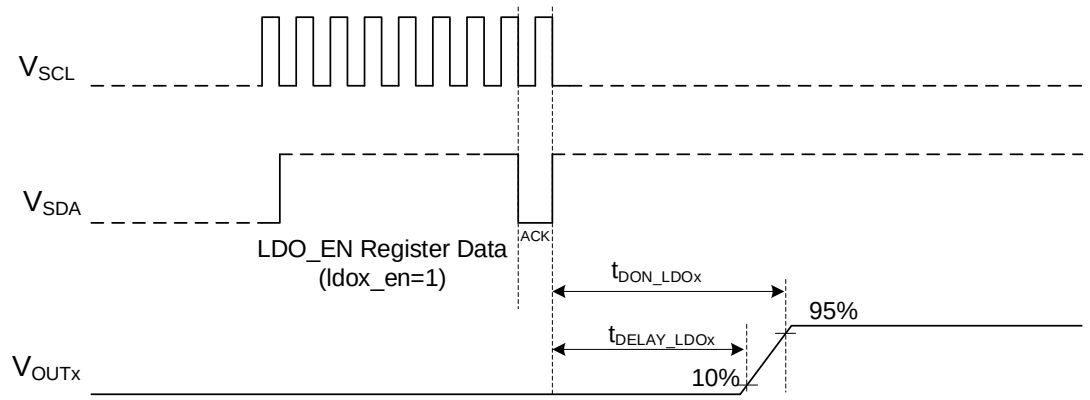


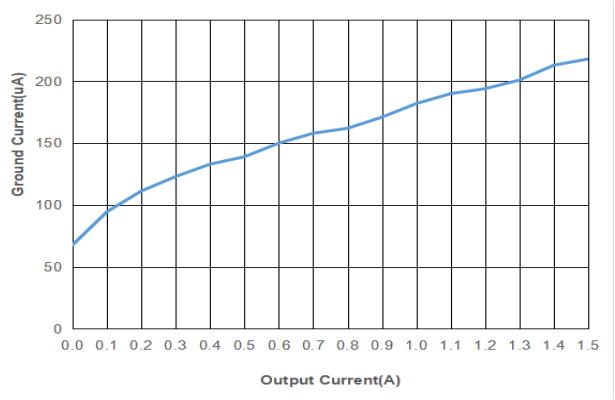
Figure 15.

Fast Mode I2C Specification

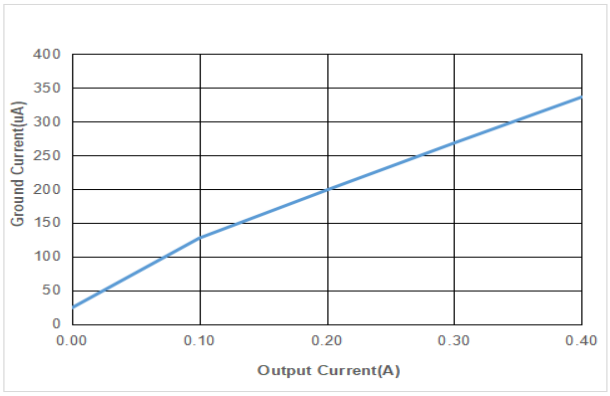
Symbol	Parameters	Min	Max	Unit
t1	SCL Clock Period, Recommended 50% Duty.	0.96		us
t2	Data in Set-Up Time to SCL High	100		ns
t3	Data Out Stable After SCL Low	100		ns
t4	SDA Low Set-Up Time to SCL Low (Start)	100		ns
t5	SDA High Hold Time after SCL High (Stop)	100		ns
t_R	SDA And SCL Rise Time		120	ns
t_F	SDA And SCL Fall Time		120	ns
C_i	SDA and SCL input capacitance	10		pF
C_b	The max load capacitance of SDA and SCL（I2C BUS）		100	pF

Typical Characteristics (continued)

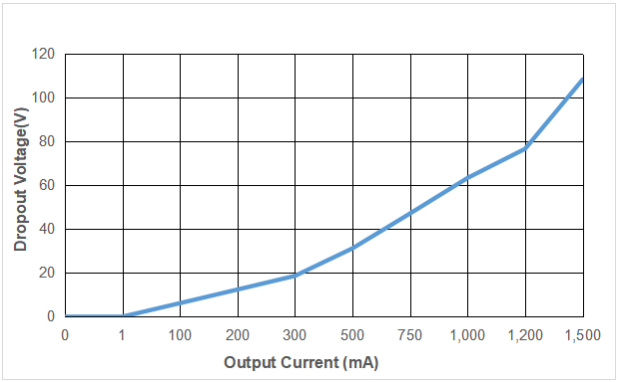
(Unless otherwise noted, V_{VIN1} = V_{LDO1} + 0.25V, V_{VSYS} = (V_{LDO1} + 1.6V) or 2.5V whichever greater, I_{OUT} = 1mA, C_{VIN1} = 10μF, $C_{VSYS/VIN2/VIN34}$ = 1uF, C_{LDO1} = 10μF, $C_{LDO2/3/4}$ = 1μF, T_A = -40°C~85°C. Typical values are at T_A = 25ºC, V_{VSYS} = 3.8V; V_{VIN1} = 1.45V; $V_{VIN2/34}$ = 3.8V; V_{LDO1} = 1.2V, $V_{LDO2/3/4}$ = 2.8V.)



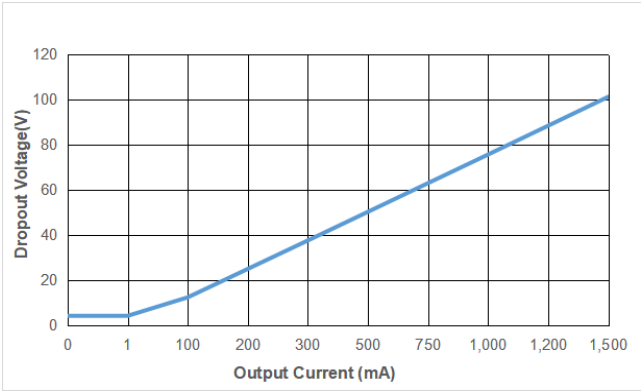
LDO1 Ground Current vs. Output Current



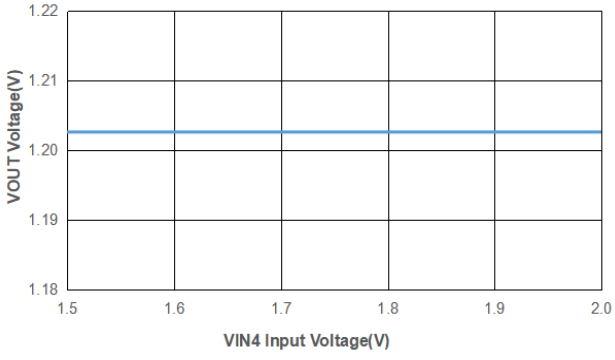
LDO2/3/4 Ground Current vs. Output Current



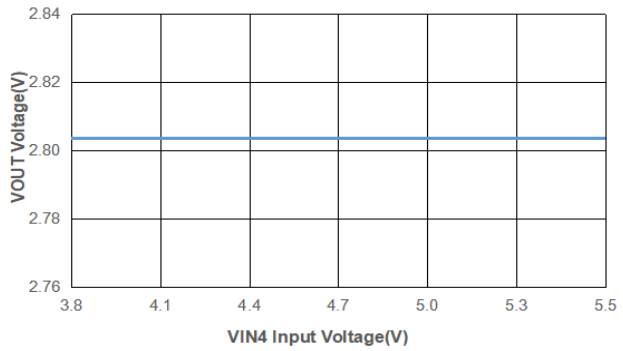
LDO1 Dropout Voltage vs. Output Current



LDO2/3/4 Dropout Voltage vs. Output Current



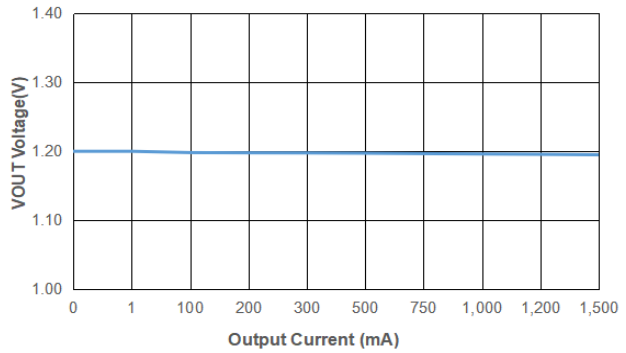
LDO1 Output Voltage vs. Input Voltage



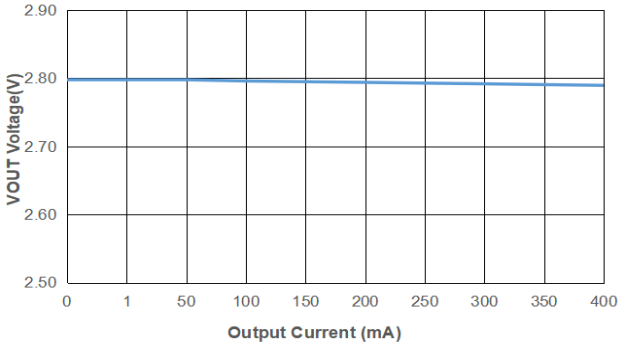
LDO2/3/4 Output Voltage vs. Input Voltage

Typical Characteristics (continued)

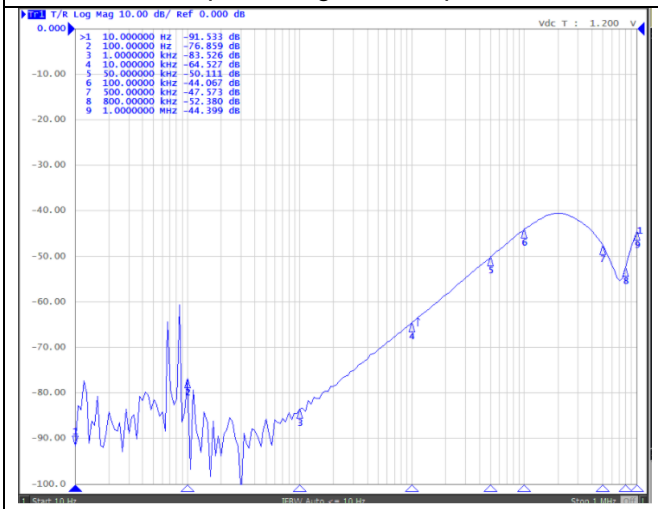
(Unless otherwise noted, V_{VIN1} = V_{LDO1} + 0.25V, V_{VSYS} = (V_{LDO1} + 1.6V) or 2.5V whichever greater, I_{OUT} = 1mA, C_{VIN1} = 10μF, $C_{VSYS/VIN2/VIN34}$ = 1uF, C_{LDO1} = 10μF, $C_{LDO2/3/4}$ = 1μF, T_A = -40°C~85°C. Typical values are at T_A = 25ºC, V_{VSYS} = 3.8V; V_{VIN1} = 1.45V; $V_{VIN2/34}$ = 3.8V; V_{LDO1} = 1.2V, $V_{LDO2/3/4}$ = 2.8V.)



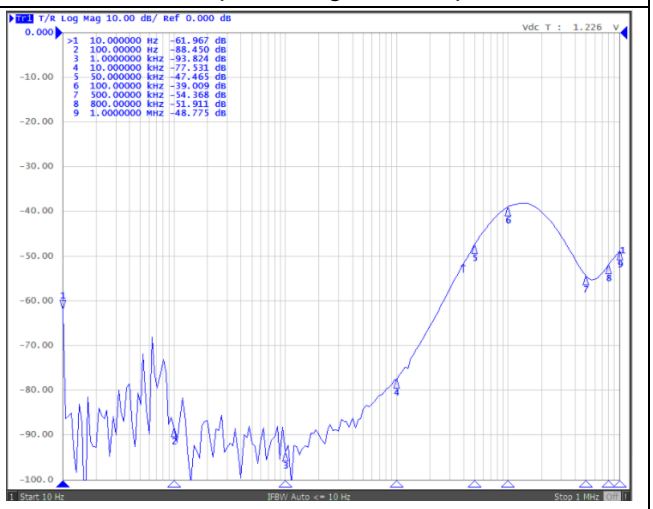
LDO1 Output Voltage vs. Output Current



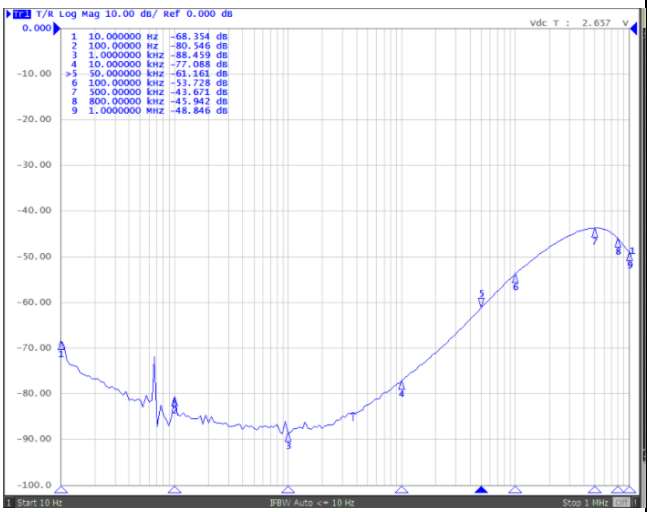
LDO2/3/4 Output Voltage vs. Output Current



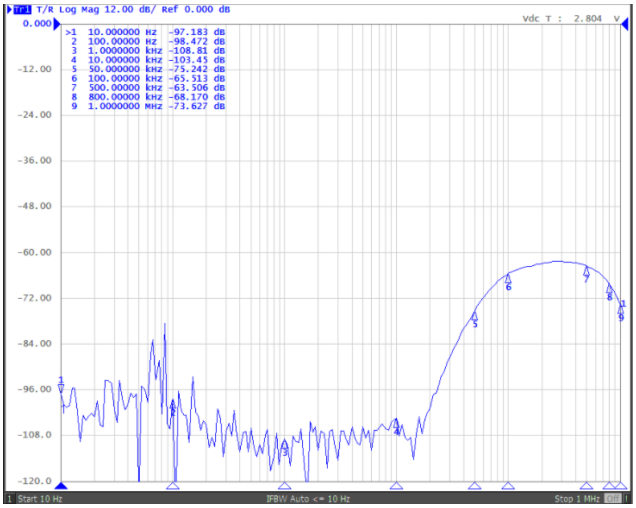
LDO1 PSRR-VIN-30mA



LDO1 PSRR-SYS-30mA



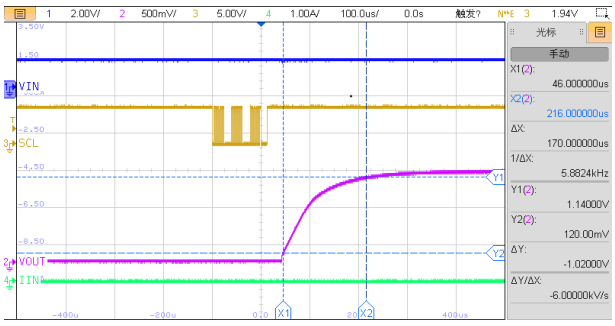
LDO2~4 PSRR-VIN-100mA



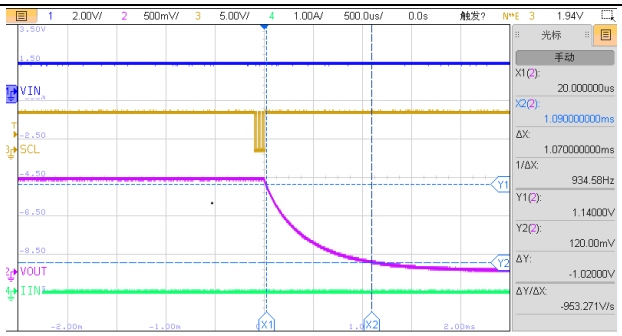
LDO2~4 PSRR-SYS-100mA

Typical Characteristics (continued)

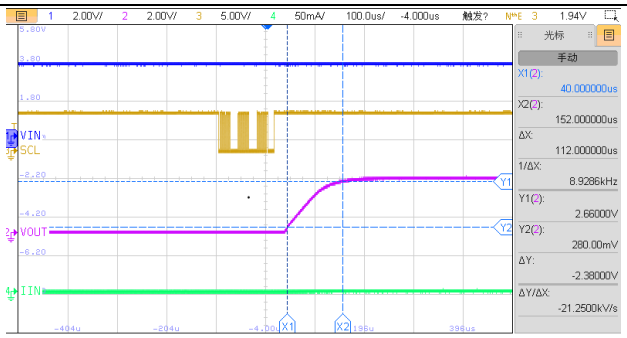
(Unless otherwise noted, V_{VIN1} = V_{LDO1} + 0.25V, V_{VSYS} = (V_{LDO1} + 1.6V) or 2.5V whichever greater, I_{OUT} = 1mA, C_{VIN1} = 10μF, $C_{VSYS/VIN2/VIN34}$ = 1uF, C_{LDO1} = 10μF, $C_{LDO2/3/4}$ = 1μF, T_A = -40°C~85°C. Typical values are at T_A = 25ºC, V_{VSYS} = 3.8V; V_{VIN1} = 1.45V; $V_{VIN2/34}$ = 3.8V; V_{LDO1} = 1.2V, $V_{LDO2/3/4}$ = 2.8V.)



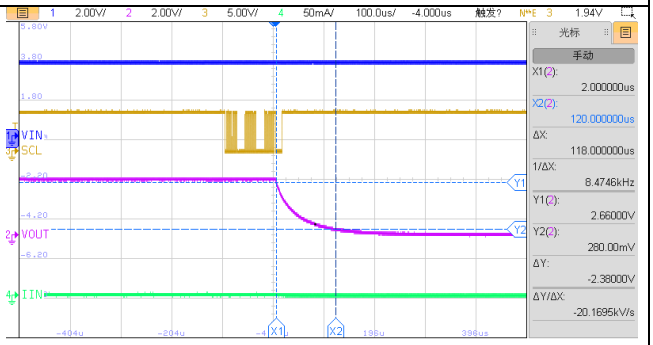
LDO1 Ton



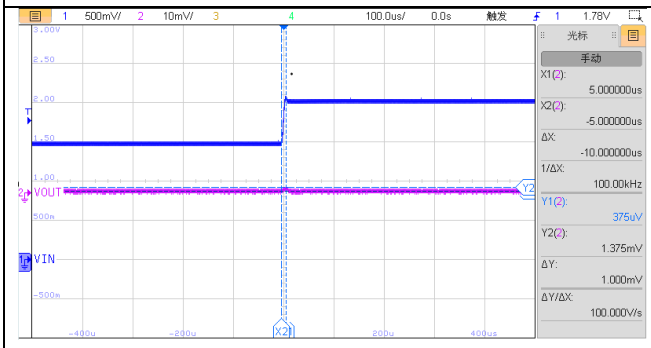
LDO1 Toff



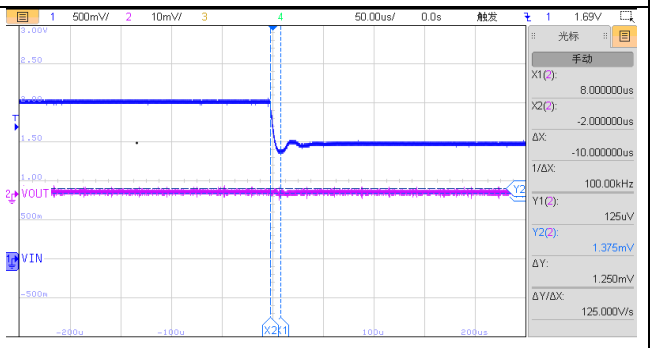
LDO2/3/4 Ton



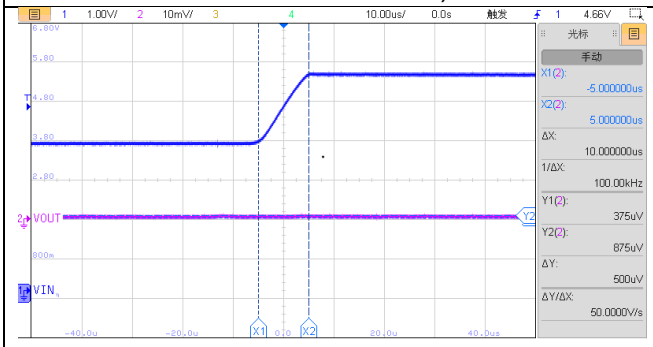
LDO2/3/4 Toff



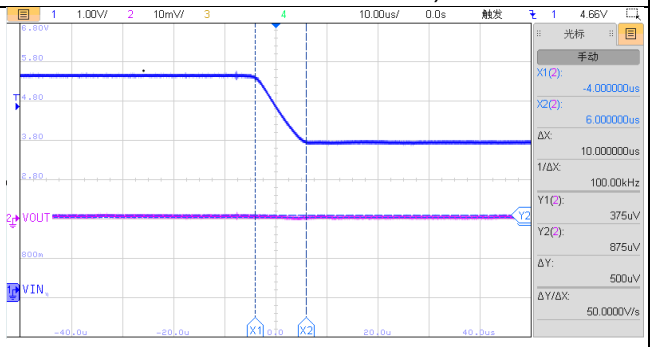
LDO1 Line Transient (I_{OUT} = 1mA, V_{IN1} = 1.45V to 2V)



LDO1 Line Transient (I_{OUT} = 1mA, V_{IN12} = 2V to 1.45V)



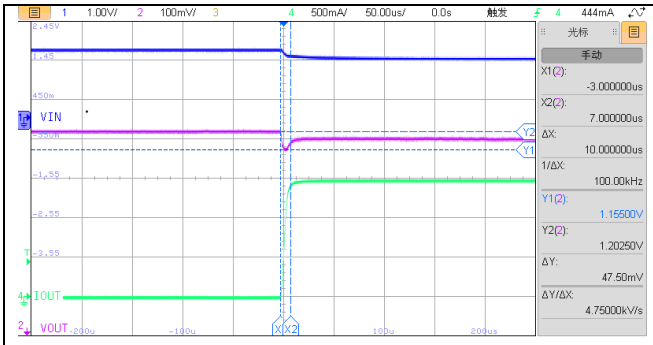
LDO2/3/4 Line Transient (I_{OUT} = 1mA, $V_{IN3~7}$ = 3.8V to 5.5V)



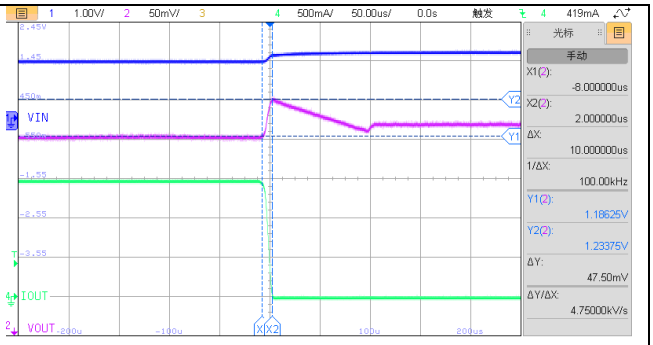
LDO2/3/4 Line Transient (I_{OUT} = 1mA, $V_{IN3~7}$ = 5.5V to 3.8V)

Typical Characteristics (continued)

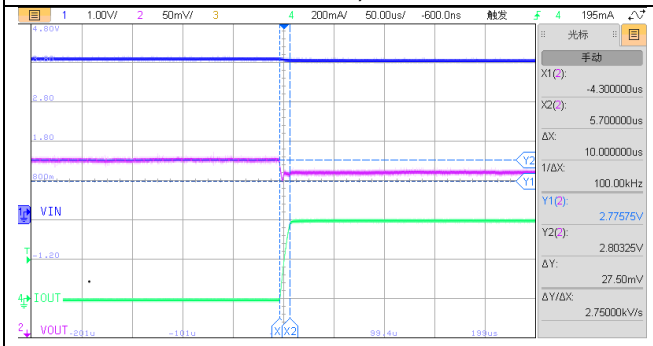
(Unless otherwise noted, V_{VIN1} = V_{LDO1} + 0.25V, V_{VSYS} = (V_{LDO1} + 1.6V) or 2.5V whichever greater, I_{OUT} = 1mA, C_{VIN1} = 10μF, $C_{VSYS/VIN2/VIN34}$ = 1uF, C_{LDO1} = 10μF, $C_{LDO2/3/4}$ = 1μF, T_A = -40°C~85°C. Typical values are at T_A = 25ºC, V_{VSYS} = 3.8V; V_{VIN1} = 1.45V; $V_{VIN2/34}$ = 3.8V; V_{LDO1} = 1.2V, $V_{LDO2/3/4}$ = 2.8V.)



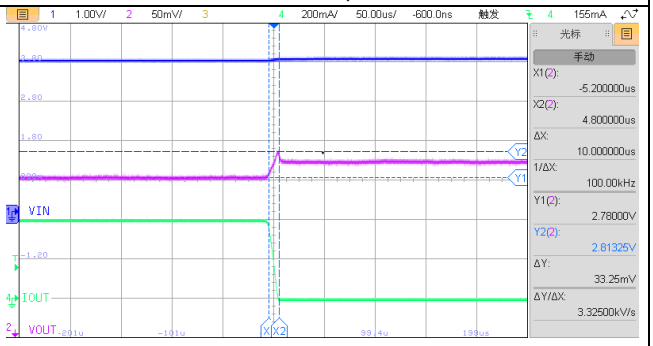
LDO1 Load Transient (V_{IN12} = 1.45V, I_{OUT} = 1mA to 1.5A)



LDO1 Load Transient (V_{IN12} = 1.45V, I_{OUT} = 1.5A to 1mA)



LDO2/3/4 Load Transient ($V_{IN2~4}$ = 3.8V, I_{OUT} = 1mA to 0.4A)



LDO2/3/4 Load Transient ($V_{IN2~4}$ = 3.8V, I_{OUT} = 0.4A to 1mA)

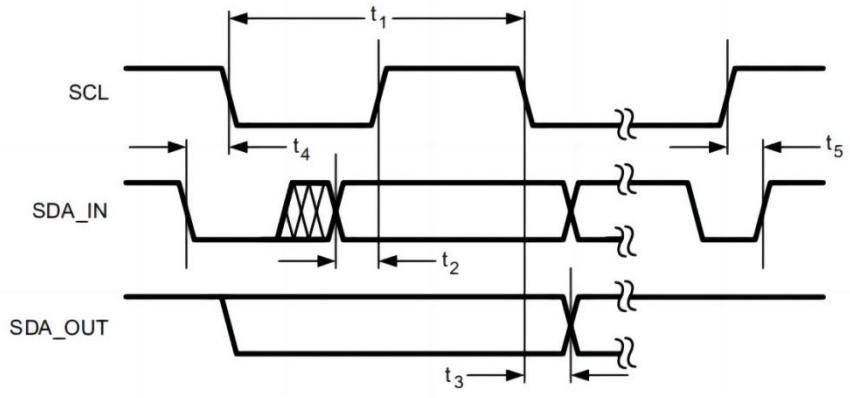
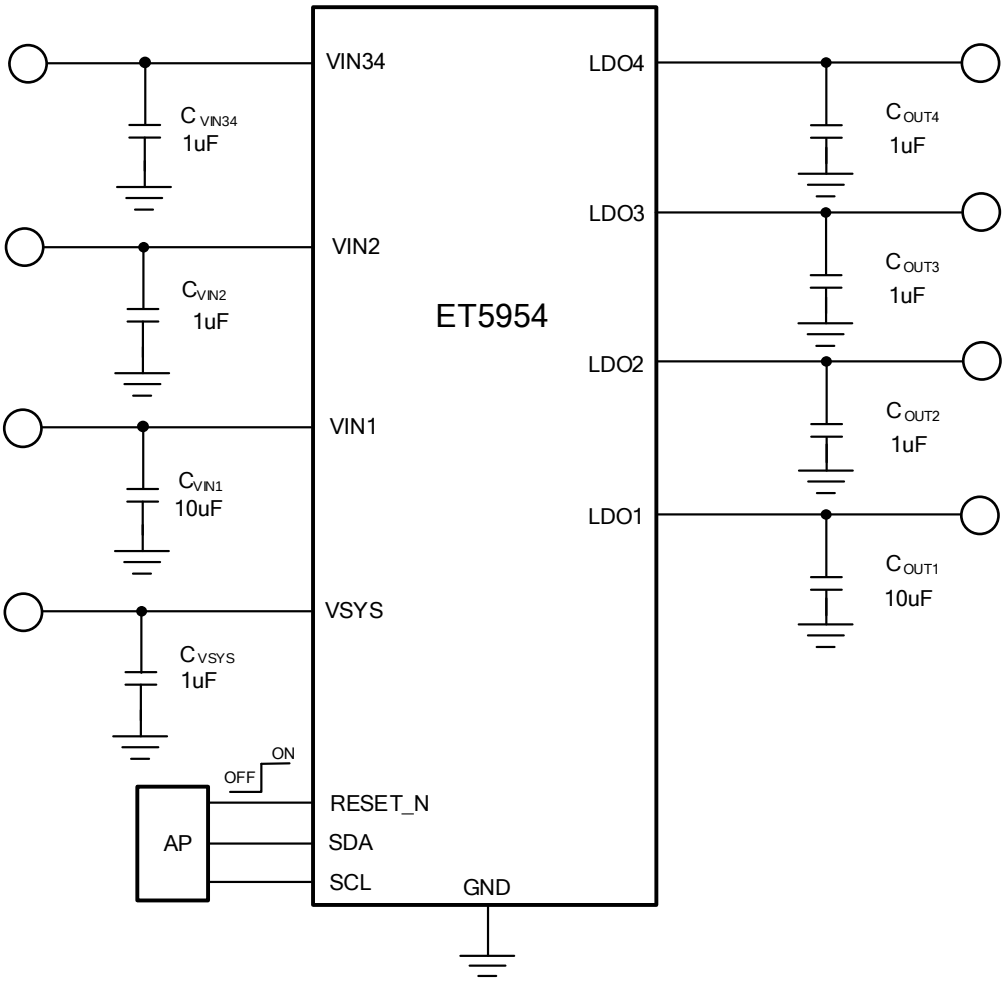
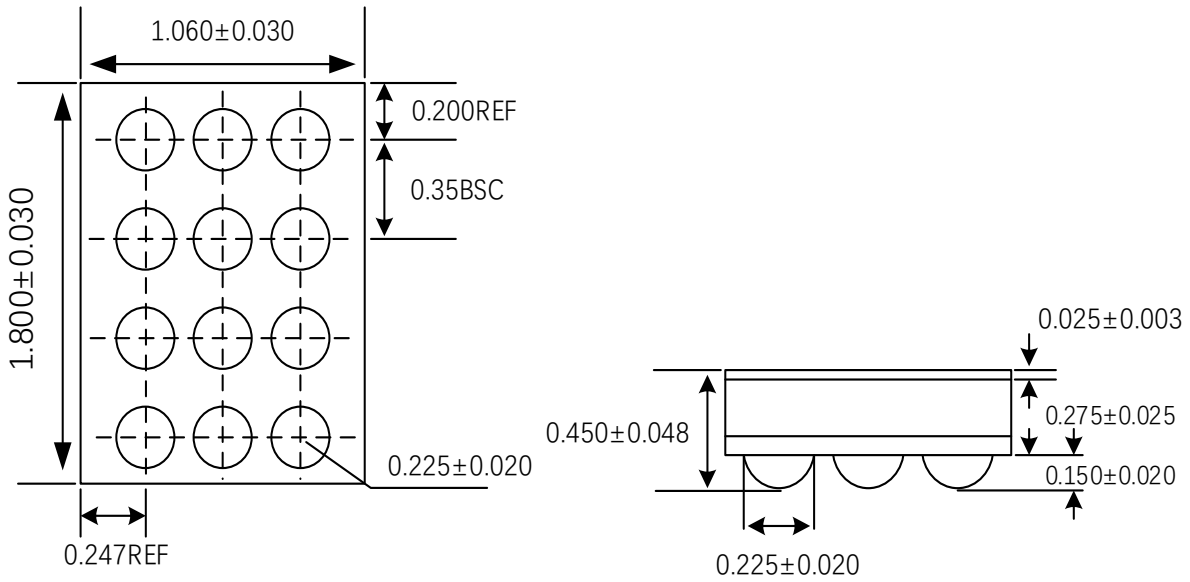


Figure 16. I²C-Compatible Interface Specifications

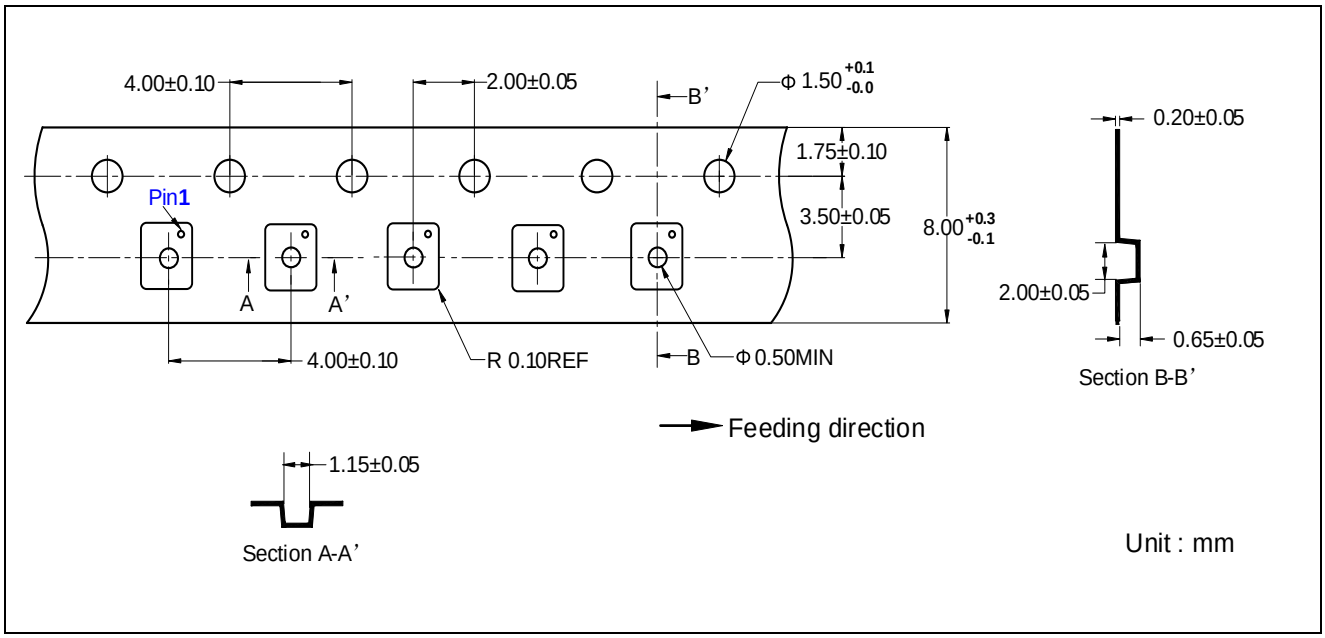
Application Circuits



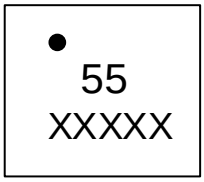
Package Dimension



Tape Information



Marking



55 = Part Number
XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2025-03-08	Preliminary Version	Ma Yan Yan	Liu Yi Guo	Liu Jia Ying
1.0	2025-06-02	Official Version	Zhang Zi Xuan	Yang Xiao Xu	Liu Jia Ying