

High-Current Over-Voltage Protectors with Adjustable OVLO and Input Voltage Detection

General Description

ET9546MV can disconnect the systems from its output pin(OUT) in case wrong input operating conditions are detected. The system is positive over-voltage protected up to 28V. The internal over-voltage threshold(OVLO) is 6.8V.

ET9546MV has internal Thermal-Shutdown Protection and Input Voltage detection.

The device is packaged in advanced full-Green compliant WLCSP12 package.

Features

- 4.5A Continuous Current Capability
- Typical R_{ON} : 33m Ω N-Channel MOSFET
- VIN Operating Range: 2.5V to 28V
- Internal Over-voltage Lockout: 6.8V
- Over-voltage-Protection Response Time: 50ns(TYP)
- Startup Debounce Time:15ms(TYP)
- Internal Thermal-Shutdown Protection
- Surge Immunity to $\pm 100V$
- ESD Protected: Human Body Model (JESD22-A114) All pins $\pm 2KV$ Pass
- Device and Package Information

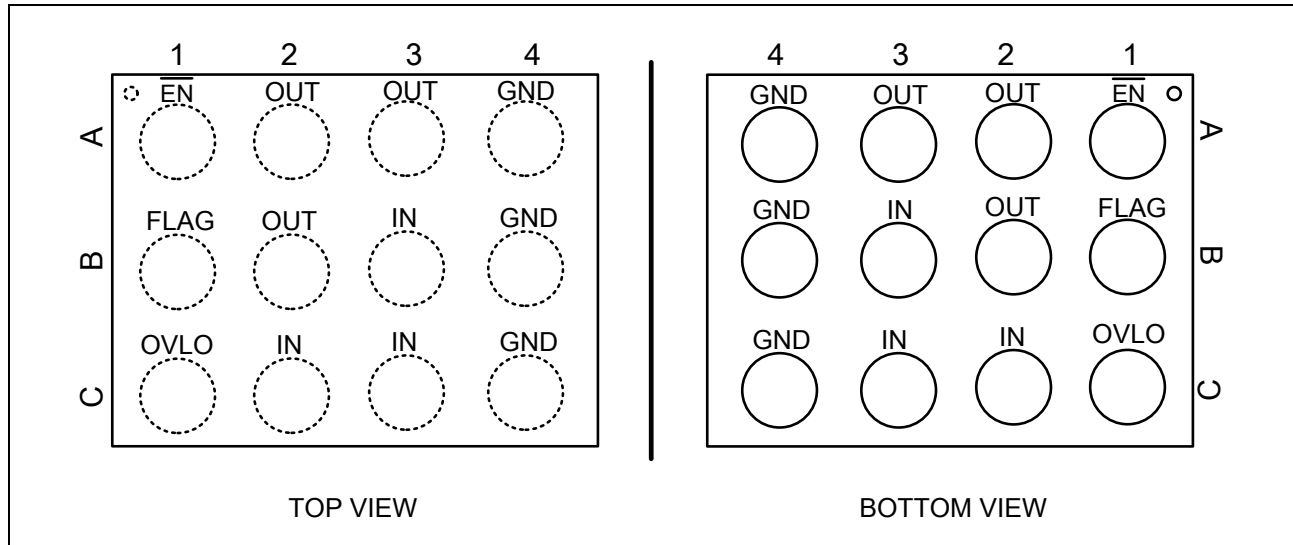
Part No.	Package	MSL
ET9546MV	WLCSP12 (1.55mm $\times$ 1.10mm 0.4mm pitch)	1

Application

- Smartphones, Tablet PC
- HDD, Storage and Solid State Memory Devices
- Portable Media Devices, Laptop & MID
- SLR Digital Cameras
- GPS and Navigation Equipment
- Industrial Handheld and Enterprise Equipment

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Pin Configuration

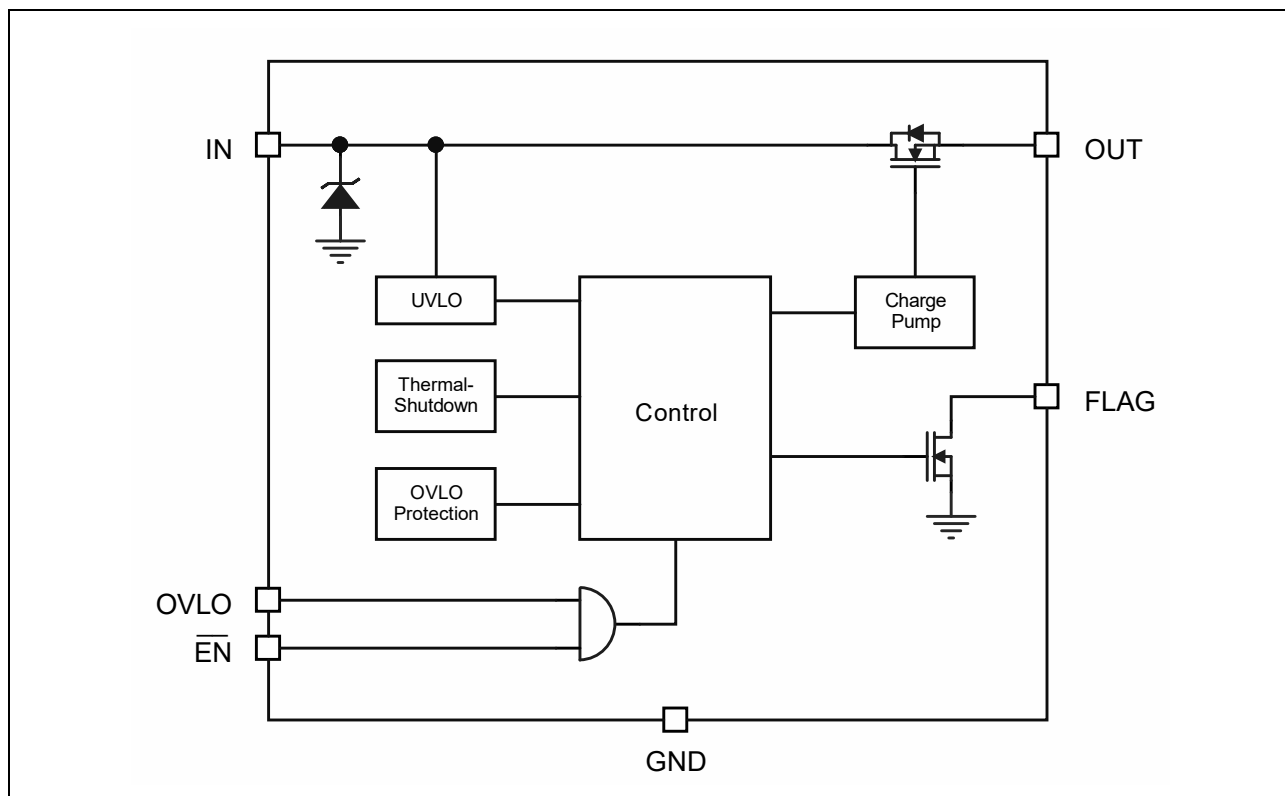


Pin Function

Pin	Name	Description		
A1	$\overline{\text{EN}}$	Device Enable. Active low.		
A2,A3,B2	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.		
A4,B4,C4	GND	Ground. Connect GND pins together for proper operation.		
B1	FLAG	Power status indicator	1	$V_{\text{IN}} < V_{\text{UVLO}}$ or $V_{\text{IN}} > V_{\text{OVLO}}$
			0	V_{IN} Stable
B3,C2,C3	IN	Voltage Input. Connect IN pins together for proper operation.		
C1	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.		

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Block Diagram



Functional Description

The OVP switch with over-voltage protection feature a low 33mΩ (TYP) on-resistance (R_{ON}) internal FET and protect low-voltage systems against voltage faults up to 28 V_{DC}. If $\overline{EN}$ is in the logic low state, when the input voltage(V_{IN}) exceeds 6.8V, the internal FET is quickly turned off to prevent damage to the protected downstream components and the flag pin will output logic high state. If $\overline{EN}$ is in the logic high state, the switch will be shutdown. If there is no input voltage at IN pin, the flag pin output logic high state.

When input (OVLO) is set lower than 0.2V. The over-voltage protection threshold is 6.8V.

The over-voltage protection threshold can also be adjusted by external resistors when input (OVLO) is set higher than 0.3V.

$$V_{IN_OVLO} = V_{OVLO_TH} \times (1 + R1/R2)$$

Note: $V_{OVLO_TH} = 1.2V(TYP)$

The internal FET turns off when the junction temperature exceeds +155°C (TYP). The device exits thermal shutdown after the junction temperature cools by 20°C (TYP).

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor 0.1μF or lager must be placed between the VIN and GND pins.

Output Capacitor

A 1μF or lager capacitor should be placed between the OUT and GND pins.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters			Min	Max	Unit
V _{IN}	VIN to GND			-0.3	29	V
V _{OUT}	VOUT to GND			-0.3	V _{IN} +0.3	V
V _{OVLO}	OVLO to GND			-0.3	7	V
V _{/EN}	$\overline{\text{EN}}$ to GND			-0.3	7	V
V _{FLAG}	FLAG to GND			-0.3	7	V
I _{SW1}	Maximum Continuous Current of switch IN-OUT				4.5	A
I _{SW2}	Maximum Peak Current of switch IN-OUT(10ms)				7	A
P _D	Power Dissipation at T _A = +25°C				1.0	W
R _{θJA} ⁽¹⁾	Thermal Resistance, Junction-to-Air				105	°C/W
T _{STG}	Storage Junction Temperature			-65	+150	°C
T _{SOLD}	Soldering Temperature (Reflow).				+260	°C
T _J	Junction Temperature			-40	+150	°C
T _A	Operating Temperature Range			-40	+85	°C
ESD	Electrostatic Discharge Capability	IEC 61000-4-2 System Level ESD	Air Discharge	-15	+15	kV
			Contact Discharge	-8	+8	
		Human Body, ANSI/ESDA/JEDEC JS-001-2012	All Pins	-2	+2	
		Charged Device Model, JESD22-C101	All Pins	-1.5	+1.5	
Surge		IEC 61000-4-5, Surge Protection	VBUS	-100	100	V

Note1: Test at T_A=25°C with the component mounted on 6cm×4cm, FR4, 2layer, Top and Bottom layer 1oz.

For Example, When I_{OUT}=2A, R_{ON}=33mΩ, P_D=2×2×0.033=0.132W, T_J=0.132×105+25=28.86°C

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Electrical Characteristics

T_A=-40°C to 85°C unless otherwise noted, typical values are at V_{IN}=5V, I_{IN}≤2A, C_{IN}=0.1μF and T_A=25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Basic Operation						
V _{IN}	Input Voltage		2.5		28	V
V _{IN_CLAMP}	Input Clamping Voltage	I _{IN} =10mA		34		V
I _{IN}	V _{IN} Quiescent Current	V _{IN} =5V, OUT Floating		95		μA
R _{ON}	On-Resistance of Switch IN-OUT	V _{IN} =5.0V, I _{OUT} =2A, T _A =25°C		33	42	mΩ
V _{OVLO}	Over-voltage protect of V _{IN}	V _{IN} Rising, OVLO=GND	6.6	6.8	7.0	V
	Over-voltage protect hysteresis of V _{IN}			0.25		V
	Adjustable OVLO Threshold Range	V _{IN} =2.5V to V _{OVLO}	4		26	V
V _{OVLO_TH}	OVLO Set Threshold	V _{IN} =2.5V to V _{OVLO}	1.18	1.2	1.22	V
V _{OVLO_SEL CET}	External OVLO Select Threshold		0.2		0.3	V
V _{UVLO_R}	Under Voltage	V _{IN} Rising		2.1		V
V _{UVLO_F}	Lockout Threshold	V _{IN} Falling		1.9		V
V _{OL_FLAG}	FLAG Output Logic Low Voltage	V _{PU} =1.8V, I _{SINK} =1mA		0.1	0.2	V
I _{FLAG_LEAK}	FLAG Output HIGH Leakage Current	V _{FLAG} =5V,			0.5	uA
I _{OVLO}	OVLO Input Leakage Current	V _{OVLO} =V _{OVLO_TH}	-100		100	nA
V _{IH}	$\overline{\text{EN}}$ Input Logic High Voltage		1.4			V
V _{IL}	$\overline{\text{EN}}$ Input Logic Low Voltage	V _{IN} =2.5V			0.3	V
T _{SHDN}	Thermal Shutdown ⁽²⁾			155		°C
T _{SHDN_HYS}	Thermal-shutdown Hysteresis ⁽²⁾			20		°C
Dynamic Characteristics						
t _{DEB}	Debounce Time	Time from V _{UVLO_R} <V _{IN} <V _{OVLO} to V _{OUT} =10% of V _{IN}		15		ms
t _{SS}	Soft-start time	Time from V _{UVLO_R} <V _{IN} <V _{OVLO} to 0.2×FLAG, V _{IO} =1.8V with 10kΩ Pull-up Resistor		30		ms

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Electrical Characteristics(Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_{ON}	Switch Turn-On Time	$R_L=100\Omega$, $C_L=22\mu F$, V_{OUT} from $0.1 \times V_{IN}$ to $0.9 \times V_{IN}$		2		ms
$t_{OFF_RES}^{(2)}$	Switch turn-off response time	$V_{IN} > V_{OVLO}$ to V_{OUT} stop rising		50		ns

Note2: Guaranteed by characterization and design.

Timing Waveform

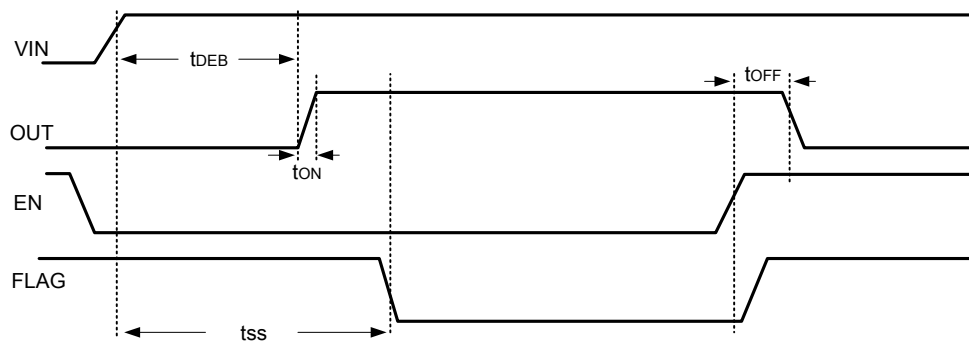


Figure1. Timing for Power Up and Normal Operation

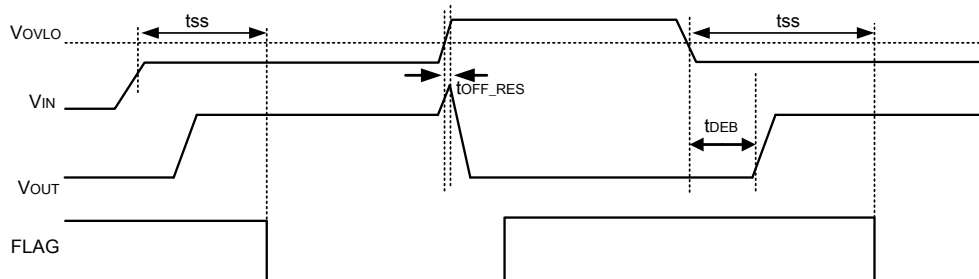


Figure2. Timing for OVLO Trip

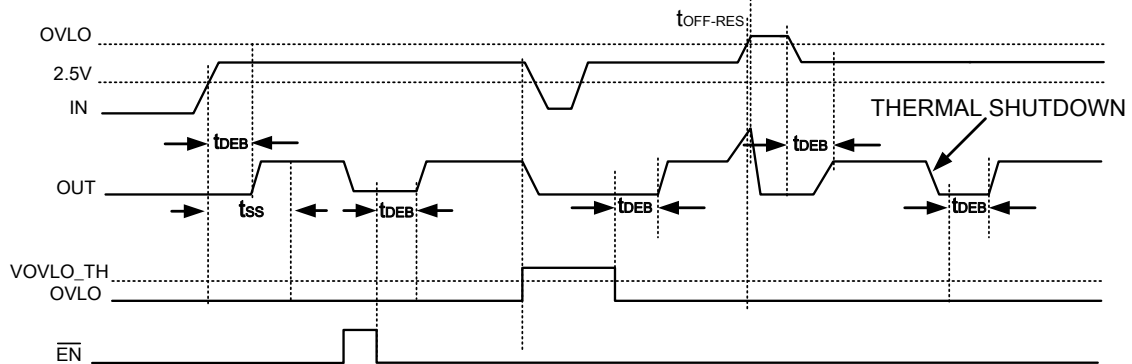
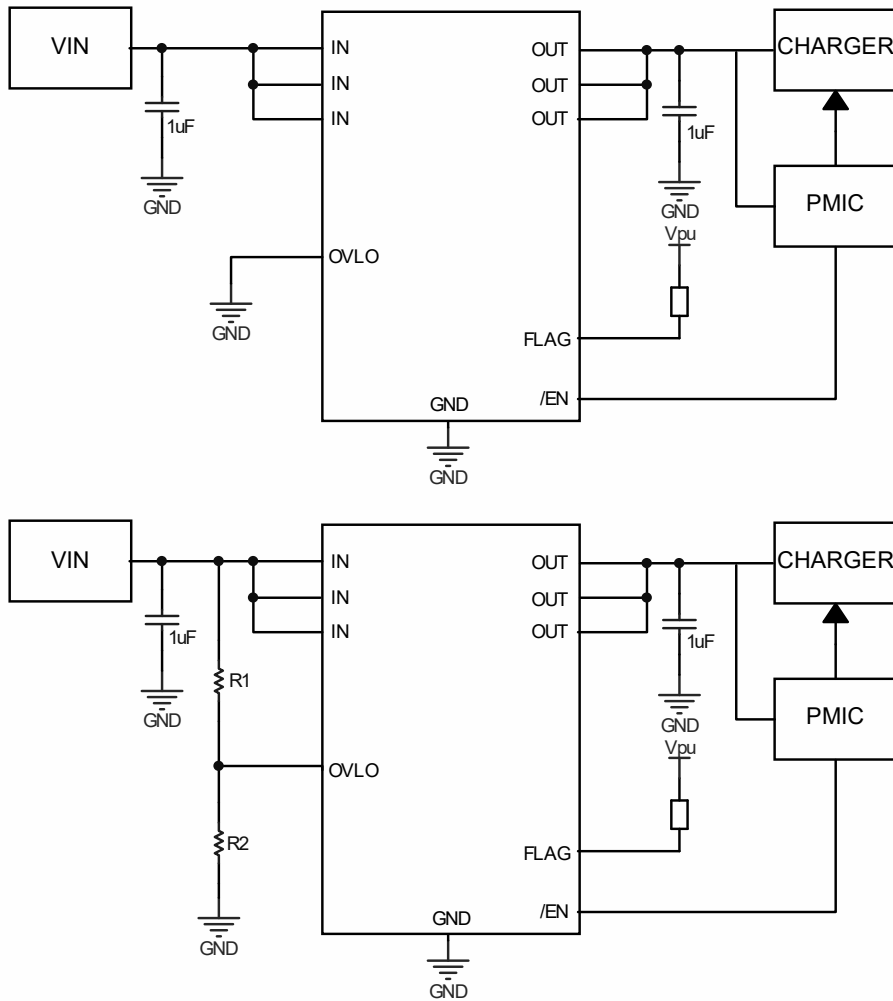


Figure3. Timing Waveform

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Application Circuits



R1 and R2 are only required for adjustable OVLO; otherwise connect OVLO to GND

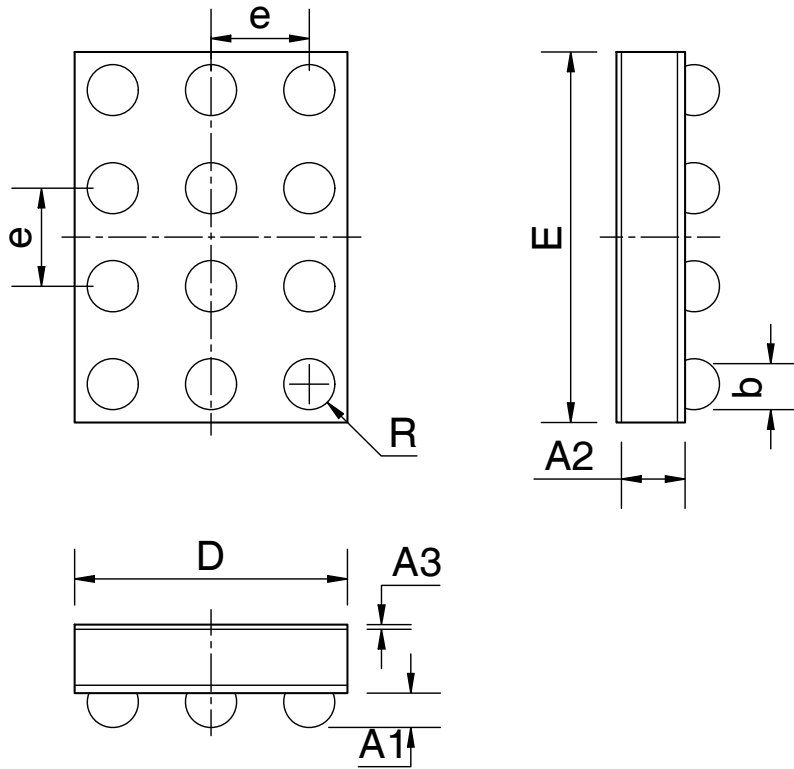
Recommend $30K \leq R2 \leq 51K$

Note*: This electric circuit only supplies for reference.

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Package Dimension

WLCSP12



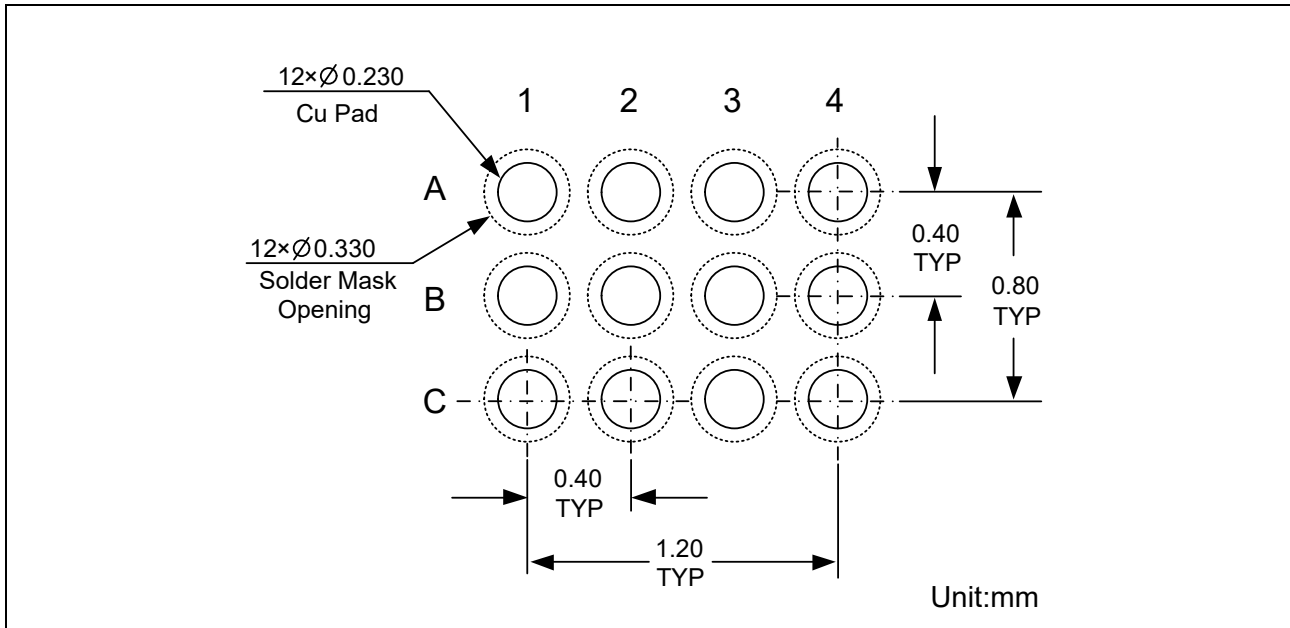
COMMON DIMENSIONS

(Unit: mm)

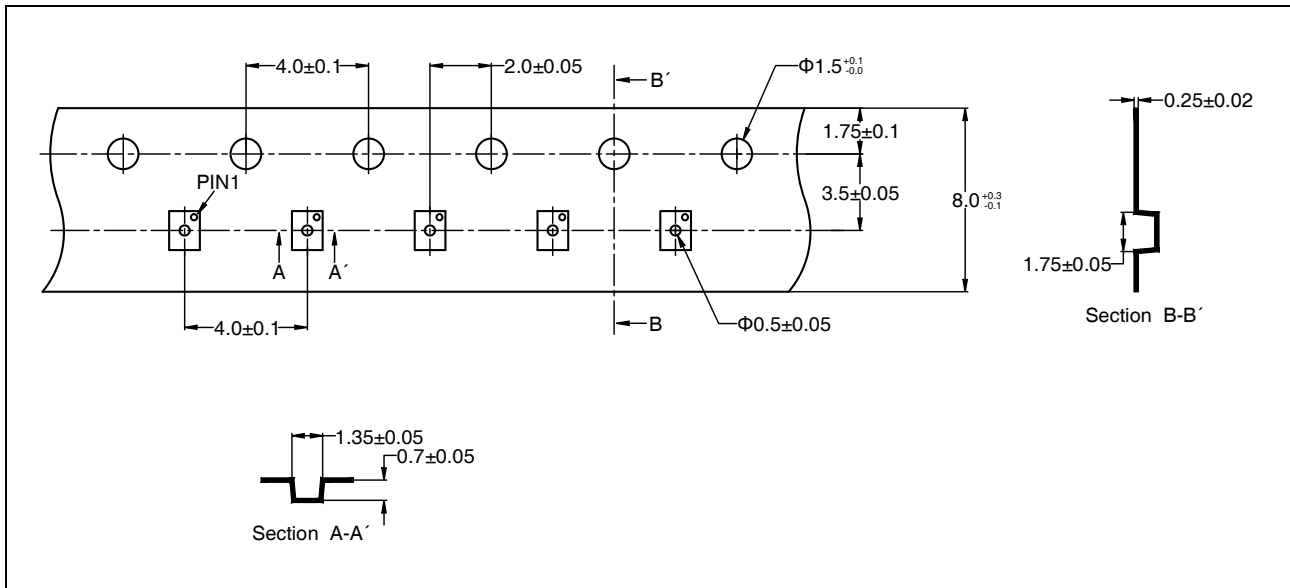
SYMBOL	MIN	NOM	MAX
A1	0.12	0.14	0.16
A2	0.39	0.40	0.41
A3	0.028	0.035	0.042
b	0.15	0.18	0.21
D	1.05	1.10	1.15
E	1.50	1.55	1.60
e	0.40BSC		
R	0.15	0.18	0.21

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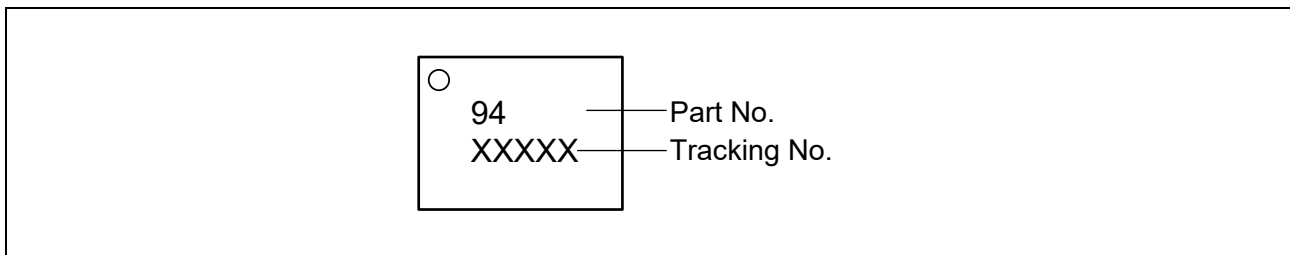
Land Pattern Data



Tape Information



Marking



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Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2020-01-16	Original Version	Wu Min	Wu Min	Zhu Jun Li
1.1	2024-07-01	Add Marking	Wangp	Wangp	Liujiy
1.2	2024-09-02	Update Adjustable OVLO Threshold Range	Wangp	Wangp	Liujiy
1.3	2025-07-23	Add R _{θJA}	Wangp	Wangp	Liujiy
1.4	2025-10-14	Add Land Pattern Data	Caojc	Wuhs	Liujiy
1.5	2026-05-22	Update Timing Waveform	Caojc	Wuhs	Liujiy