

ET2104 - 4 Bit Level Translator for I²C Applications

General Description

The ET2104 is a high-performance configurable dual-voltage-supply translator for bi-directional voltage translation over a wide range of input and output voltages levels. The ET2104 also works in a push-pull environment.

It is intended for use as a voltage translator between I²C-Bus compliant masters and slaves. Internal 10K Ω pull-up resistors are provided.

The device is designed so the A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi-directional A/B-port voltage translation between any two levels from 1.65V to 5.5V. V_{CCA} can equal V_{CCB} from 1.65V to 5.5V. Either V_{CC} can be powered-up first. Internal power-down control circuits place the device in 3-state if either V_{CC} is removed.

The four ports of the device have automatic direction-sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

Features

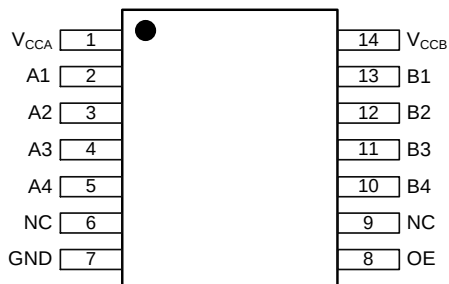
- Bi-Directional Interface between Any Two Levels: 1.65V to 5.5V
- No Direction Control Needed
- Internal 10K Pull-Up Resistors
- System GPIO Resources Not Required when OE tied to V_{CCA}
- I²C-Bus Isolation
- A/B Port V_{OL} = 175mV (Typical) @ V_{IL} = 150mV, I_{OL} = 6mA
- Open-Drain Inputs / Outputs
- Works in Push Pull Environment
- Accommodates Standard-Mode and Fast-Mode I²C-Bus Devices
- Supports I²C Clock Stretching & Multi-Master
- Fully Configurable: Inputs and Outputs Track V_{CC}
- Non-Preferential Power-Up; Either V_{CC} Can Power-Up First
- Outputs Switch to 3-State if Either V_{CC} is at GND
- Tolerant Output Enable: 5V
- ESD Protection Exceeds:
 - B Port: ± 8 kV HBM ESD Pass (vs. GND & vs. V_{CCB})
 - All Pins: ± 4 kV HBM ESD Pass per JKDEC JS-001
 - All Pins: ± 2 kV CDM ESD Pass per JKDEC JS-002

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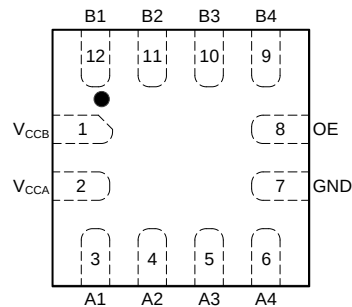
Device Information

Part No.	Package
ET2104	CSP12 (0.5pitch)
ET2104V	TSSOP14
ET2104Y	QFN12 (1.8mm x 1.8mm)
ET2104Y2	QFN12 (2.0mm x 2.0mm)
ET2104Y3	QFN14 (2.5mm x 3.0mm)
ET2104YS	QFN14 (3.5mm x 3.5mm)

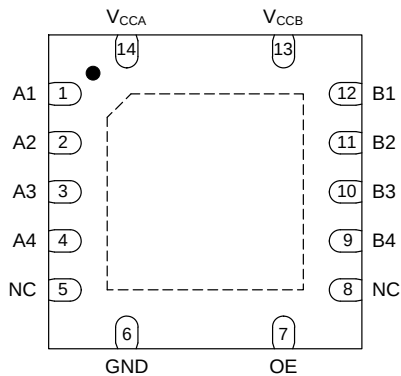
Pin Configuration



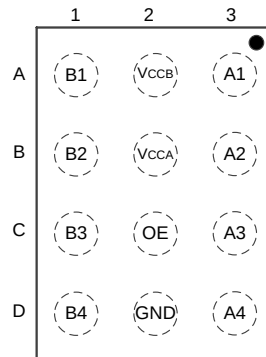
(ET2104V) TSSOP14



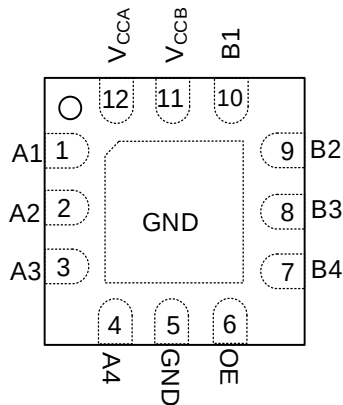
(ET2104Y) QFN12



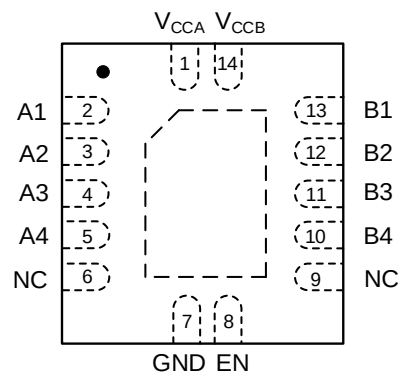
(ET2104YS) QFN14



(ET2104) CSP12



(ET2104Y2) QFN12



(ET2104Y3) QFN14

TOP VIEW

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Pin Function

TSSOP14 ET2104V	CSP12 ET2104	QFN12 ET2104Y	QFN12 ET2104Y2	QFN14 ET2104YS	QFN14 ET2104Y3	Symbol	Description
1	B2	2	12	14	1	V _{CCA}	A-Side Power Supply
2, 3, 4, 5	A3, B3, C3, D3	3, 4, 5, 6	1, 2, 3, 4	1, 2, 3, 4	2, 3, 4, 5	A1, A2, A3, A4	A-Side Inputs or 3-State Outputs
7	D2	7	5	6	7	GND	Ground
8	C2	8	6	7	8	OE	Output Enable Port, Input
10, 11, 12, 13	D1, C1, B1, A1	9, 10, 11, 12	7, 8, 9, 10	9, 10, 11, 12	10, 11, 12, 13	B4, B3, B2, B1	B-Side Inputs or 3-State Outputs
14	A2	1	11	13	14	V _{CCB}	B-Side Power Supply
6, 9				5, 8	6, 9	NC	

Truth Table

Control	Outputs
OE ⁽¹⁾	
Low Logic Level	3-State
High Logic Level	Normal Operation

Note1: If the OE pin is driven LOW, the ET2104 is disabled and the A1~A4, B1~B4 pins (including dynamic drivers) are forced into 3-state and all four 10KΩ internal pull-up resistors are decoupled from their respective V_{CC}.

Block Diagram

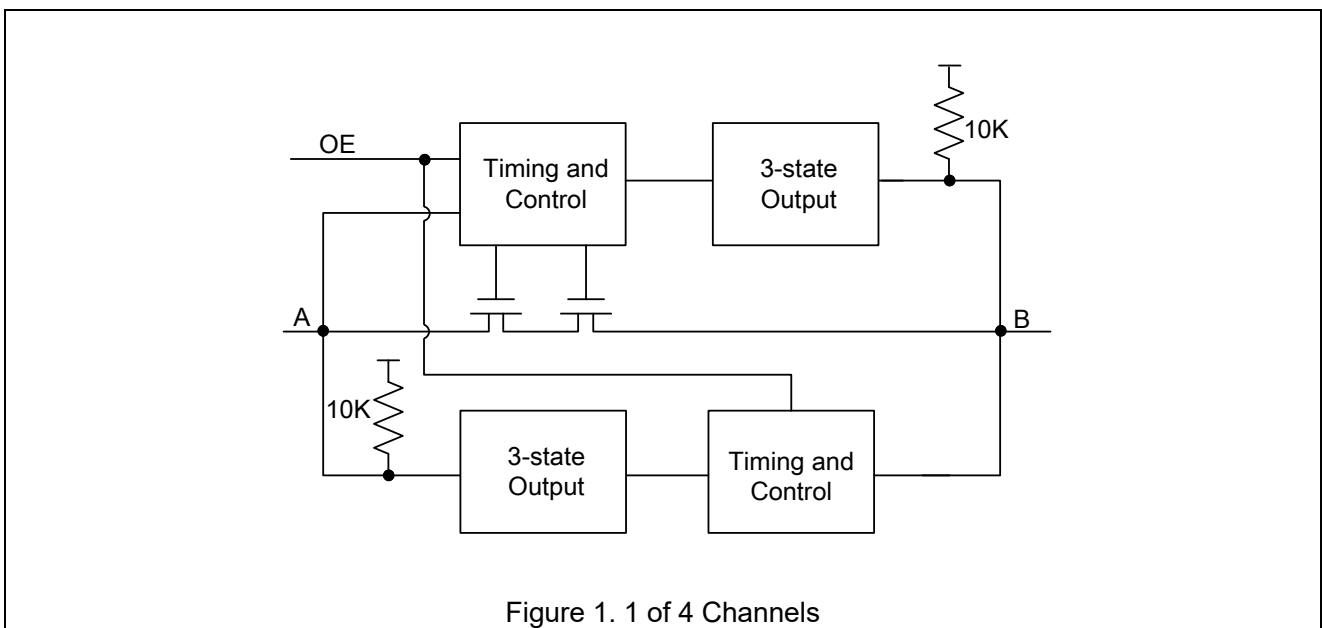


Figure 1. 1 of 4 Channels

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Functional Description

Power-Up / Power-Down Sequencing

ET2104 is a bi-directional level shift. So translators offer an advantage in that either VCC may be powered up first. This benefit derives from the chip design. When either VCC is at 0V, outputs are in a high-impedance state. The control input (OE) is designed to track the V_{CCA} supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin. We recommended the power-up and power-down as below:

The recommended power-up sequence is:

1. Apply power to the first VCC.
2. Apply power to the second VCC.
3. Drive the OE input HIGH to enable the device.

The recommended power-down sequence is:

1. Drive OE input LOW to disable the device.
2. Remove power from either VCC.
3. Remove power from the other VCC.

Note2: Alternatively, the OE pin can be hardwired to V_{CCA} to save GPIO pins. If OE is hardwired to V_{CCA} , either VCC can be powered up or down first.

Application Circuits

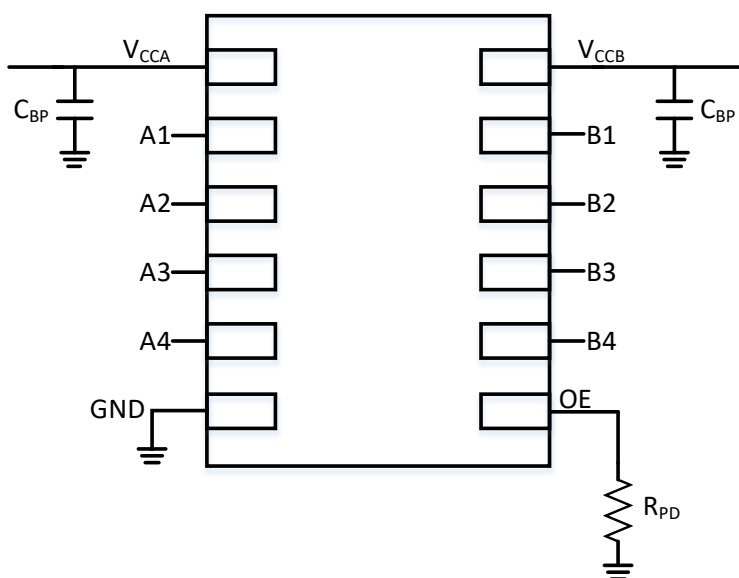


Figure 2. Application Circuit (*)

Note*: This electric circuit only supplies for reference.

Application Information

ET2104 has open-drain I/Os and includes a total of four 10K internal pull-up resistors (R_{PU}) on each of the four data I/O pins, as shown in Figure 2. If a pair of data I/O pins (A_n/B_n) is not used, both pins should be disconnected, eliminating unwanted current flow through the internal R_{PU} s. External R_{PU} s can be added to the I/Os to reduce the total R_{PU} value, depending on the total bus capacitance.

The designer is free to lower the total pull-up resistor value to meet the maximum I²C edge rate per the I²C specification. For example, according to the I²C specification, the maximum edge rate (30% - 70%) during Fast Mode (400kbit/s) is 300ns. If the bus capacitance is approaching the maximum 400pF, a lower total R_{PU} value helps keep the rise time below 300ns (Fast Mode). Likewise, the I²C specification also specifies a minimum Serial Clock Line High Time of 600ns during Fast Mode (400KHz). Lowering the total R_{PU} also helps increase the SCL High Time. If the bus capacitance approaches 400pF, it may make sense to use the ET2104, which does not contain internal R_{PU} . Then calculate the ideal external R_{PU} value.

Note3: Section 7.1 of the I²C specification provides an excellent guideline for pull-up resistor sizing.

Theory of Operation

ET2104 is designed for high-performance level shifting and buffer / repeating in an I²C application. Figure 1 shows that each bi-directional channel contains two series-N-gates and two dynamic drivers. This hybrid architecture is highly beneficial in an I²C application where auto-direction is a necessity.

For example, during the following three I²C protocol events:

- Clock Stretching
- Slave's ACK Bit (9th bit = 0) following a Master's Write Bit (8th bit = 0)
- Clock Synchronization and Multi-Master Arbitration

The bus direction needs to change from master-to-slave to slave-to-master without the occurrence of an edge. If there is an I²C translator between the master and slave in these examples, the I²C translator must change direction when both A and B ports are LOW. The N-gates can accomplish this task very efficiently because, when both A and B ports are LOW, the N-gates act as a low-resistive short between the A and B ports.

Due to I²C's open-drain topology, I²C masters and slaves are not push/pull drivers. Logic LOWs are "pulled down" (I_{SINK}), while logic HIGHs are "let go" (3-state). For example, when the master lets go of SCL (SCL always comes from the master), the rise time of SCL is largely determined by the RC time constant, where $R = R_{PU}$ and C = the bus capacitance.

If the ET2104 is attached to the master [on the A port] and there is a slave on the B port, the N-gates act as a low-resistive short between both ports until either of the port's $V_{CC}/2$ thresholds are reached. After the RC time constant has reached the $V_{CC}/2$ threshold of either port, the port's edge detector triggers both dynamic drivers to drive their respective ports in the LOW-to-HIGH (LH) direction, accelerating the rising edge. Effectively, two distinct slew rates appear in rise time. The first slew rate (slower) is the RC time constant of the bus. The second slew rate (much faster) is the dynamic driver accelerating the edge.

If both the A and B ports of the translator are HIGH, a high-impedance path exists between the A and B ports. Because both the N-gates are turned off. If a master or slave device decides to pull SCL or SDA LOW, that

device's driver pulls down (I_{SINK}) SCL or SDA until the edge reaches the A or B port VCC/2 threshold. When either the A or B port threshold is reached, the port's edge detector triggers both dynamic drivers to drive their respective ports in the HIGH-to-LOW (HL) direction, accelerating the falling edge.

VOL vs IOL

The I²C specification mandates a maximum V_{IL} (I_{OL} of 3mA) of $VCC \times 0.3$ and a maximum V_{OL} of 0.4V. If there is a master on the A port of an I²C translator with a VCC of 1.65V and a slave on the I²C translator B port with a VCC of 3.3V, the maximum V_{IL} of the master is $(1.65V \times 0.3)$ 495mV. The slave could legally transmit a valid logic LOW of 0.4V to the master.

If the I²C translator's channel resistance is too high, the voltage drop across the translator could present a V_{IL} to the master greater than 495mV. To complicate matters, the I²C specification states that 6mA of I_{OL} is recommended for bus capacitance approaching 400pF. More I_{OL} increases the voltage drop across the I²C translator. The I²C application benefits when I²C translators exhibit low V_{OL} performance.

I²C Bus Isolation

The ET2104 supports I²C-Bus isolation for the following conditions:

- Bus isolation if bus clear
- Bus isolation if either VCC goes to ground

Bus Clear

Because the I²C specification defines the minimum SCL frequency of DC, the SCL signal can be held LOW forever; however. This condition shuts down the I²C bus. The I²C specification refers to this condition as "Bus Clear."

In Figure 3; if slave #2 holds down SCL forever, the master and slave #1 are not able to communicate because the ET2104 passes the SCL stuck-LOW condition from slave #2 to slave #1 and as the master. However, if the OE pin is pulled LOW (disabled), both ports (A and B) are 3-stated. This results in the ET2104 isolating slave #2 from the master and slave #1, allowing full communication between the master and slave #1.

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VCC to GND

If slave #2 is a camera that is suddenly removed from the I²C bus, resulting in V_{CCB} transitioning from a valid VCC (1.65V~5.5V) to 0V; the ET2104 automatically forces SCL and SDA on both its A and B ports into 3-state. Once V_{CCB} has reached 0V, full I²C communication between the master and slave #1 remains undisturbed.

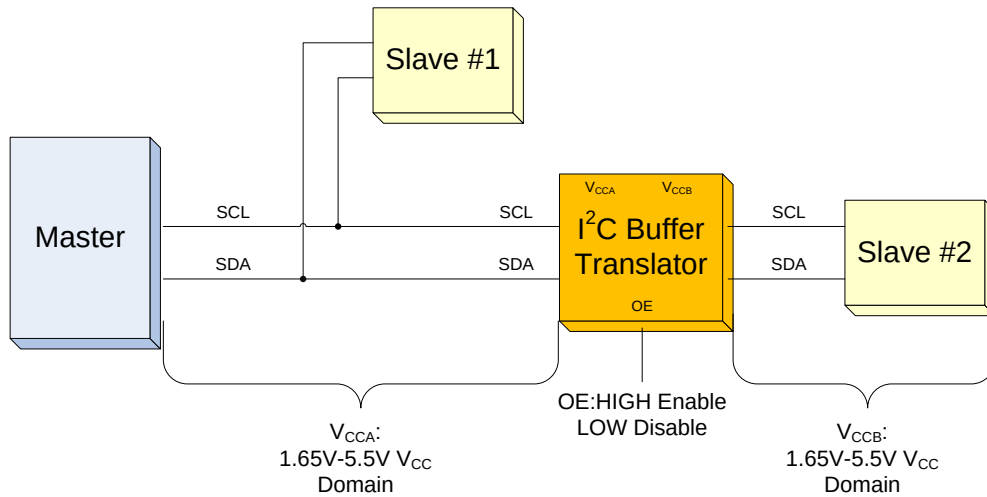


Figure 3. Bus Isolation

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Supply Voltage		-0.5	7.0	V
V_{IN}	DC Input Voltage	A Port	-0.5	7.0	
		B Port	-0.5	7.0	
		Control Input (OE)	-0.5	7.0	
V_O	Output Voltage ⁽⁴⁾	An Outputs 3-State	-0.5	7.0	V
		Bn Outputs 3-State	-0.5	7.0	
		An Outputs Active	-0.5	$V_{CCA} + 0.5V$	
		Bn Outputs Active	-0.5	$V_{CCB} + 0.5V$	
I_{IK}	DC Input Diode Current	At $V_{IN} < 0V$		-50	mA
I_{OK}	DC Output Diode Current	At $V_O < 0V$		-50	
		At $V_O > V_{CC}$		+50	
I_{OH} / I_{OL}	DC Output Source/Sink Current		-50	+50	
I_{CC}	DC VCC or Ground Current per Supply Pin			± 100	
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction temperature		-40	+150	°C
V_{ESD}	Electrostatic Discharge Capability	Human Body Model, B-Port Pins		± 8	kV
		Human Body Model, All Pins (JKDEC JS-001)		± 4	
		Charged Device Mode, JKDEC JS-002		± 2	

Note4: I_O absolute maximum rating must be observed.

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Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. We does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Power Supply Operating		1.65	5.5	V
V_{IN}	Input Voltage ⁽⁵⁾	A-Port	0	5.5	V
		B-Port	0	5.5	
		Control Input (OE)	0	V_{CCA}	
T_A	Free Air Operating Temperature		-40	+85	°C

Note5: All unused inputs and I/O pins must be held at V_{CCI} or GND. V_{CCI} is the V_{CC} associated with the input side.

DC Electrical Characteristics⁽⁶⁾

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Conditions	$V_{CCA}(\text{V})$	$V_{CCB}(\text{V})$	Min	Typ	Max	Unit
V_{IHA}	High Level Input Voltage A	Data Inputs An	1.65~5.5	1.65~5.5	V_{CCA} -0.4			V
		Control Input OE	1.65~5.5	1.65~5.5	$0.7 \times V_{CCA}$			
V_{IHB}	High Level Input Voltage B	Data Inputs Bn	1.65~5.5	1.65~5.5	V_{CCB} -0.4			V
V_{ILA}	Low Level Input Voltage A	Data Inputs An	1.65~5.5	1.65~5.5			0.4	V
		Control Input OE	1.65~5.5	1.65~5.5			$0.3 \times V_{CCA}$	
V_{ILB}	Low Level Input Voltage B	Data Inputs Bn	1.65~5.5	1.65~5.5			0.4	V
V_{OL}	Low Level Output Voltage	$V_{IL} = 0.15\text{V}$ $I_{OL} = 6\text{mA}$	1.65~5.5	1.65~5.5			0.4	V
I_L	Input Leakage Current	Control Input OE, $V_{IN} = V_{CCA}$ or GND	1.65~5.5	1.65~5.5			± 1.0	μA
I_{OFF}	Power-Off Leakage Current	An V_{IN} or $V_O = 0\text{V}$ to 5.5V	0	5.5			± 2.0	μA
		Bn V_{IN} or $V_O = 0\text{V}$ to 5.5V	5.5	0			± 2.0	

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DC Electrical Characteristics (Continued) ⁽⁶⁾

T_A = -40°C to +85°C

Symbol	Parameter	Conditions		V _{CCA} (V)	V _{CCB} (V)	Min	Typ	Max	Unit
I _{OZ}	3-State Output Leakage ⁽⁷⁾	AnBn	V _O =0V to 5.5V OE=V _{IL}	5.5	5.5			±2.0	uA
I _{OZ}	3-State Output Leakage ⁽⁷⁾	An	V _O =0V to 5.5V, OE=Don't care	5.5	0			±2.0	uA
		Bn	V _O =0V to 5.5V, OE=Don't care	0	5.5			±2.0	
I _{CCA/B}	Quiescent Supply Current ^(8,9)	V _{IN} =V _{CCI} or Floating, I _O = 0		1.65~5.5	1.65~5.5			5.0	uA
I _{CCZ}	Quiescent Supply Current ⁽⁸⁾	V _{IN} = V _{CCI} or GND, I _O = 0, OE = V _{IL}		1.65~5.5	1.65~5.5			5.0	uA
I _{CCA}	Quiescent Supply Current ⁽⁷⁾	V _{IN} = 5.5V or GND, I _O =0, OE=Don't Care, Bn to An		0	1.65~5.5			-2.0	uA
				1.65~5.5	0			2.0	
I _{CCB}	Quiescent Supply Current ⁽⁷⁾	V _{IN} = 5.5V or GND, I _O = 0, OE = Don't Care, An to Bn		1.65~5.5	0			-2.0	uA
				0	1.65~5.5			2.0	
R _{PU}	Resistor Pull-up Value	V _{CCA} & V _{CCB} Sides		1.65~5.5	1.65~5.5		10		kΩ

Notes:

6. This table contains the output voltage for static conditions.

Dynamic drive specifications are given in dynamic output Electrical Characteristics.

7. "Don't Care" indicates any valid logic level.

8. V_{CCI} is the VCC associated with the input side.

9. Reflects current per supply, V_{CCA} or V_{CCB}.

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Dynamic Output Electrical Characteristics

Output Rise / Fall Time ⁽¹⁰⁾

Output load: $C_L = 50\text{pF}$, $R_{PU} = \text{NC}$, push / pull driver, and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

Symbol	Parameter	V_{CCO} ⁽¹¹⁾				Unit
		4.5 to 5.5V	3.0 to 3.6V	2.3 to 2.7V	1.65 to 1.95V	
		Typ.	Typ.	Typ.	Typ.	
t_{RISE}	Output Rise Time: A Port, B Port ⁽¹²⁾	3	4	5	7	ns
t_{FALL}	Output Fall Time: A Port, B Port ⁽¹³⁾	1	1	1	1	ns

Notes:

10. Output rise and fall times guaranteed by design simulation and characterization; not production tested.

11. V_{CCO} is the V_{CC} associated with the output side.

12. See Figure 8.

13. See Figure 9.

Maximum Data Rate ⁽¹⁴⁾

Output load: $C_L = 50\text{pF}$, $R_{PU} = \text{NC}$, push / pull driver, and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

V _{CCA}	Direction	V _{CCB}				Unit
		4.5V to 5.5V	3.0V to 3.6V	2.3V to 2.7V	1.65V to 1.95V	
		Min.				
4.5V to 5.5V	A to B	15	16	13	9	MHz
	B to A	15	11	8	5	
3.0V to 3.6V	A to B	12	11	11	7	MHz
	B to A	16	12	9	5	
2.3V to 2.7V	A to B	6	6	6	6	MHz
	B to A	12	11	9	5	
1.65V to 1.95V	A to B	5	5	5	5	MHz
	B to A	8	7	6	5	

Open-Drain Data Rate

V_{CCA}	Direction	V_{CCB}	Test condition	Date Rate	Unit
1.8~5.5V	A to B	1.8~5.5V	I/O port parallel 1K resistance to power supply	1	Mbps
	B to A			1	Mbps

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AC Characteristics ⁽¹⁵⁾

Output Load: $C_L = 50\text{pF}$, $R_{PU} = \text{NC}$, push / pull driver, and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

Symbol	Parameter	V _{CCB}								Unit
		4.5V to 5.5V		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
V _{CCA} =4.5V to 5.5V										
t _{PLH}	A to B	10	22	10	22	10	22	12	26	ns
	B to A	5	12	7	16	9	20	12	26	
t _{PHL}	A to B	16	34	15	32	14	30	14	30	ns
	B to A	12	26	12	26	12	26	13	28	
t _{PZL}	OE to A	13	26	13	26	13	26	13	26	ns
	OE to B	11	22	11	22	11	22	14	28	
t _{PLZ}	OE to A	65	105	65	105	65	105	65	105	ns
	OE to B	5	11	5	11	5	11	6	13	
t _{SKEW}	A Port,B Port ⁽¹⁶⁾	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns
V _{CCA} =3.0V to 3.6V										
t _{PLH}	A to B	4	10	4	10	4	10	7	16	ns
	B to A	4	10	4	10	6	14	8	18	
t _{PHL}	A to B	13	28	13	28	13	28	13	28	ns
	B to A	9	20	9	20	12	26	15	32	
t _{PZL}	OE to A	5	10	5	10	7	14	10	20	ns
	OE to B	5	10	6	12	7	14	11	22	
t _{PLZ}	OE to A	100	115	100	115	100	115	100	115	ns
	OE to B	5	11	5	11	6	13	9	15	
t _{SKEW}	A Port,B Port ⁽¹⁶⁾	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns
V _{CCA} =2.3V to 2.7V										
t _{PLH}	A to B	6	14	6	14	6	14	9	20	ns
	B to A	4	10	4	10	6	14	10	22	
t _{PHL}	A to B	20	42	14	30	13	28	13	28	ns
	B to A	9	20	9	20	11	24	14	30	
t _{PZL}	OE to A	6	12	6	12	7	14	11	22	ns
	OE to B	6	12	6	12	7	14	12	24	
t _{PLZ}	OE to A	100	115	100	115	100	115	100	115	ns
	OE to B	65	110	62	110	12	25	12	25	
t _{SKEW}	A Port,B Port ⁽¹⁶⁾	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns

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AC Characteristics (Continued) ⁽¹⁵⁾

Output Load: $C_L = 50\text{pF}$, $R_{PU} = \text{NC}$, push / pull driver, and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

Symbol	Parameter	V _{CCB}								Unit
		4.5V to 5.5V		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
V _{CCA} =1.65V to 1.95V										
t _{PLH}	A to B	10	24	10	24	10	24	12	28	ns
	B to A	5	14	7	16	9	18	12	28	
t _{PHL}	A to B	16	36	15	34	14	31	14	31	ns
	B to A	12	28	11	26	11	26	11	26	
t _{PZL}	OE to A	13	25	13	25	13	25	13	25	ns
	OE to B	11	23	11	23	11	23	14	26	
t _{PLZ}	OE to A	75	115	75	115	75	115	75	115	ns
	OE to B	75	115	75	115	75	115	75	115	
t _{SKEW}	A Port, B Port ⁽¹⁶⁾	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns

Notes:

14. 15. AC characteristics are guaranteed by design and characterization.

16. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (An or Bn) and switching with the same polarity (LOW to HIGH or HIGH to LOW) (see Figure 11). Skew is guaranteed; not production tested.

Capacitance

$T_A = +25^\circ\text{C}$.

Symbol	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance Control Pin (OE)	$V_{CCA} = V_{CCB} = \text{GND}$	2.2	pF
$C_{I/O}$	Input/Output Capacitance, An, Bn	$V_{CCA} = V_{CCB} = 5.0\text{V}$, OE = GND	13	pF

AC Test Reference Circuit

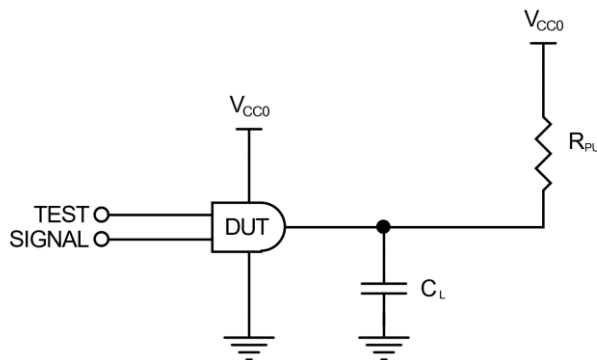


Figure 4. AC Test Circuit

AC Test Reference Conditions

Propagation Delay Test Conditions ⁽¹⁷⁾

Test	Input Signal	Output Enable Control
t_{PLH} , t_{PHL}	Data Pulses	V_{CCA}
t_{PZL} (OE to An, Bn)	0V	LOW to HIGH Switch
t_{PLZ} (OE to An, Bn)	0V	HIGH to LOW Switch

Note17: For t_{PZL} and t_{PLZ} testing, an external 2.2K pull-up resistor to V_{CCO} is required in order to force the I/O pins high while OE is Low because when OE is low, the internal 10K Ω RPU's are decoupled from their respective VCC'S.

AC Load Conditions

V_{CCO}	C_L	R_L
$1.8 \pm 0.15V$	50pF	NC
$2.5 \pm 0.2V$	50pF	NC
$3.3 \pm 0.3V$	50pF	NC
$5.0 \pm 0.5V$	50pF	NC

Timing Diagrams

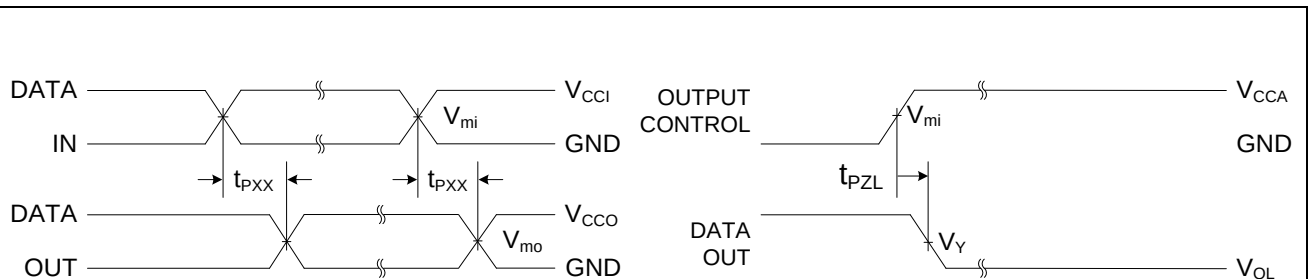


Figure 5. Inverting and Non-Inverting Functions ⁽¹⁸⁾

Figure 6. 3-STATE Output Low Enable Time ⁽¹⁸⁾

Timing Diagrams (Continued)

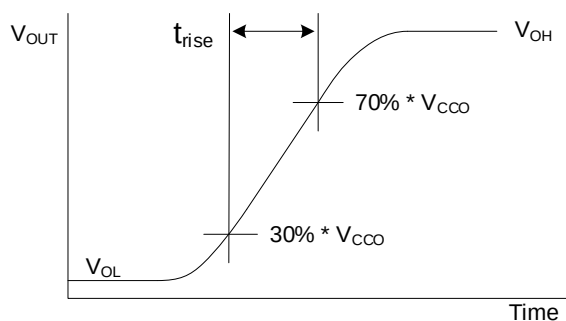


Figure 8. Active Output Rise Time

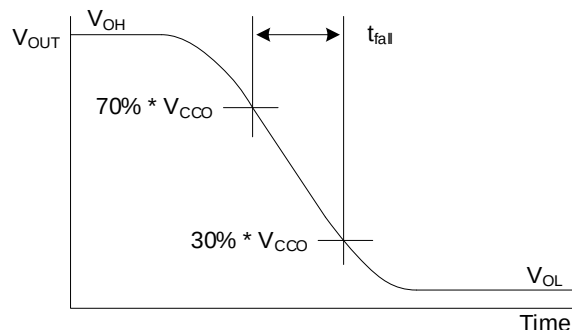


Figure 9. Active Output Fall Time

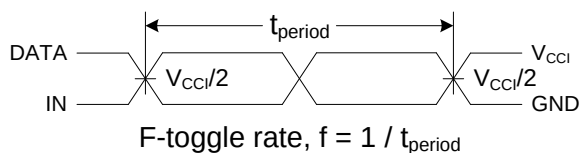


Figure 10. F-Toggle Rate

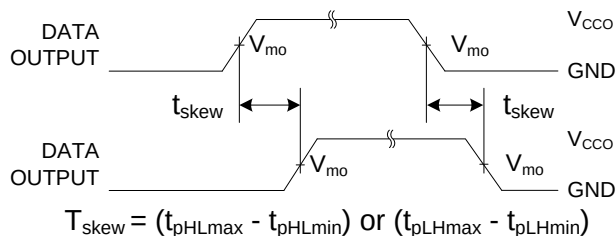


Figure 11. Output Skew Time

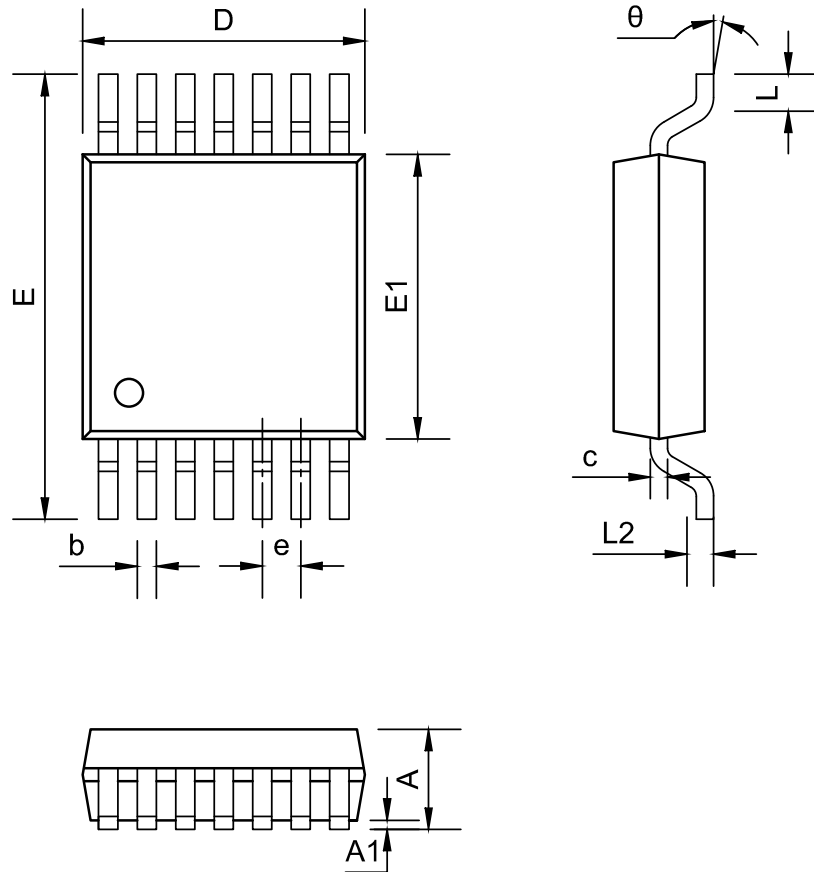
Notes:

18. Input $t_R = t_F = 2.0ns$, 10% to 90% at $V_{IN} = 1.65V$ to $1.95V$;
 Input $t_R = t_F = 2.0ns$, 10% to 90% at $V_{IN} = 2.3$ to $2.7V$;
 Input $t_R = t_F = 2.5ns$, 10% to 90%, at $V_{IN} = 3.0V$ to $3.6V$ only;
 Input $t_R = t_F = 2.5ns$, 10% to 90%, at $V_{IN} = 4.5V$ to 5.5 only.
19. $V_{CCI} = V_{CCA}$ for control pin OE or $V_{MIN} = (V_{CCA} / 2)$.

ET2104

Package Dimension

TSSOP14 (ET2104V)

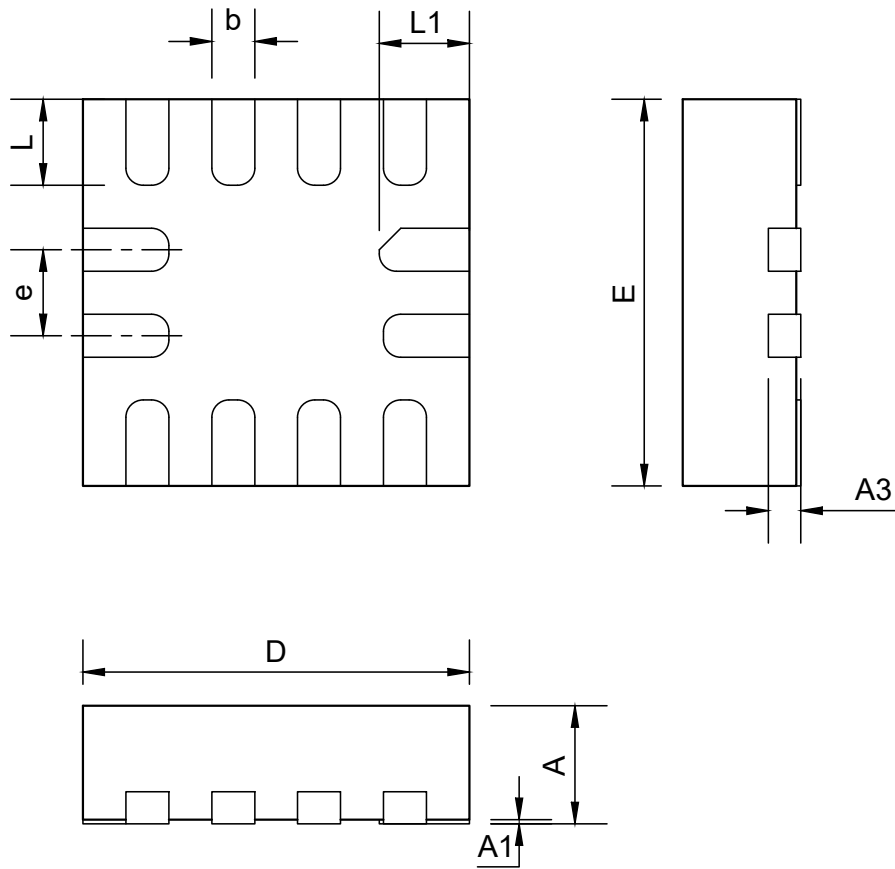


Dimensions Table (Units: mm)

Symbol	Min	Max
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 REF	
D	4.90	5.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.50	0.72
L2	0.25 REF	
θ	0°	8°

ET2104

QFN12(1.8mm x 1.8mm) (ET2104Y)

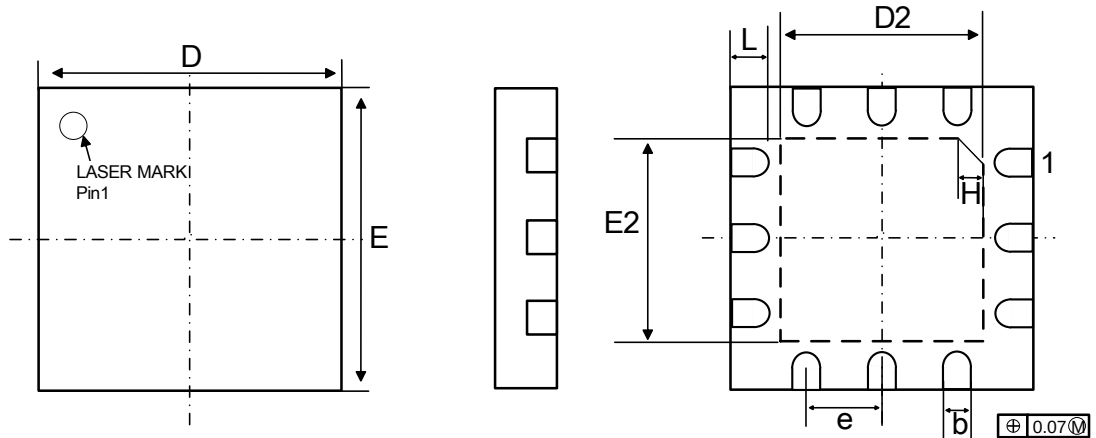


Dimensions Table (Units: mm)

Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00	--	0.05
A3	0.15 REF		
b	0.15	0.20	0.25
D	1.75	1.80	1.85
E	1.75	1.80	1.85
e	0.40 BSC		
L	0.35	0.40	0.45
L1	0.42 REF		

ET2104

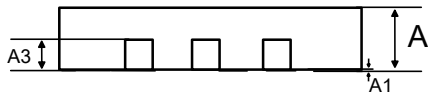
QFN12(2.0mm x 2.0mm) (ET2104Y2)



Top View

Side View

Bottom View



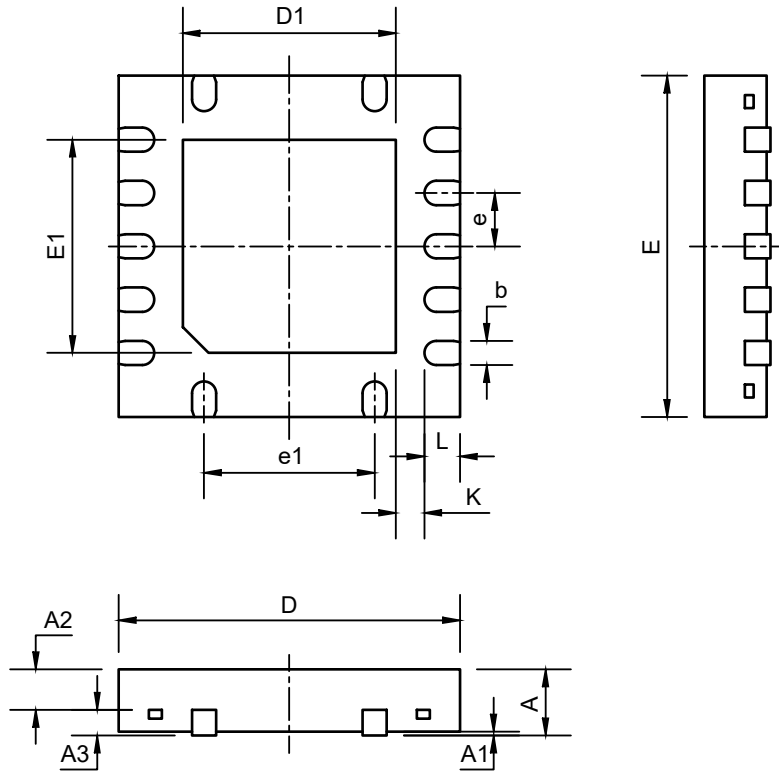
Side View

Dimensions Table (Units: mm)

Symbol	Min	Typ	Max
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A3	0.152 REF		
b	0.15	0.20	0.25
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D2	1.00	1.10	1.20
E2	1.00	1.10	1.20
e	0.35	0.40	0.45
L	0.15	0.20	0.25
H	0.20 REF		

ET2104

QFN14(3.5mm × 3.5mm) (ET2104YS)

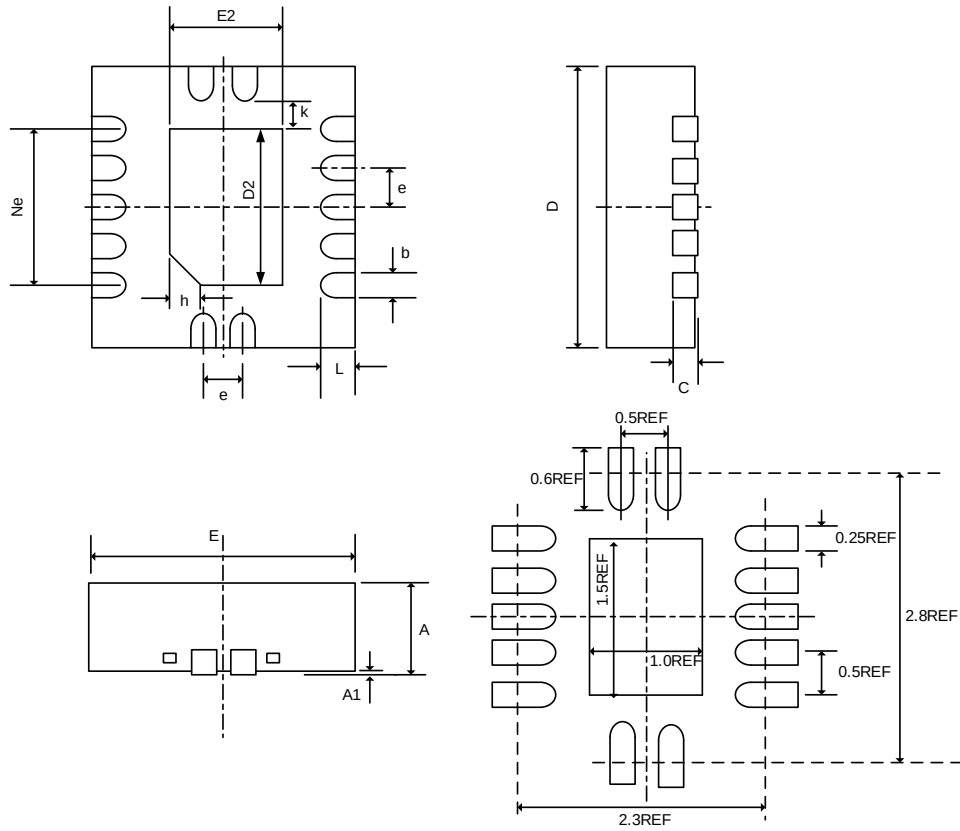


Dimensions Table (Units: mm)

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.7	0.75	0.8	e	0.5 BSC		
A1	0	0.02	0.05	e1	1.5 BSC		
A2	--	0.55	--	D1	1.9	2	2.1
A3	0.203 REF			E1	1.9	2	2.1
b	0.2	0.25	0.3	L	0.3	0.4	0.5
D	3.5 BSC			K	0.325 REF		
E	3.5 BSC						

ET2104

QFN14(2.5mm × 3.0mm) (ET2104Y3)

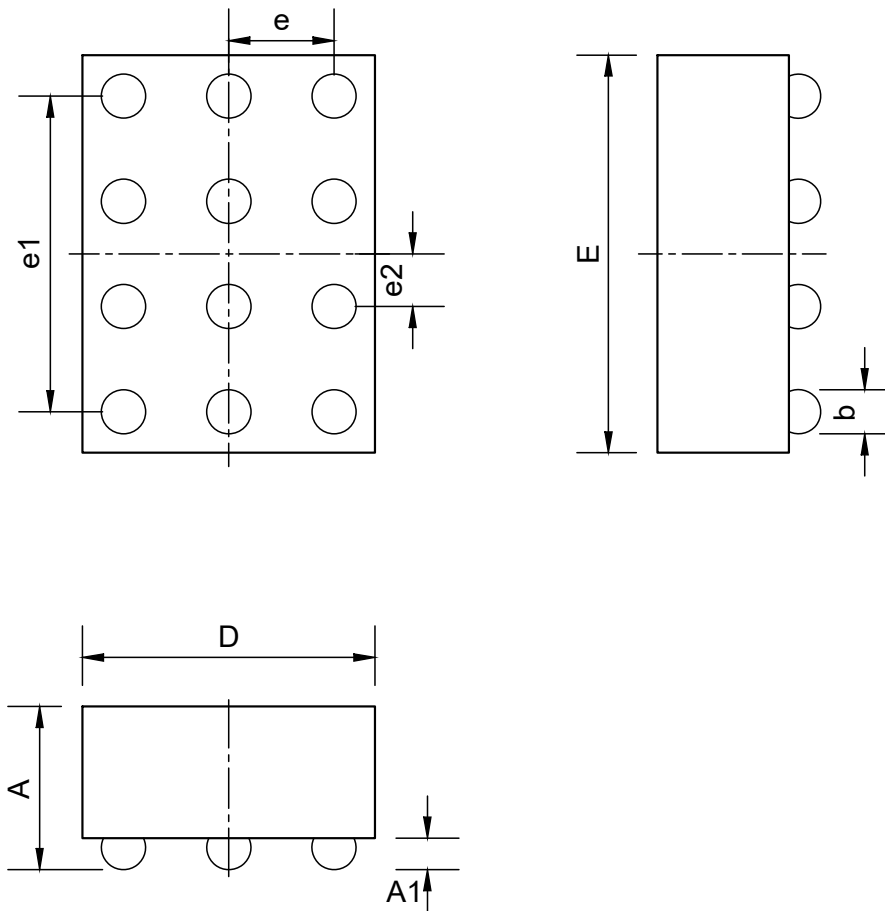


Dimensions Table (Units: mm)

Symbol	Min	Typ	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.2	0.25	0.3
c	0.20 REF		
D	2.90	3.00	3.10
D2	1.40	1.50	1.60
Ne	2.00 BSC		
e	0.50 BSC		
E	2.40	2.50	2.60
E2	0.90	1.00	1.10
L	0.3	0.4	0.5
K	0.20	-	-
h	0.25 REF		

ET2104

CSP12 (ET2104)



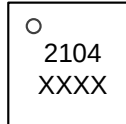
Dimensions Table (Units: mm)

Symbol	Min	Max
A	--	0.625
A1	0.15	0.19
b	0.21	0.25
D	1.33	1.39
E	1.83	1.89
e	0.50 BSC	
e1	1.50 BSC	
e2	0.25 BSC	

ET2104

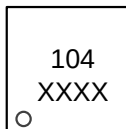
Marking Information

(1) ET2104Y QFN12



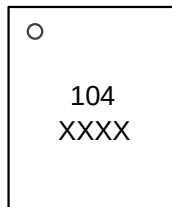
2104 - Part Number
XXXX - Tracking Number

(2) ET2104Y2 QFN12



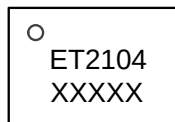
104 - Part Number
XXXX - Tracking Number

(3) ET2104Y3 QFN14



104 - Part Number
XXXX - Tracking Number

(4) ET2104 CSP12

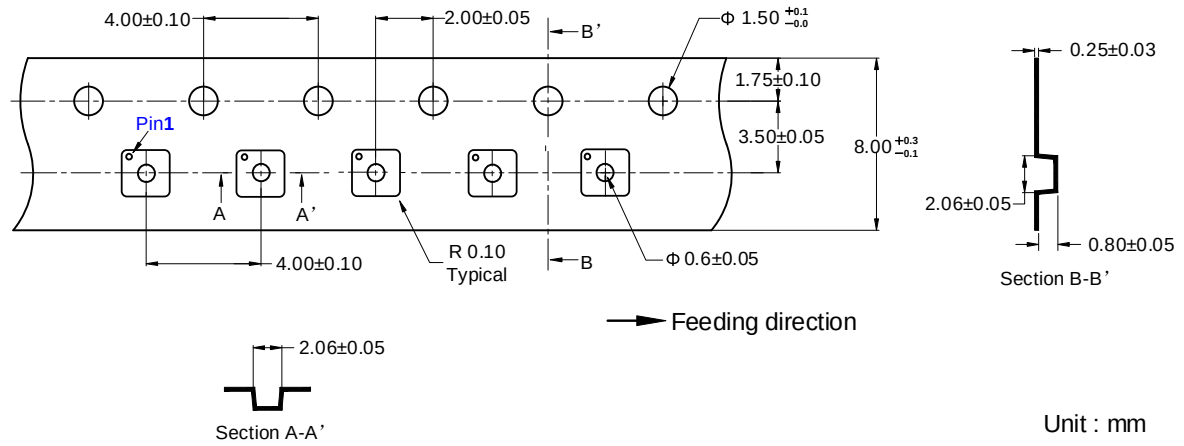


ET2104 - Part Number
XXXXX - Tracking Number

ET2104

Tape Information

ET2104Y



ET2104

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2016-08-29	Original Version	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.1	2016-09-23	Updated Pin Configuration	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.2	2016-11-08	Updated PIN1 shape	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.3	2017-12-12	Updated package	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.4	2019-09-03	Delete DFN8 package	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.5	2020-05-09	Updated form	Shibo	Shibo	Shibo
1.6	2022-7-27	Update Typeset	Shibo	Shibo	Shibo
1.7	2023-3-14	Update Marking	Shibo	Shibo	Shibo
1.8	2024-10-08	Update Marking and Tape	Wangp	Wangp	Wangp
1.9	2024-10-20	Update ET2104Y Marking	Wangp	Wangp	Liujiy
1.10	2024-11-13	Revise Marking	Wangp	Shibo	Liujiy
1.11	2025-06-19	Add Package	Wangar	Yangxx	Liujiy
1.12	2025-09-20	Add Package	Yangxx	Yangxx	Liujiy
1.12.a	2025-11-27	Correction EC Table	Yangxx	Yangxx	Liujiy
1.12.b	2025-12-25	Add Marking	Yangxx	Yangxx	Liujiy