

Low-Voltage CMOS Octal Buffer With 5V Tolerant Inputs and Outputs

General Description

The ET74LCX244 is a high performance, non-inverting octal buffer operating from a 2.3 to 5.5V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A VI specification of 5.5V allows ET74LCX244 inputs to be safely driven from 5V devices.

The ET74LCX244 is suitable for memory address driving and all TTL level bus-oriented transceiver applications. Current drive capability is 24mA at the outputs. The Output Enable (OE) input, when HIGH, disable the output by placing them in a HIGH Z condition.

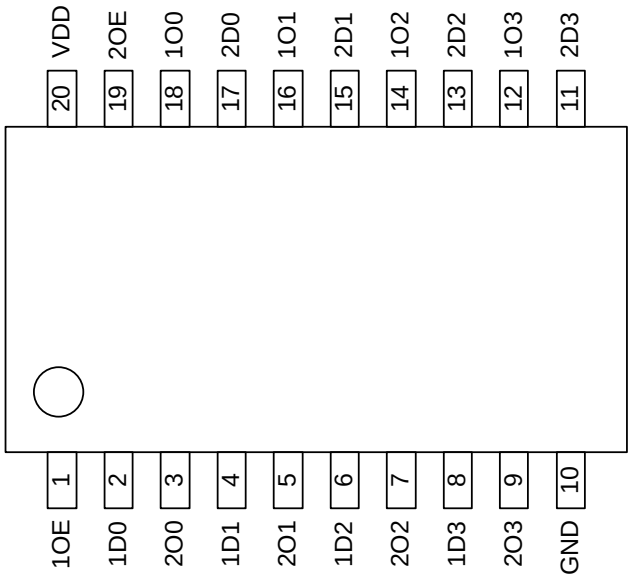
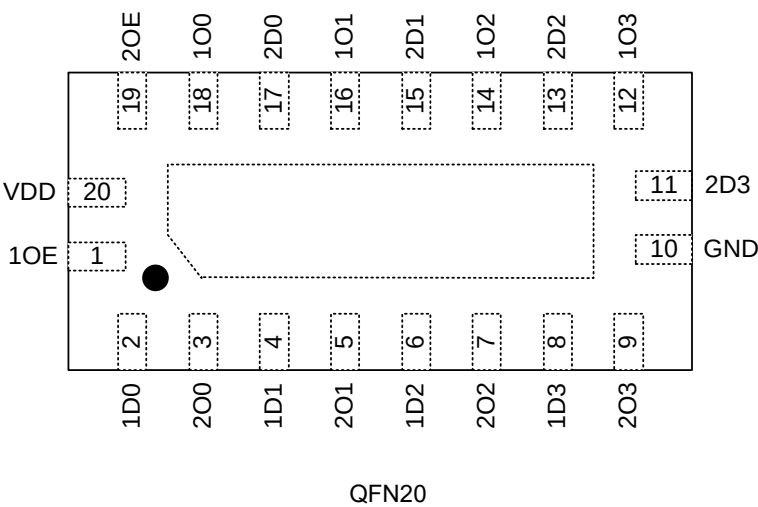
Features

- Designed for 2.3 to 5.5V V_{CC} Operation
- 5V Tolerant-Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10uA) Substantially Reduces System Power Requirements
- Latch up Performance Exceeds 500mA
- ESD Performance:
 - Human Body Model >2000V
 - Machine Model >200V
- These Devices are Pb. Free, Halogen Free/BFR Free and are RoHS Compliant
- Part No. and Package Information

Part No.	Package	MSL
ET74LCX244	QFN20 (2.5mm×3.5mm)	Level 3
ET74LCX244M	SOP20 (12.75mm×10.3mm)	Level 3
ET74LCX244V	TSSOP20 (6.5mm×6.4mm)	Level 3

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Pin Configuration



SOP20/TSSOP20
TOP VIEW
Figure1. Pin Configuration

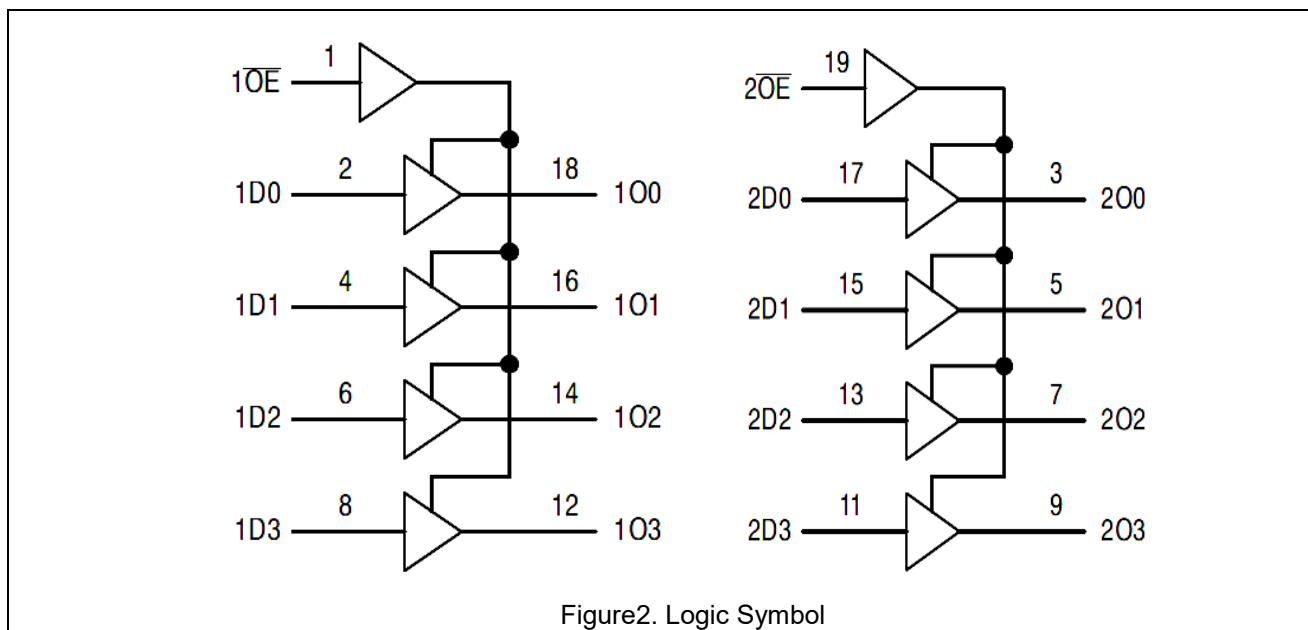
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Pin Function

QFN20/SOP20/TSSOP20

Pin No.	Symbol	Description
1,19	nOE	Output Enable Inputs
2,4,6,8	1Dn	Data Inputs
18,16,14,12	1On	3-State Outputs
17,15,13,11	2Dn	Data Inputs
3,5,7,9	2On	3-State Outputs
10	GND	Ground
20	VCC	Supply Voltage

Block Diagram



Function Table

Input		Output
1OE/2OE	1Dn/2Dn	1On/2On
Low voltage level	Low voltage level	Low voltage level
Low voltage level	High voltage level	High voltage level
High voltage level	High or Low voltage level	High Impedance State

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Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min / Max	Unit
V_{CC}	Supply Voltage		-0.5 to +7.0	V
V_I	Input Voltage		$-0.5 \leq V_I \leq +7.0$	V
V_O	Output Voltage	Output in 3-State	$-0.5 \leq V_O \leq +7.0$	V
		Output in High or Low State ⁽¹⁾	$-0.5 \leq V_O \leq V_{CC}+0.5$	V
I_{IK}	Input Diode Current	$V_I < 0V$	-50	mA
I_{OK}	Output Diode Current	$V_O < 0V$	-50	mA
		$V_O > V_{CC}$	+50	mA
I_O	Output Source/Sink Current		± 50	mA
I_{CC}	Supply Current Per Supply Pin		+100	mA
I_{GND}	Ground Current Per Ground Pin		-100	mA
T_{STG}	Storage Temperature Range		-65 to +150	°C
T_J	Max Junction Temperature		+150	°C
θ_{JA}	Thermal Resistance		140	°C/W

Note1: Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

I_O absolute maximum rating must be observed.

Recommended operating conditions

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating	2.0	2.5, 3.3	5.5	V
		Data Retention Only	1.5	2.5, 3.3	5.5	
V_I	Input Voltage		0		V_{CC}	V
V_O	Output Voltage	HIGH or LOW State	0		V_{CC}	V
		3-State	0		5.5	
I_{OH}	HIGH Level Output Current	$V_{CC} = 3.0V - 5.5V$			-32	mA
		$V_{CC} = 3.0V - 3.6V$			-24	
		$V_{CC} = 2.7V - 3.0V$			-12	
I_{OL}	LOW Level Output Current	$V_{CC} = 3.0V - 5.5V$			32	mA
		$V_{CC} = 3.0V - 3.6V$			24	
		$V_{CC} = 2.7V - 3.0V$			12	
T_A	Operating Free-Air Temperature		-55		+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, $V_{CC} = 3.0V$		0		10	ns/V

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Electrical Characteristics

DC Electrical Characteristics

Symbol	Characteristic	Condition	T _A = -55°C to +125°C		Unit
			Min	Max	
V _{IH}	HIGH Level Input Voltage ⁽²⁾	2.3V ≤ V _{CC} ≤ 2.7V	1.7		V
		2.7V ≤ V _{CC} ≤ 3.6V	2.0		
		3.6V ≤ V _{CC} ≤ 5.5V	3.0		
V _{IL}	LOW Level Input Voltage ⁽²⁾	2.3V ≤ V _{CC} ≤ 2.7V		0.7	V
		2.7V ≤ V _{CC} ≤ 3.6V		0.8	
		3.6V ≤ V _{CC} ≤ 5.5V		1.0	
V _{OH}	HIGH Level Output Voltage	2.3V ≤ V _{CC} ≤ 3.6V, I _{OL} = -100uA	V _{CC} - 0.2		V
		V _{CC} = 2.3V, I _{OH} = -8mA	1.8		
		V _{CC} = 2.7V, I _{OH} = -12mA	2.2		
		V _{CC} = 3.0V, I _{OH} = -18mA	2.4		
		V _{CC} = 5.0V, I _{OH} = -32mA	4.0		
V _{OL}	LOW Level Output Voltage	2.3V ≤ V _{CC} ≤ 3.6V, I _{OL} = 100uA		0.2	V
		V _{CC} = 2.3V, I _{OL} = 8mA		0.6	
		V _{CC} = 2.7V, I _{OL} = 12mA		0.4	
		V _{CC} = 3.0V, I _{OL} = 16mA		0.4	
		V _{CC} = 5.0V, I _{OL} = 32mA		0.6	
I _{OZ}	3-State Output Current	V _{CC} = 5.5V, V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 5.5 V		±5	uA
I _{OFF}	Power Off Leakage Current	V _{CC} = 0V, V _{IN} = 5.5V or V _{OUT} = 5.5V		10	uA
I _{IN}	Input Leakage Current	V _{CC} = 5.5V V _{IN} = 5.5V or GND		±5	uA
I _{CC}	Quiescent Supply Current	V _{CC} = 5.5V V _{IN} = 5.5V or GND		10	uA
ΔI _{CC}	Increase in I _{CC} per Input	2.3V ≤ V _{CC} ≤ 5.5V V _{IH} = V _{CC} - 0.6V		500	uA

Note2: These values of V_I are used to test DC electrical characteristics only.

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AC Electrical Characteristics

($t_R = t_F = 2.5 \text{ ns}$; $R_L = 500\Omega$)

Symbol	Parameter	T _A = -55°C to +125°C								Unit
		V _{CC} = 5.0V		V _{CC} = 3.0V to 3.6V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2		
		C _L = 50pF		C _L = 50pF		C _L = 50pF		C _L = 30pF		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	1.0	6.0	1.5	6.5	1.5	7.5	1.5	7.8	ns
t _{PHL}	Input to Output	1.0	6.0	1.5	6.5	1.5	7.5	1.5	7.8	
t _{PZH}	Output Enable Time to	1.0	6.5	1.5	8.0	1.5	9.0	1.5	10	ns
t _{PZL}	High and Low Level	1.0	6.5	1.5	8.0	1.5	9.0	1.5	10	
t _{PHZ}	Output Disable Time	0.8	5.0	1.5	7.0	1.5	8.0	1.5	8.4	ns
t _{PLZ}	from High and Low Level	0.8	5.0	1.5	7.0	1.5	8.0	1.5	8.4	
t _{OSHL}	Output-to-Output Skew		1.5		1.0					ns
t _{OSLH}	(3)		1.5		1.0					

Note3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Characteristic	Condition	$T_A = 25^\circ\text{C}$			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (4)	$V_{CC} = 5.0\text{V}, C_L = 50\text{pF}, V_{IH} = 5.0\text{V}, V_{IL} = 0\text{V}$		1.6		V
		$V_{CC} = 3.3\text{V}, C_L = 50\text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$		0.8		
		$V_{CC} = 2.5\text{V}, C_L = 30\text{pF}, V_{IH} = 2.5\text{V}, V_{IL} = 0\text{V}$		0.6		
V_{OLV}	Dynamic LOW Valley Voltage (4)	$V_{CC} = 5.0\text{V}, C_L = 50\text{pF}, V_{IH} = 5.0\text{V}, V_{IL} = 0\text{V}$		-1.6		V
		$V_{CC} = 3.3\text{V}, C_L = 50\text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$		-0.8		
		$V_{CC} = 2.5\text{V}, C_L = 30\text{pF}, V_{IH} = 2.5\text{V}, V_{IL} = 0\text{V}$		-0.6		

Note4: Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	$V_{CC} = 3.3\text{V}, V_I = 0\text{V or } V_{CC}$	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3\text{V}, V_O = 0\text{V or } V_{CC}$	8	pF
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3\text{V}, V_I = 0\text{V or } V_{CC}$	25	pF

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PROPAGATION DELAYS

$t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

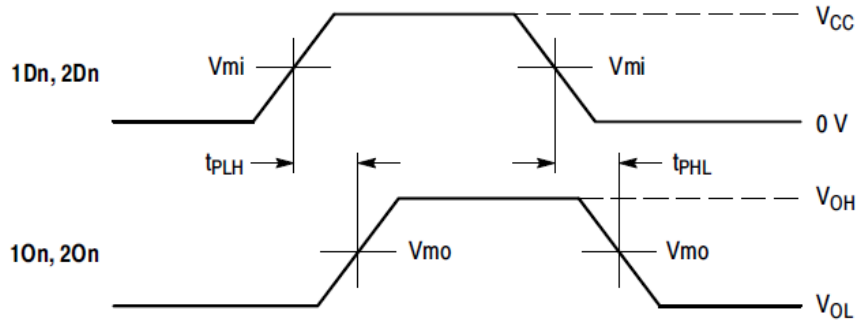


Figure3. t_{PLH} / t_{PHL}

OUTPUT ENABLE AND DISABLE TIMES

$t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

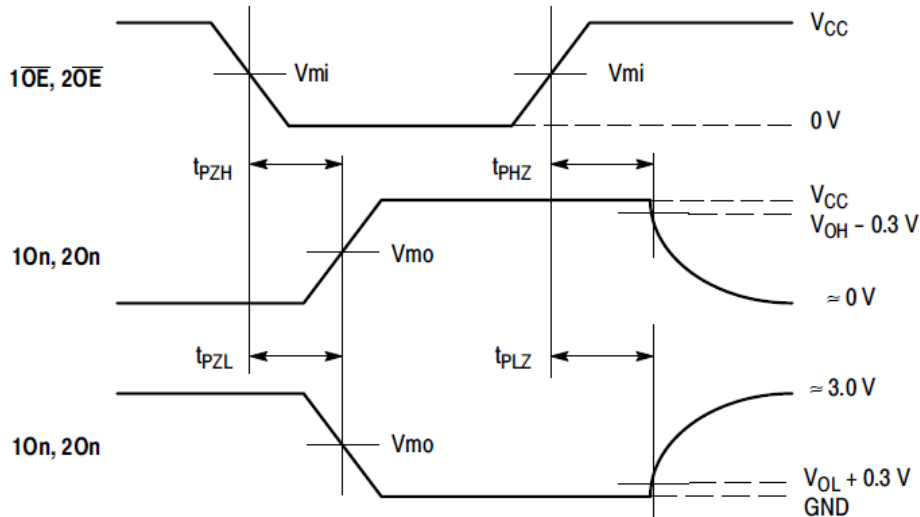
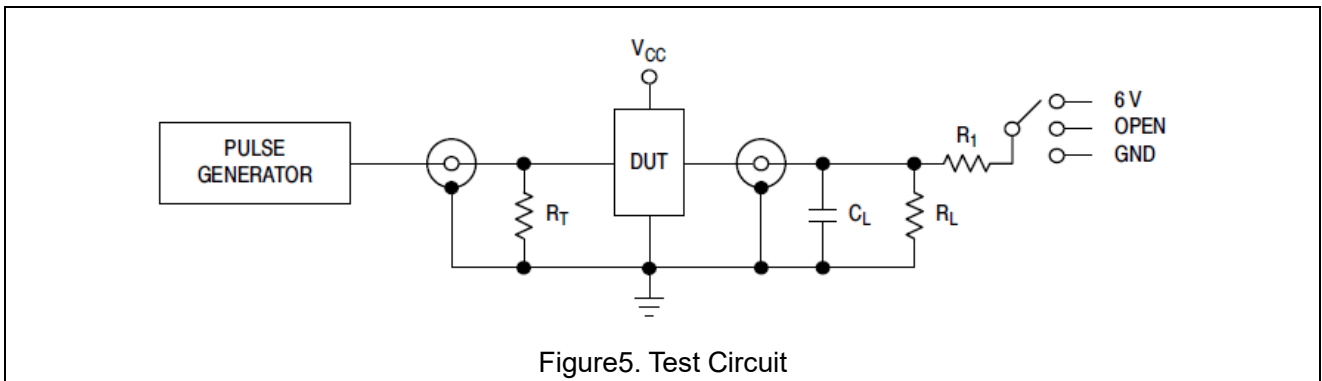


Figure4. $t_{PZH} / t_{PZL} / t_{PHZ} / t_{PLZ}$

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AC Waveforms

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_{HZ}	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15 V$
V_{LZ}	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15 V$



Test Item	Switch Mode
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ 6V at $V_{CC} = 2.5 \pm 0.2V$
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH} , t_{PHZ}	GND

$C_L = 50 \text{ pF}$ at $V_{CC} = 3.3 \pm 0.3 V$ or equivalent (includes jig and probe capacitance)

$C_L = 30 \text{ pF}$ at $V_{CC} = 2.5 \pm 0.2 V$ or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500\Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

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Application Circuits

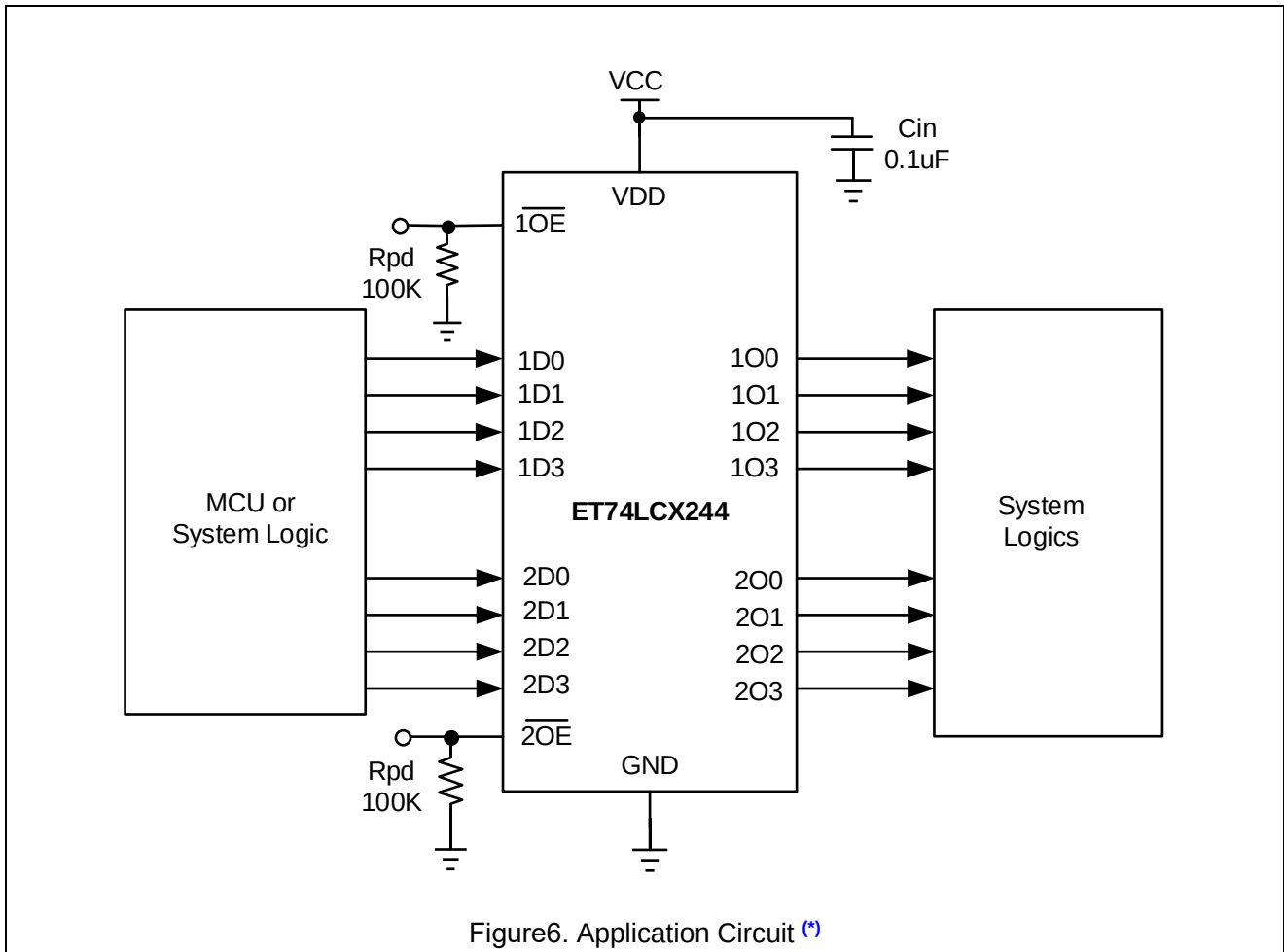


Figure6. Application Circuit (*)

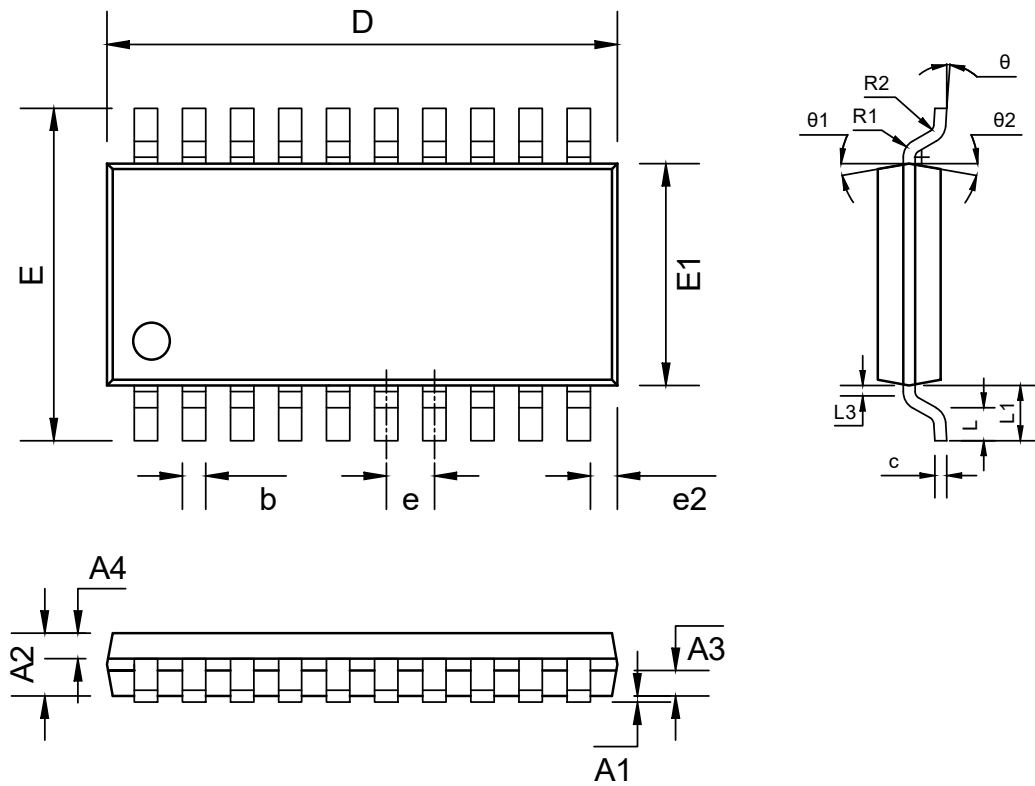
Note: This electric circuit only supplies for reference. It is recommended to ground the unused I/O ports and ensure they are **not left floating**.

Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - For traces longer than 12cm, use impedance controlled traces

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SOP20

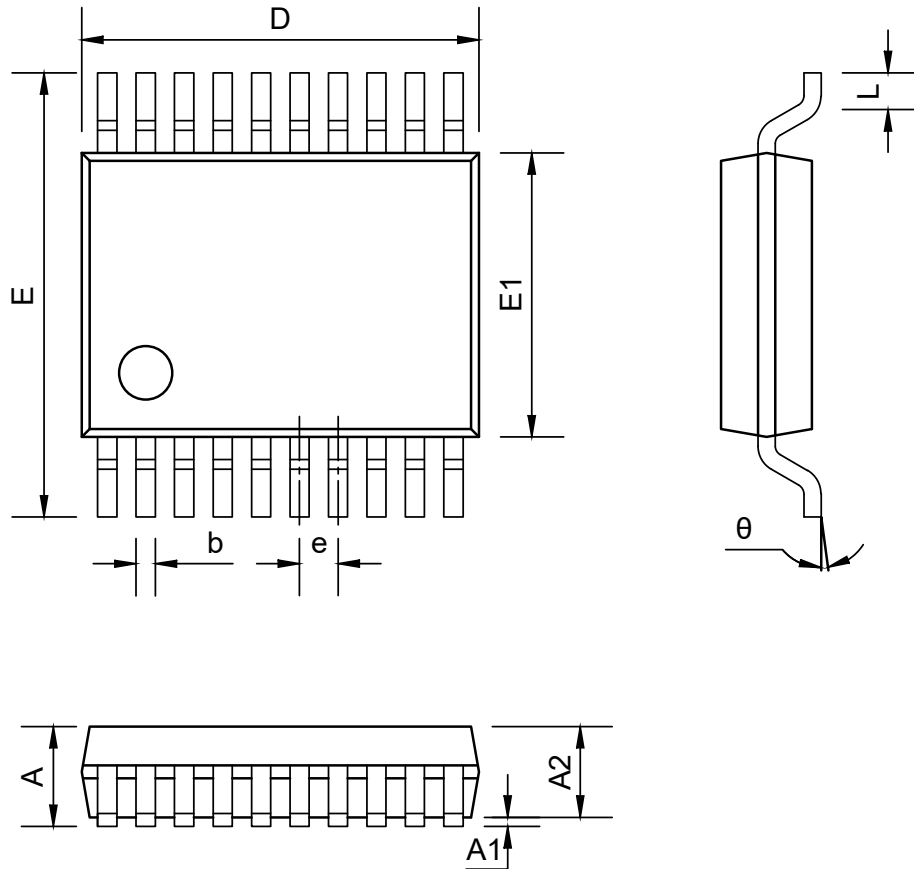


Dimensions Table (Units:mm)

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A1	0.1	0.205	e2	0.45	0.46
A2	2.1	2.5	L	0.764	0.946
A3	0.938	1.038	L1	1.303	1.503
A4	0.938	1.038	L3	0.18REF	
b	0.356	0.456	R1	0.20REF	
c	0.246	0.289	R2	0.30REF	
D	12.5	12.9	θ	0°	10°
E	10.206	10.406	θ1	12°REF	
E1	7.4	7.6	θ2	12°REF	
e	1.24	1.30			

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TSSOP20



Dimensions Table (Units:mm)

SYMBOL	MIN	NOM	MAX
A	--	--	1.20
A1	0.05	--	0.15
A2	0.90	--	1.05
b	0.20	--	0.28
D	6.35	6.45	6.55
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
θ	0°	--	8°

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Marking

74LCX244 XXXXX QFN20 74LCX244-Part Number XXXXXX-Tracking Number	74LCX244M XXXXX SOP20 74LCX244M-Part Number XXXXXX-Tracking Number	74LCX244V XXXXX TSSOP20 74LCX244V-Part Number XXXXXX-Tracking Number
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Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2016-07-29	Original Version	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.1	2016-12-15	Update package dimension	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.2	2022-03-29	Update package	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.3	2022-08-29	Update Typeset	Shi Bo	Shi Liang Jun	Zhu Jun Li
1.4	2024-08-16	Update Marking	Wang Peng	Lu Hao	Liu Jia Ying
1.5	2025-09-16	Update Application Circuit	Wang Peng	Lu Hao	Liu Jia Ying
1.6	2025-10-29	Update EC Table	Yang Xiao Xu	Lu Hao	Liu Jia Ying
1.6.a	2026-05-18	Add Unused Pin Note	Yang Xiao Xu	Lu Hao	Liu Jia Ying