

## 3A, Low-noise (6 $\mu$ V) Voltage Regulator

### General Description

The ET5C001YB is a low-noise (6 $\mu$ V<sub>RMS</sub>), low-dropout voltage regulator (LDO) capable of sourcing a 3A load with low dropout. The output voltages are fully user-adjustable using a printed circuit board (PCB) layout without the need of external resistors, thus reducing overall component count. For higher output voltage applications, the device achieves output voltages up to 5V with the use of external resistors. The device supports very low input voltages (down to 1.1V) with the use of an additional BIAS rail.

With very high accuracy, remote sensing, and soft-start capabilities to reduce inrush current, the ET5C001YB is ideal for powering high-current, low-voltage devices such as high-end microprocessors and field-programmable gate arrays.

The ET5C001YB is designed to power-up noise-sensitive components in high-speed communication applications. The very low-noise, 6 $\mu$ V<sub>RMS</sub> device output and high broad-bandwidth PSRR minimizes phase noise and clock jitter in high-frequency signals. These features maximize performance of clocking devices, analog-to-digital converters, and digital-to-analog converters.

### Features

- Ultra-low Dropout: 260mV Maximum at 3A
- Output Voltage Noise: 6 $\mu$ V<sub>RMS</sub>
- Power-Supply Ripple Rejection: 80dB at 1KHz, 0.8V & 30mA
- Input Voltage Range: Without BIAS: 1.4V to 5.5V; With BIAS: 1.1V to 5.5V
- Two Output Voltage Modes:
  - Programmable output Version: Output Voltage Range: 0.8V to 3.95V
  - Adjustable Version: Output Voltage Range: 0.8V to 5.0V
- 1.0% Accuracy Over Line, Load, and Temperature
- Programmable Soft-Start Output
- Power-Good (PG) Output
- Built-in Under Voltage Lockout (UVLO)
- Built-in Internal Current Limit
- Package Information:

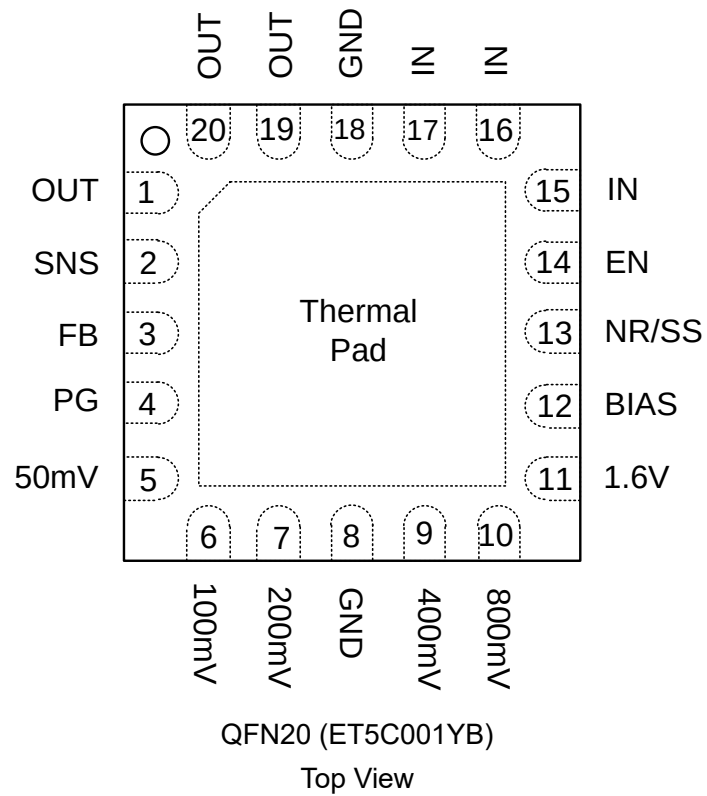
| Part No.  | Package           | MSL     |
|-----------|-------------------|---------|
| ET5C001YB | QFN20 (5mm × 5mm) | Level 3 |

# ET5C001YB

## Applications

- RF, IF Components: VCO, ADC, DAC, LVDS
- Wireless Infrastructure: FPGA, DSP
- Test and Measurement
- Instrumentation, Medical, and Audio

## Pin Configuration



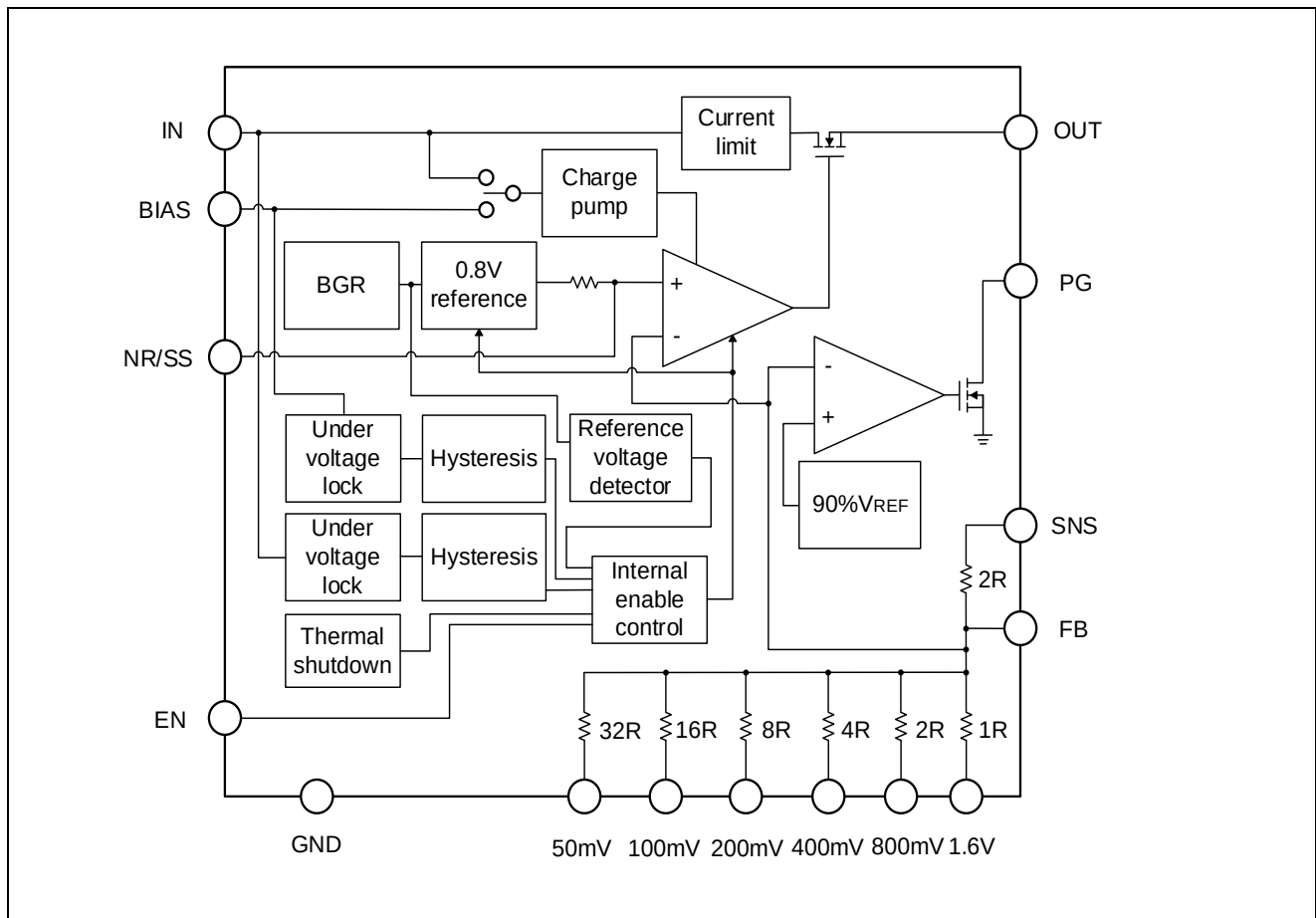
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## Pin Function

| Pin No.       | Pin Name                                        | Pin Function                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------------|-------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1,19,20       | OUT                                             | Regulated output pin. A ceramic capacitor is required for stability.                                                                                                                                                                                                                                                                                                                                                |
| 2             | SNS                                             | Output voltage sense input pin. Connect this pin only if the Programmable output feature is used.                                                                                                                                                                                                                                                                                                                   |
| 3             | FB                                              | Output voltage feedback pin connected to the error amplifier. Although not required, a 10nF feed-forward capacitor from FB to OUT (as close to the device as possible) is recommended for low-noise applications to maximize ac performance. The use of a feed-forward capacitor may disrupt PG (power good) functionality. See the Programmable Output Voltage and Adjustable Operation sections for more details. |
| 4             | PG                                              | Active-high power-good pin. An open-drain output indicates when the output voltage reaches the target. The use of a feed-forward capacitor may disrupt PG functionality.                                                                                                                                                                                                                                            |
| 5,6,7,9,10,11 | 50mV, 100mV,<br>200mV,<br>400mV,<br>800mV, 1.6V | Output voltage setting pins. Connect these pins to ground or leave floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) when not in use. See the Programmable Output Voltage section for more details.                                  |
| 8,18          | GND                                             | Ground pin.                                                                                                                                                                                                                                                                                                                                                                                                         |
| 12            | BIAS                                            | BIAS supply voltage pin for the use of $1.1V \leq IN \leq 1.4V$ and to connect a 10 $\mu$ F capacitor between this pin and ground.                                                                                                                                                                                                                                                                                  |
| 13            | NR/SS                                           | Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a capacitor is recommended for low-noise applications to connect a 10nF capacitor from NR/SS to GND (as close to the device as possible) to maximize ac performance.                                              |
| 14            | EN                                              | Enable pin. Driving this pin to logic high enables the device; Driving this pin to logic low disables the device. See the Start-Up section for more details.                                                                                                                                                                                                                                                        |
| 15,16,17      | IN                                              | Input supply voltage pin. A 10 $\mu$ F input ceramic capacitor is required.                                                                                                                                                                                                                                                                                                                                         |
|               | Thermal Pad                                     | Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.                                                                                                                                                                                                                                                                                                               |

**ET5C001YB**

## Block Diagram



## Functional Description

## Overview

The ET5C001YB is a low-noise, high PSRR, low-dropout regulator capable of sourcing a 3A load with low dropout. The ET5C001YB can operate down to 1.1V input voltage and 0.8V output voltage. This combination of low noise, high PSRR, and low output voltage makes the device an ideal low dropout regulator to power a multitude of loads from noise-sensitive communication components in high-speed communication applications to high-end microprocessors or field-programmable gate array.

The ET5C001YB block diagram contains several features, including:

- With an internal charge pump;
- Low-noise, 0.8V reference;
- Internal protection circuitry: UVLO, Internal current limit, TSD;
- Programmable soft-start;
- Power-good output;
- An integrated resistance network (Programmable output) with a 50mV minimum resolution.

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## Device Functional Modes

- Operation with  $1.1V < V_{IN} < 1.4V$

The ET5C001YB requires a bias voltage on the BIAS pin  $\geq 3.0V$  if the high-current input supply voltage is between 1.1V to 1.4V. The bias voltage pin consumes 2.3mA, nominally.

- Operation with  $1.4V \leq V_{IN} < 5.5V$

If the input voltage is equal to, or exceeds 1.4V, no bias voltage is necessary. The device is automatically selected to be powered from the IN pin in this condition and the BIAS pin can be left floating.

- Disabled

If the voltage on the EN pin is less than 0.5V, the device is disabled and the output is high impedance. The output impedance of the LDO is then set by the gain setting resistors if a path to GND is provided between OUT and GND. In this state, quiescent current does not exceed 2.5 $\mu$ A. Raising EN above 1.1V (maximum) initiates the startup sequence of the device.

## Start-Up

- Enable (EN) and Under voltage Lockout (UVLO)

The ET5C001YB only turns on when both EN and UVLO are above the respective voltage thresholds. The UVLO circuit monitors input and bias voltage ( $V_{IN}$  and  $V_{BIAS}$ , respectively) to prevent device turn-on before  $V_{IN}$  and  $V_{BIAS}$  rise above the lockout voltage. The UVLO circuit also causes a shutdown when  $V_{IN}$  and  $V_{BIAS}$  fall below lockout. The EN signal allows independent logic-level turn-on and shutdown of the LDO. If the device turn-on is required to be controlled, the device must be enabled with or after  $V_{IN}$ . Connect EN to  $V_{IN}$  if turn-on control of the output voltage is not needed.

- Noise-Reduction and Soft-Start Capacitor ( $C_{NR/SS}$ )

The ET5C001YB features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ( $C_{NR/SS}$ ). This soft-start eliminates power-up initialization problems when powering field-programmable gate arrays (FPGAs), digital signal processors (DSPs), or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a linear and monotonic start-up, the ET5C001YB error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current ( $I_{NR/SS}$ ), the soft-start capacitance ( $C_{NR/SS}$ ), and the internal reference ( $V_{REF}$ ). Soft-start ramp time can be calculated as followed:

$$t_{SS} = (V_{REF} \times C_{NR/SS}) / I_{NR/SS}$$

**Note:** That  $I_{NR/SS}$  is provided in the Electrical Characteristics table and has a typical value of 6.2  $\mu$ A

For low-noise applications, the noise-reduction capacitor (connected to the NR/SS pin of the LDO) forms an RC filter for filtering out noise that is ordinarily amplified by the control loop and appears on the output voltage. For low-noise applications, a 10nF to 1 $\mu$ F  $C_{NR/SS}$  is recommended.

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- Soft-Start and Inrush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO achieve threshold voltage. The noise-reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

Inrush current is defined as the current into the LDO at the IN pin during start-up. Inrush current then consists primarily of the sum of load and current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended.

## Feature Description

### Programmable Output Operation

The ET5C001YB does not require external resistors to set output voltage, which is typical of adjustable low-dropout voltage regulators. However, the ET5C001YB uses pins 5, 6, 7, 9, 10, and 11 to program the regulated output voltage. Each pin is either connected to ground (active) or left open (floating). Programmable output programming is set by Equation below as the sum of the internal reference voltage ( $V_{REF}=0.8V$ ) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 50mV (pin5), 100mV (pin6), 200mV (pin7), 400mV (pin9), 800mV (pin10), or 1.6V (pin11). By leaving all program pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to  $V_{REF}$ .

$$V_{OUT}=V_{REF}+(\sum \text{Pins to Ground})$$

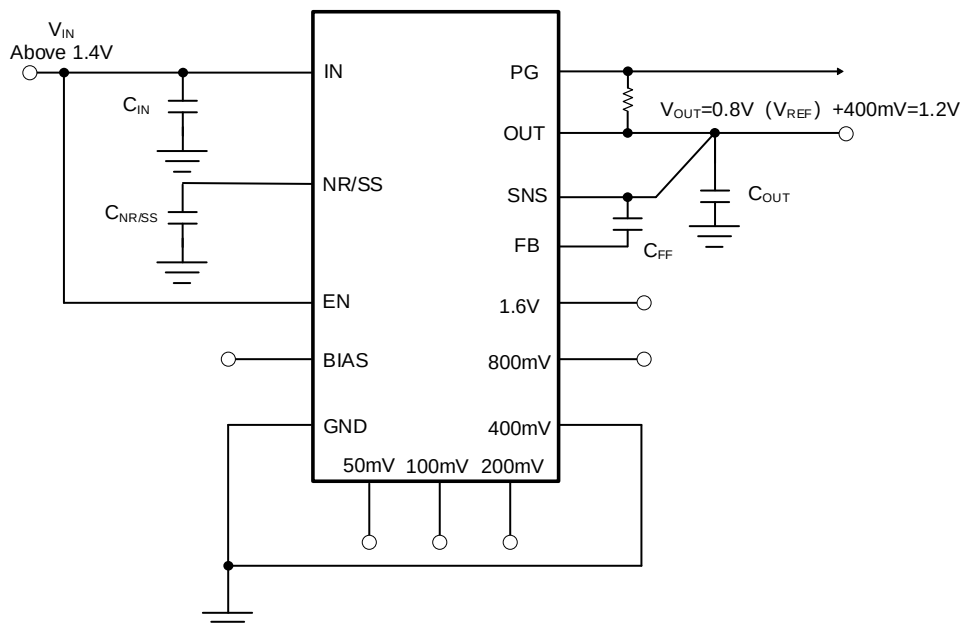
| PROGRAM PINS (Active Low) | ADDITIVE OUTPUT VOLTAGE LEVEL |
|---------------------------|-------------------------------|
| Pin 5 (50mV)              | 50mV                          |
| Pin 6 (100mV)             | 100mV                         |
| Pin 7 (200mV)             | 200mV                         |
| Pin 9 (400mV)             | 400mV                         |
| Pin 10 (800mV)            | 800mV                         |
| Pin 11 (1.6V)             | 1.6V                          |

The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 0.8V to 3.95V in 50mV steps. As followed: Binary 0 means the pin is open, Binary 1 means the pin is connected to GND.

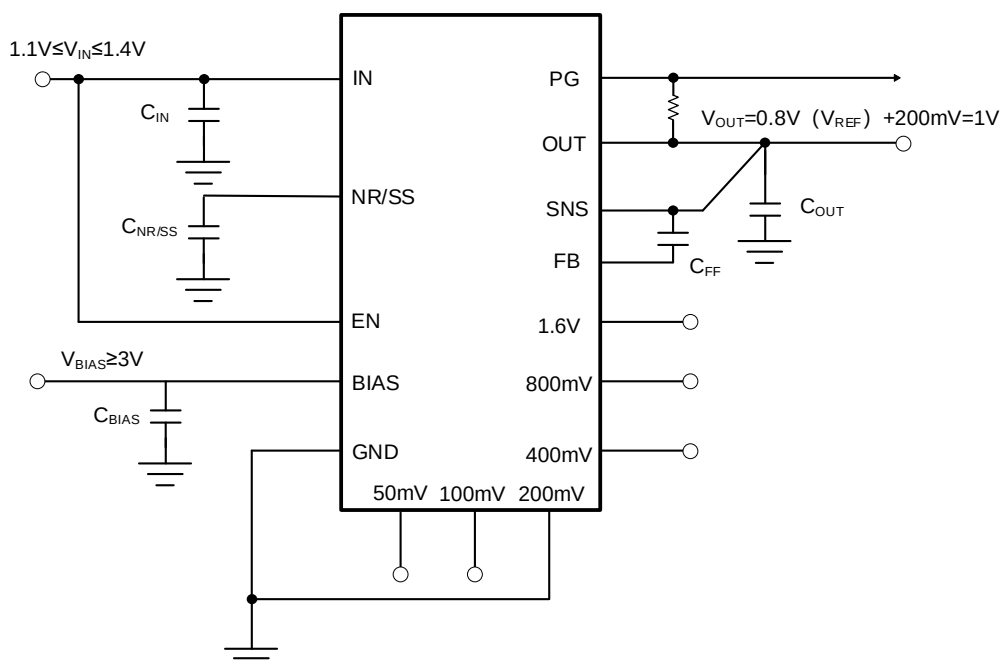
| {1.6V,800mv, 400mv, 200mv, 100mv, 50mv} | Output Voltage(V) |
|-----------------------------------------|-------------------|
| 00_0000(default)                        | 0.80              |
| 00_0001                                 | 0.85              |
| 00_0010                                 | 0.90              |
| .....                                   | .....             |
| 10_0000                                 | 2.40              |
| 10_0001                                 | 2.45              |
| 10_0010                                 | 2.50              |
| .....                                   | .....             |
| 11_1101                                 | 3.85              |
| 11_1110                                 | 3.90              |
| 11_1111                                 | 3.95              |

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Considering the use of the programmable output internal network, the output voltage is set by grounding the appropriate control pins. When grounded, all control pins add a specific voltage on top of the internal reference voltage ( $V_{REF}=0.8V$ ). The followed figures show a 1.2V and 1V output voltage, respectively, that provide an example of the circuit usage with and without BIAS voltage. These schematics are described in more detail in the Application Circuits.



Typical application:  $V_{IN} \geq 1.4V$  (1.4V Input, 1.2V Output, no external BIAS)

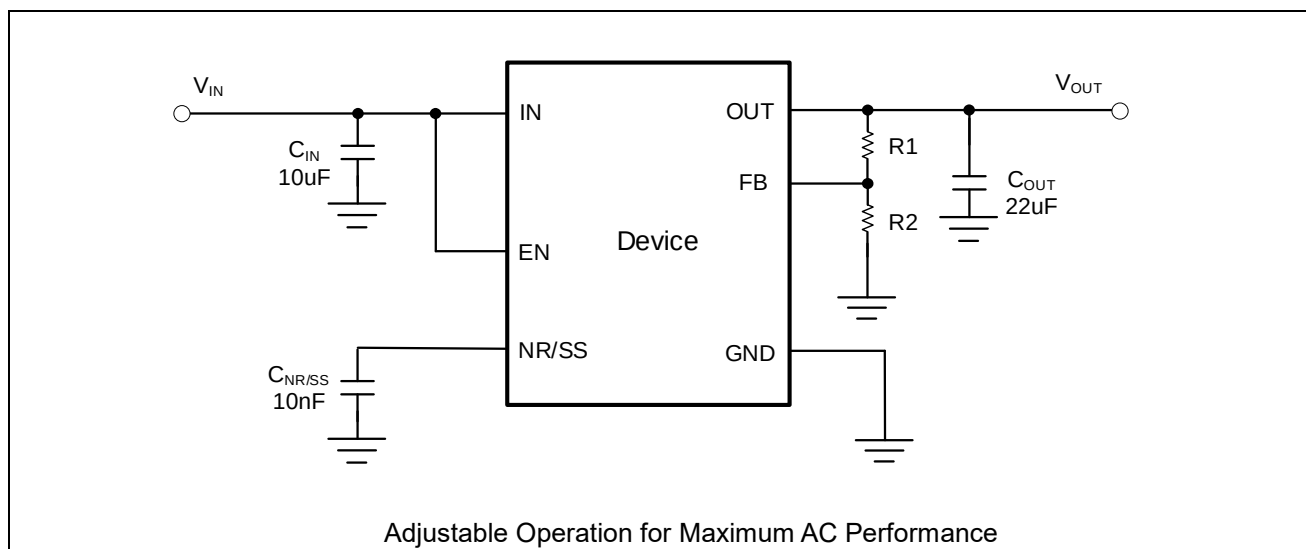


Typical application:  $1.1V \leq V_{IN} < 1.4V$  (1.1V Input, 1.0V Output, 3V BIAS voltage)

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## Adjustable Operation

The ET5C001YB can be used either with the internal programmable output network or using external resistors. Using the programmable output network allows the ET5C001YB to be programmed from 0.8V to 3.95V. To extend this range of output voltage operation to 5.0V, external resistors must be used. This configuration is referred to as the adjustable configuration of the ET5C001YB throughout this document. Regardless whether the internal resistor network or whether external resistors are used, the nominal output voltage of the device is set by two resistors. Using an internal resistor ensures a 1% matching and minimizes both the number of external components and layout footprint.



R1 and R2 can be calculated for any output voltage range using followed Equation. This resistive network must provide a current equal to or greater than 5μA for optimum noise performance.

$$R_1 = R_2 \left( \frac{V_{OUT}}{V_{REF}} - 1 \right), \text{ where } \frac{|V_{REF(max)}|}{R_2} > 5\mu A$$

Recommended feedback resistor values (R1+R2) <150KΩ.

## 3A LDO with an Internal Charge Pump

The ET5C001YB can be used either with the internal resistor network provided, or with the external component as a traditional adjustable LDO. Regardless of the implementation, the ET5C001YB provides excellent regulation to 1% accuracy, excellent dropout voltage, and high output current capability.

If the input voltage is below 1.4V, an external BIAS voltage must be supplied to maintain the dropout characteristics. The input voltage or the BIAS voltage is fed through to an internal charge pump to power the internal error amplifier providing the regulation.

The internal charge pump ensures proper operation without requiring an external BIAS voltage down to 1.4V input voltage. Below a 1.4V input voltage, a BIAS input voltage between 3.0V and 5.5V is required.

## Low-Noise, 0.8-V Reference

The ET5C001YB includes a low-noise reference ensuring minimal noise during operation because the internal reference is normally the dominant term in noise analysis. Further noise reduction can be achieved using the NR/SS pin and by adding an external C<sub>FF</sub> between the SNS pin and the FB pin.



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## Under voltage Lockout (UVLO)

The under-voltage lockout (UVLO) circuit monitors the input and bias voltage ( $V_{IN}$  and  $V_{BIAS}$ , respectively) to prevent the device from turning on before  $V_{IN}$  and  $V_{BIAS}$  rise above the lockout voltage. The UVLO circuit also causes a shutdown when  $V_{IN}$  and  $V_{BIAS}$  fall below the lockout voltage.

## Internal Current Limit ( $I_{LIMIT}$ )

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

A fold back feature limits the short-circuit current to protect the regulator from damage under all load conditions. If OUT is forced below 0 V before EN goes high and the load current required exceeds the fold back current limit, the device does not start up. In applications that function with both a positive and negative voltage supply, there are several ways to ensure proper start-up:

- Enable the ET5C001YB first and disable the device last.
- When power is off, EN voltage turned off first allows the internal pull-down resistor to discharge any residual voltage at OUT. If a faster discharge rate is required, use an external resistor from OUT to GND.

## Thermal Shutdown Protection (TSD)

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the ET5C001YB has been designed to protect against temporary thermal overload conditions. The TSD circuitry was not intended to replace proper heat-sinking. Continuously running the ET5C001YB device into thermal shutdown may degrade device reliability

## Programmable Soft-Start

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO exceed the respective threshold voltage. The noise-reduction capacitor ( $C_{NR/SS}$ ) serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

## Power-Good Function

The ET5C001YB has a power-good function that works by toggling the state of the PG output pin. When the output voltage falls below the PG threshold voltage, the PG pin open-drain output engages (low impedance to GND). When the output voltage exceeds the PG threshold voltage by an amount greater than  $V_{HYS}$  (PG), the PG pin becomes high-impedance. By connecting a pull-up resistor to an external supply, any downstream device can receive PG as a logic signal. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices. Use a pull-up resistor from 10kΩ to 100kΩ for best results.

When employing the feed-forward capacitor ( $C_{FF}$ ), the turn-on time-constant for the LDO is increased and the

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power-good output time-constant stays the same, resulting in an invalid status of the LDO. To avoid this issue and receive a valid PG output, ensure that the time-constant of both the LDO and the power-good output match.

## Capacitor Recommendation

The ET5C001YB is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR, pin13). Ceramic capacitors that employ X7R, X5R, and COG rated dielectric materials provide relatively good capacitive stability across temperature.

- Input and Output Capacitor Requirements ( $C_{IN}$  and  $C_{OUT}$ )

The ET5C001YB is designed and characterized for operation with ceramic capacitors of 22 $\mu$ F or greater at the output and 10 $\mu$ F at the input. Locate the input and output capacitors as near as practical to the respective input and output pins.

- Feed-Forward Capacitor ( $C_{FF}$ )

Although a feed-forward capacitor ( $C_{FF}$ ), from the FB pin to the OUT pin is not required to achieve stability, a 10nF, feed-forward capacitor optimizes the noise and PSRR performance. A higher capacitance  $C_{FF}$  can be used; However, the startup time is longer and the power-good signal may incorrectly indicate the output voltage has settled.

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## Absolute Maximum Ratings

| Symbol                          | Parameters (Items)                             | Value                 | Unit                 |
|---------------------------------|------------------------------------------------|-----------------------|----------------------|
| $V_{IN}/V_{BIAS}/V_{PG}/V_{EN}$ | IN, BIAS, PG, EN Voltage                       | -0.3 to 6             | V                    |
| $V_{SNS}/V_{OUT}$               | SNS, Output Voltage                            | -0.3 to $V_{IN}+0.3$  | V                    |
| $V_{NR/SS}/V_{FB}$              | NR/SS, FB Output Voltage                       | -0.3 to 3.6           | V                    |
| $V_{OTHER\_PINS}$               | 50mV, 100mV, 200mV, 400mV, 800mV, 1.6V Voltage | -0.3 to $V_{OUT}+0.3$ | V                    |
| $I_{OUT\_MAX}$                  | Maximum Load Current                           | 3000                  | mA                   |
| $I_{PG\_MAX}$                   | PG (sink current into device)                  | 5                     | mA                   |
| $P_D$                           | Maximum Power Consumption QFN20(5*5)           | 2000                  | mW                   |
| $V_{ESD}$                       | Human Body Model (JESD22-A114)                 | $\pm 2000$            | V                    |
|                                 | Charged Device Model (JESD22-C101)             | $\pm 2000$            |                      |
| $R_{\theta JA}$                 | Junction-to-ambient Thermal Resistance         | 62.5                  | $^{\circ}\text{C/W}$ |
| $T_J$                           | Operating Junction Temperature                 | -40 to 150            | $^{\circ}\text{C}$   |
| $T_{STG}$                       | Storage Temperature                            | -65 to 150            | $^{\circ}\text{C}$   |
| $T_{SLOD}$                      | Lead Temperature (Soldering, 10 sec)           | 300                   | $^{\circ}\text{C}$   |

## Recommended Operating Conditions

| Symbol     | Parameters                                                    | Rating     | Unit               |
|------------|---------------------------------------------------------------|------------|--------------------|
| $V_{IN}$   | Input Voltage                                                 | 1.1 to 5.5 | V                  |
| $V_{BIAS}$ | Supply Bias Voltage                                           | 3.0 to 5.5 | V                  |
| $I_{OUT}$  | Output Current                                                | 0 to 3000  | mA                 |
| $T_A$      | Operating Ambient Temperature                                 | -40 to 85  | $^{\circ}\text{C}$ |
| $C_{IN}$   | Effective Input Ceramic Capacitor Value                       | Min 10     | $\mu\text{F}$      |
| $C_{BIAS}$ | Effective Input Ceramic Capacitor Value                       | Min 10     | $\mu\text{F}$      |
| $C_{OUT}$  | Effective Output Ceramic Capacitor Value                      | Min 22     | $\mu\text{F}$      |
| ESR        | Input and Output Capacitor Equivalent Series Resistance (ESR) | 5 to 100   | $\text{m}\Omega$   |

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## Electrical Characteristics

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $\{1.1\text{V} \leq V_{IN} < 1.4\text{V}$  and  $3.0\text{V} \leq V_{BIAS} \leq 5.5\text{V}\}$  or  $\{V_{IN} \geq 1.4\text{V}$  and  $V_{BIAS}$  open<sup>(1)</sup>,  $V_{IN} \geq V_{OUT(TARGET)} + 0.3\text{V}$ <sup>(2)</sup>,  $V_{OUT(TARGET)} = 0.8\text{V}$ , OUT connected to  $50\Omega$  to GND<sup>(3)</sup>,  $V_{EN} = 1.1\text{V}$ ,  $C_{OUT} = 22\mu\text{F}$ ,  $C_{NR/SS} = 0\text{nF}$ ,  $C_{FF} = 0\text{nF}$ , and PG pin pulled up to  $V_{IN}$  with  $100\text{k}\Omega$ , unless otherwise noted.

| Symbol           | Parameters                                | Conditions                                                                                                                                              | Min      | Typ    | Max       | Unit |
|------------------|-------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------|-----------|------|
| $V_{IN}$         | Input Voltage Range                       |                                                                                                                                                         | 1.1      |        | 5.5       | V    |
| $V_{BIAS}$       | Bias Supply Voltage <sup>(1)</sup>        |                                                                                                                                                         | 3.0      |        | 5.5       | V    |
| $V_{REF}$        | Reference Voltage                         | $V_{REF} = V_{FB} = V_{NR/SS}$                                                                                                                          |          | 0.8    |           | V    |
| $V_{UVLO1(IN)}$  | Input Supply UVLO With BIAS               | $V_{IN}$ Increasing                                                                                                                                     |          | 1.02   | 1.085     | V    |
| $V_{HYS1(IN)}$   | $V_{UVLO1(IN)}$ Hysteresis                | $V_{IN}$ Falling                                                                                                                                        |          | 0.2    |           | V    |
| $V_{UVLO2(IN)}$  | Input Supply UVLO Without BIAS            | $V_{IN}$ Increasing                                                                                                                                     |          | 1.25   | 1.35      | V    |
| $V_{HYS2(IN)}$   | $V_{UVLO2(IN)}$ Hysteresis                | $V_{IN}$ Falling                                                                                                                                        |          | 250    |           | mV   |
| $V_{UVLO(BIAS)}$ | Bias Supply UVLO                          | $V_{BIAS}$ Increasing                                                                                                                                   |          | 2.83   | 2.9       | V    |
| $V_{HYS(BIAS)}$  | $V_{UVLO(BIAS)}$ Hysteresis               | $V_{BIAS}$ Falling                                                                                                                                      |          | 290    |           | mV   |
| $V_{OUT}$        | Output Voltage                            | Using Voltage Setting Pins(50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V)                                                                                  | 0.8-1.0% |        | 3.95+1.0% | V    |
|                  |                                           | Using External Resistors                                                                                                                                | 0.8-1.0% |        | 5.0+1.0%  |      |
|                  | Output Voltage Accuracy <sup>(4)(5)</sup> | $0.8\text{V} \leq V_{OUT} \leq 5\text{V}$ ,<br>$5\text{mA} \leq I_{OUT} \leq 3\text{A}$                                                                 | -1.0%    |        | 1.0%      |      |
|                  |                                           | $V_{IN} = 1.5\text{V}$ , $V_{OUT} = 1.2\text{V}$ ,<br>$5\text{mA} \leq I_{OUT} \leq 1.2\text{A}$                                                        | -1.0%    |        | 1.0%      |      |
| $\Delta V_{OUT}$ | Output Voltage Line Regulation            | $V_{IN} = 1.4\text{V}$ to $5.5\text{V}$ ,<br>$I_{OUT} = 5\text{mA}$                                                                                     |          | 0.003  |           | %/V  |
|                  | Output Voltage Load Regulation            | $I_{OUT}$ from 5mA to 3000mA                                                                                                                            |          | 0.0001 |           | %/A  |
| $V_{DROP}$       | Dropout Voltage                           | $V_{IN} \geq 1.4\text{V}$ and $V_{BIAS}$ Open,<br>$0.8\text{V} \leq V_{OUT} \leq 5.0\text{V}$ ,<br>$I_{OUT} = 3\text{A}$ , $V_{FB} = 0.8\text{V} - 3\%$ |          | 160    | 320       | mV   |
|                  |                                           | $V_{IN} = 1.1\text{V}$ , $V_{BIAS} = 5.0\text{V}$ ,<br>$V_{OUT(TARGET)} = 0.8\text{V}$ ,<br>$I_{OUT} = 3\text{A}$ , $V_{FB} = 0.8\text{V} - 3\%$        |          | 130    | 260       |      |
| $I_{LIMIT}$      | Current Limit                             | $V_{OUT}$ Forced at<br>$0.9 \times V_{OUT(TARGET)}$ ,<br>$V_{IN} = V_{OUT(TARGET)} + 300\text{mV}$                                                      | 3300     | 4300   | 5300      | mA   |

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## Electrical Characteristics (Continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $\{1.1\text{V} \leq V_{IN} < 1.4\text{V}$  and  $3.0\text{V} \leq V_{BIAS} \leq 5.5\text{V}\}$  or  $\{V_{IN} \geq 1.4\text{V}$  and  $V_{BIAS}$  open<sup>(1)</sup>,  $V_{IN} \geq V_{OUT(TARGET)} + 0.3\text{V}$ <sup>(2)</sup>,  $V_{OUT(TARGET)} = 0.8\text{V}$ , OUT connected to  $50\Omega$  to GND<sup>(3)</sup>,  $V_{EN} = 1.1\text{V}$ ,  $C_{OUT} = 22\mu\text{F}$ ,  $C_{NR/SS} = 0\text{nF}$ ,  $C_{FF} = 0\text{nF}$ , and PG pin pulled up to  $V_{IN}$  with  $100\text{k}\Omega$ , unless otherwise noted.

| Symbol                | Parameters                          | Conditions                                                                                                                                                                     | Min                  | Typ                  | Max                  | Unit               |
|-----------------------|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------|----------------------|--------------------|
| I <sub>GND</sub>      | GND Pin Current                     | Minimum Load, $V_{IN} = 5.5\text{V}$ , no $V_{BIAS}$ Supply, $I_{OUT} = 5\text{mA}$                                                                                            |                      | 2.8                  | 4                    | mA                 |
|                       |                                     | Maximum Load, $V_{IN} = 1.4\text{V}$ , no $V_{BIAS}$ Supply, $I_{OUT} = 3\text{A}$                                                                                             |                      | 3.7                  | 5                    |                    |
|                       |                                     | Shutdown, PG=(open), $V_{IN} = 4.3\text{V}$ , no $V_{BIAS}$ Supply, $V_{EN} = 0\text{V}$                                                                                       |                      |                      | 2.5                  | $\mu\text{A}$      |
| I <sub>EN</sub>       | EN Pin Input Current                | $V_{IN} = 5.5\text{V}$ , no $V_{BIAS}$ Supply, $V_{EN} = 0\text{V}$ and $5.5\text{V}$                                                                                          | -0.1                 |                      | 0.1                  | $\mu\text{A}$      |
| I <sub>BIAS</sub>     | BIAS Pin Current                    | $V_{IN} = 1.1\text{V}$ , $V_{BIAS} = 5.5\text{V}$ , $V_{OUT(TARGET)} = 0.8\text{V}$ , $I_{OUT} = 3\text{A}$                                                                    |                      | 2.3                  | 3.5                  | mA                 |
| V <sub>IL(EN)</sub>   | En Low Threshold                    | $V_{EN}$ Falling from $1.2\text{V}$                                                                                                                                            | 0                    |                      | 0.5                  | V                  |
| V <sub>IH(EN)</sub>   | En High Threshold                   | $V_{EN}$ Increasing from $0\text{V}$                                                                                                                                           | 1.1                  |                      | 5.5                  | V                  |
| V <sub>IT(PG)</sub>   | PG Pin Threshold                    | For the Direction PG with Decreasing $V_{OUT}$                                                                                                                                 | $0.82 \cdot V_{OUT}$ | $0.87 \cdot V_{OUT}$ | $0.93 \cdot V_{OUT}$ | V                  |
| V <sub>HYS(PG)</sub>  | PG Pin Hysteresis                   |                                                                                                                                                                                |                      | $0.02 \cdot V_{OUT}$ |                      | V                  |
| V <sub>OL(PG)</sub>   | PG Pin Low-Level Output Voltage     | $V_{OUT} < V_{IT(PG)}$ , $I_{PG} = -1\text{mA}$ (Current into Device)                                                                                                          |                      |                      | 0.4                  | V                  |
| I <sub>LEAK(PG)</sub> | PG Pin Leakage Current              | $V_{OUT} > V_{IT(PG)}$ , $V_{(PG)} = 5.5\text{V}$                                                                                                                              |                      |                      | 1                    | $\mu\text{A}$      |
| I <sub>NR/SS</sub>    | NR/SS Pin Charging Current          | $V_{NR/SS} = \text{GND}$ , $V_{IN} = 5.5\text{V}$                                                                                                                              | 4.0                  | 6.2                  | 9.0                  | $\mu\text{A}$      |
| I <sub>FB</sub>       | FB Pin Leakage Current              | $V_{IN} = 5.5\text{V}$                                                                                                                                                         | -100                 |                      | 100                  | nA                 |
| PSRR                  | Power Supply Rejection Ratio        | $f = 1\text{KHz}$ , $V_{IN} = 1.1\text{V}$ , $V_{BIAS} = 3.0\text{V}$ , $V_{OUT} = 0.8\text{V}$ , $I_{OUT} = 30\text{mA}$ , $C_{NR/SS} = 10\text{nF}$ , $C_{FF} = 10\text{nF}$ |                      | 80                   |                      | dB                 |
| e <sub>N</sub>        | Output Noise                        | $f = 10\text{Hz}$ to $100\text{kHz}$ , $V_{IN} = 1.4\text{V}$ , $V_{OUT} = 0.8\text{V}$ , $I_{OUT} = 1.5\text{A}$ , $C_{NR/SS} = 10\text{nF}$ , $C_{FF} = 10\text{nF}$         |                      | 6                    |                      | $\mu\text{V}$      |
| T <sub>TSD</sub>      | Over-Temperature Shutdown Threshold | T <sub>J</sub> Rising                                                                                                                                                          |                      | 160                  |                      | $^{\circ}\text{C}$ |
|                       |                                     | T <sub>J</sub> Falling from Shutdown                                                                                                                                           |                      | 140                  |                      | $^{\circ}\text{C}$ |

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**Note1:** BIAS supply is required when the  $V_{IN}$  supply is below 1.4V. Conversely, no BIAS supply is needed when the  $V_{IN}$  supply is higher than or equal to 1.4 V.

**Note2:**  $V_{OUT (TARGET)}$  is the calculated  $V_{OUT}$  target value from the output voltage setting pins: 50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V in a fixed configuration. In an adjustable configuration,  $V_{OUT (TARGET)}$  is the expected  $V_{OUT}$  value set by the external feedback resistors.

**Note3:** This 50 $\Omega$  load is disconnected when the test conditions specify an  $I_{OUT}$  value.

**Note4:** When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.

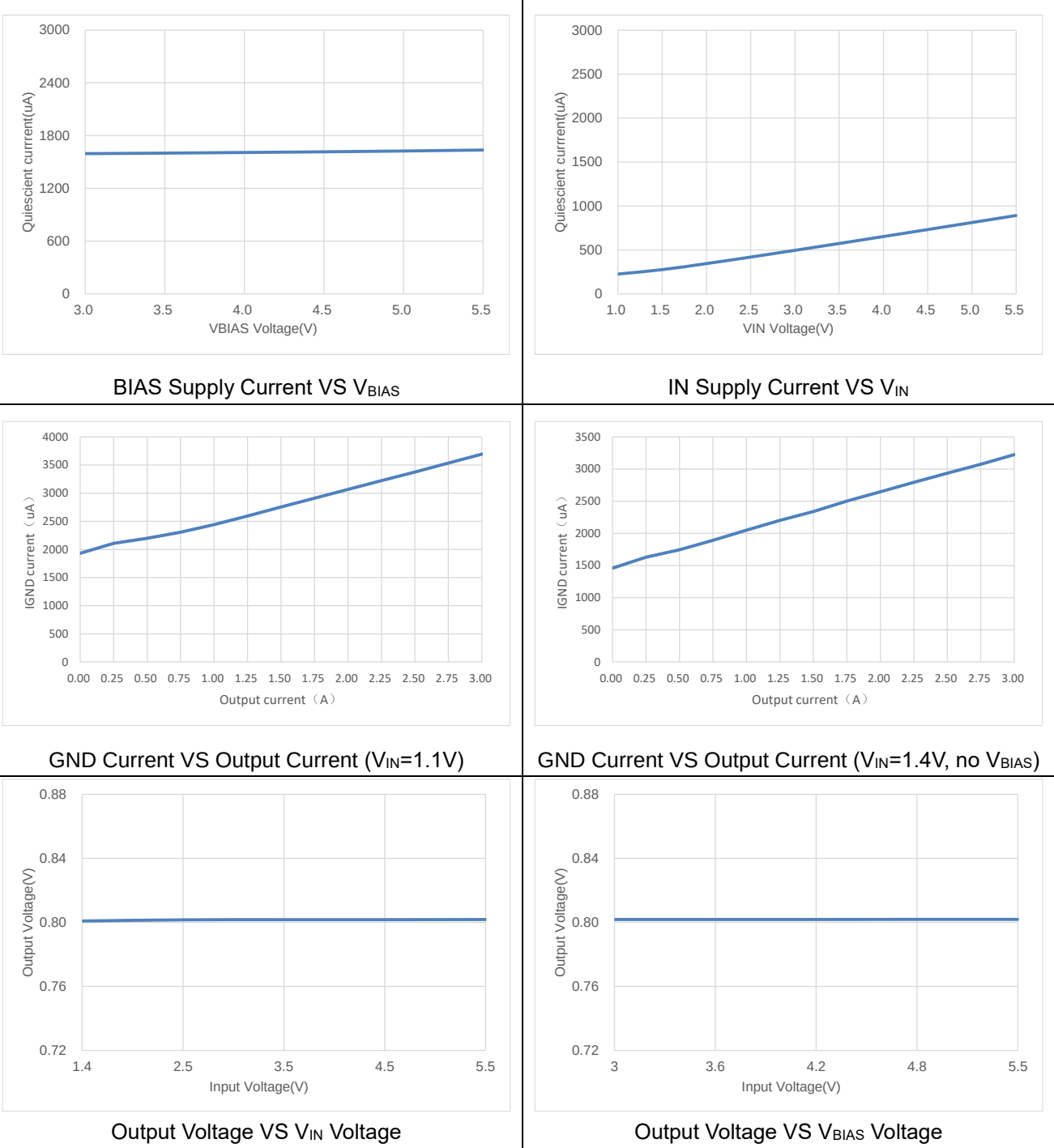
**Note5:** The device is not tested under conditions where  $V_{IN} > V_{OUT} + 2.5V$  and  $I_{OUT} = 3A$ , because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

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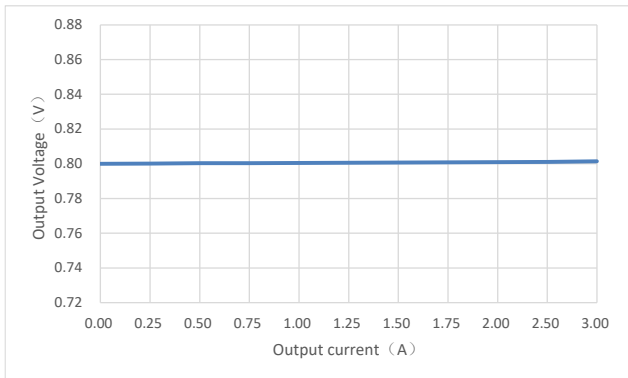
## Typical Characteristics

### (1) VOLTAGE VERSION 0.8 V

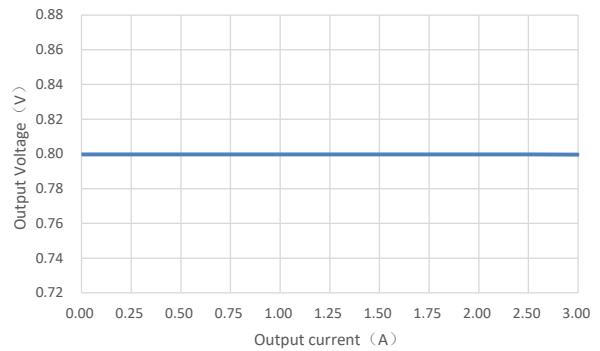
( $V_{IN}=1.1V$ ,  $V_{BIAS}=3.0V$ ,  $I_{OUT}=1mA$ ,  $C_{IN}=C_{BIAS}=10\mu F$ ,  $C_{OUT}=22\mu F$ , unless otherwise noted. Typical values are at  $T_A=25^{\circ}C$ .)



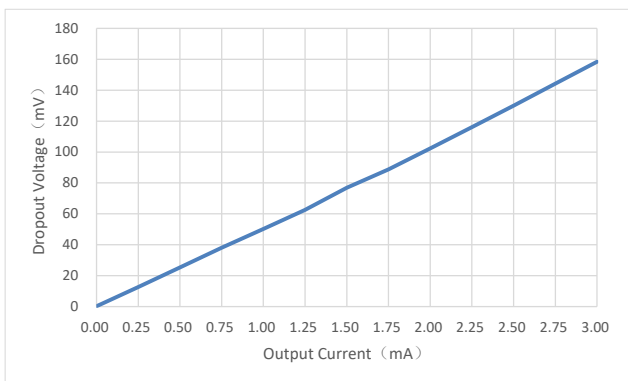
# ET5C001YB



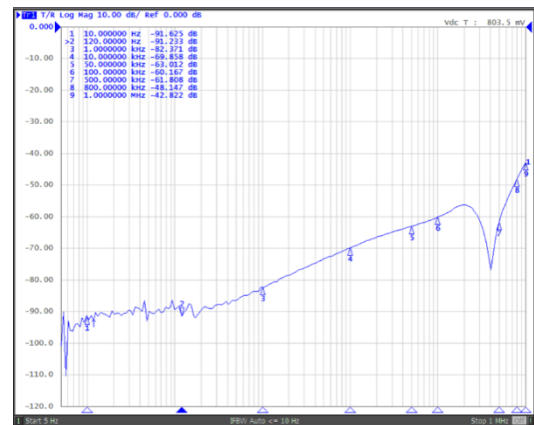
Output Voltage VS Output Current ( $V_{IN}=1.1V$ )



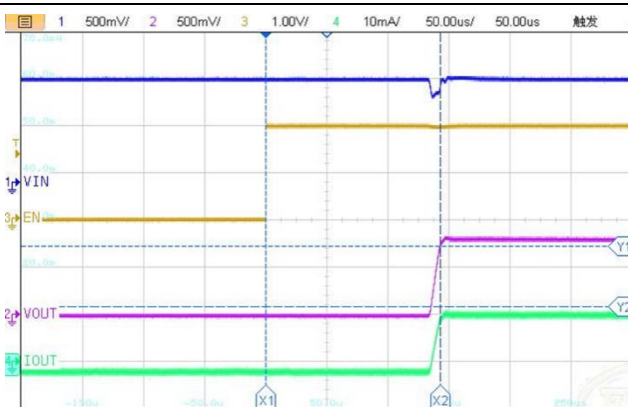
Output Voltage VS Output Current ( $V_{IN}=1.4V$ , no  $V_{BIAS}$ )



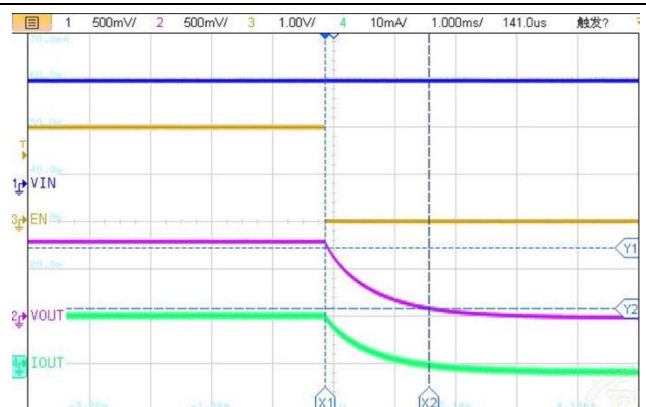
Drop Voltage VS Output Current



PSRR @30mA



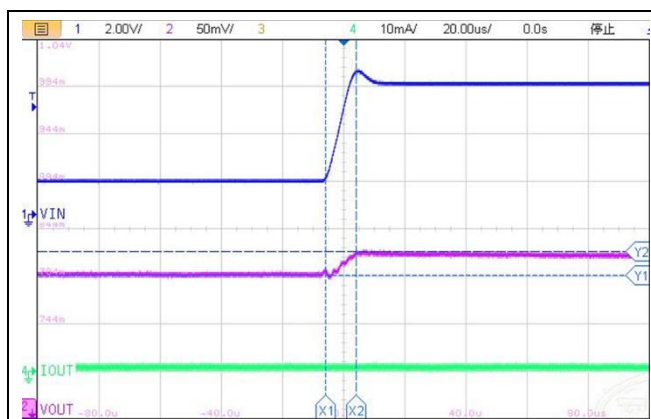
Turn On Speed VS EN Voltage ( $I_{OUT}=10mA$ )



Turn Off Speed VS EN Voltage ( $I_{OUT}=10mA$ )

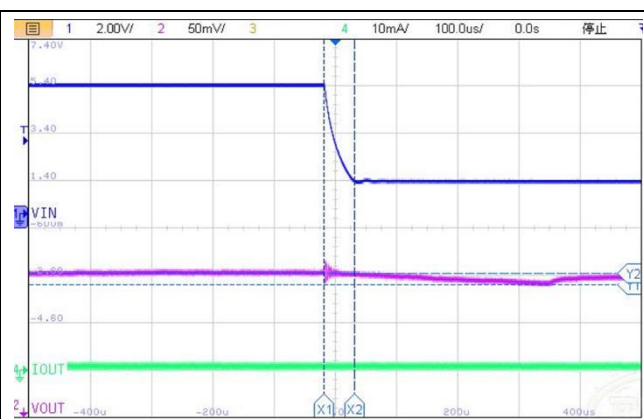


# ET5C001YB



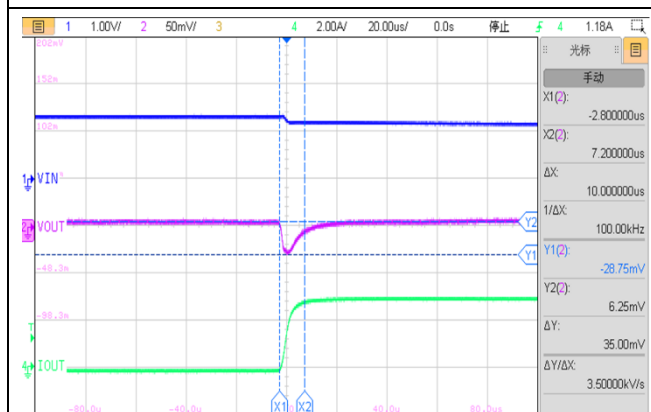
Line Transient Response

$V_{IN}=1.4V\sim 5.5V$ ,  $V_{OUT}=0.8V$ ,  $I_{OUT}=1mA$



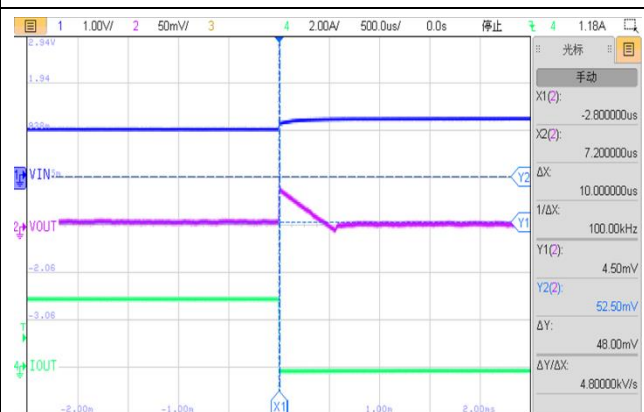
Line Transient Response

$V_{IN}=5.5V\sim 1.4V$ ,  $V_{OUT}=0.8V$ ,  $I_{OUT}=1mA$



Load Transient Response

$V_{IN}=1.1V$ ,  $V_{BIAS}=3V$ ,  $V_{OUT}=0.8V$ ,  $I_{OUT}=1mA\sim 3000mA$

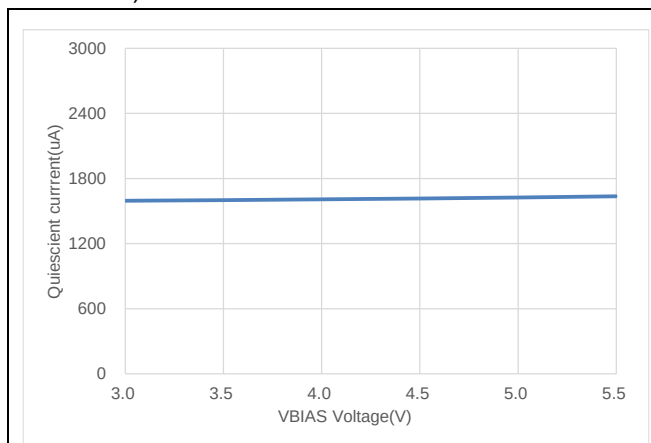


Load Transient Response

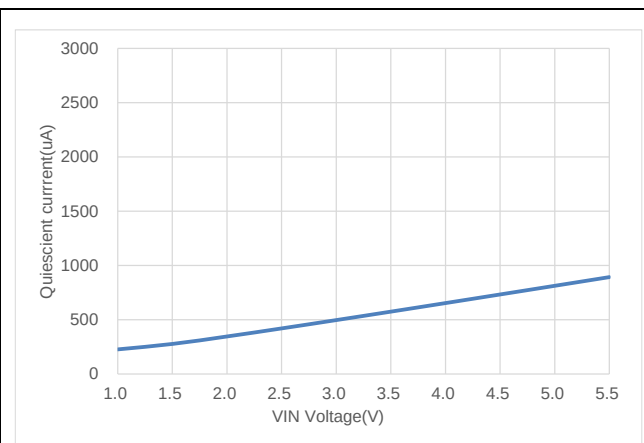
$V_{IN}=1.1V$ ,  $V_{BIAS}=3V$ ,  $V_{OUT}=0.8V$ ,  $I_{OUT}=3000mA\sim 1mA$

## (2) VOLTAGE VERSION 3.95 V

( $V_{IN}=4.25V$ , no  $V_{BIAS}$ ,  $I_{OUT}=1mA$ ,  $C_{IN}=C_{BIAS}=10\mu F$ ,  $C_{OUT}=22\mu F$ , unless otherwise noted. Typical values are at  $T_A=25^\circ C$ .)

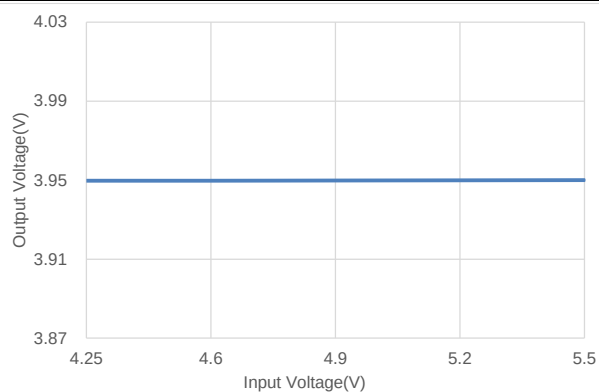


BIAS Supply Current VS  $V_{BIAS}$

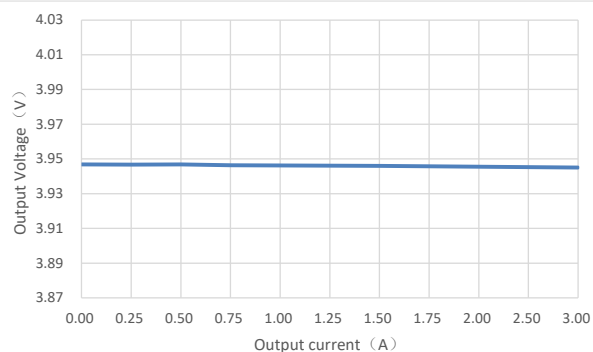


IN Supply Current VS  $V_{IN}$

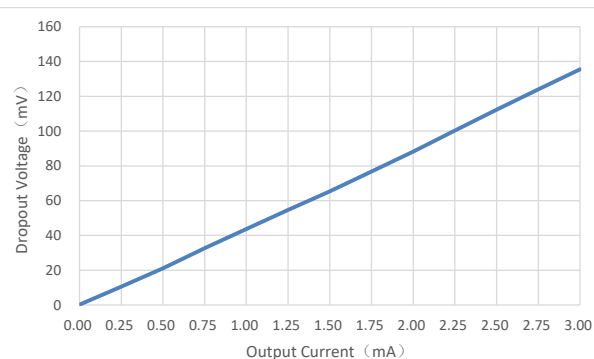
# ET5C001YB



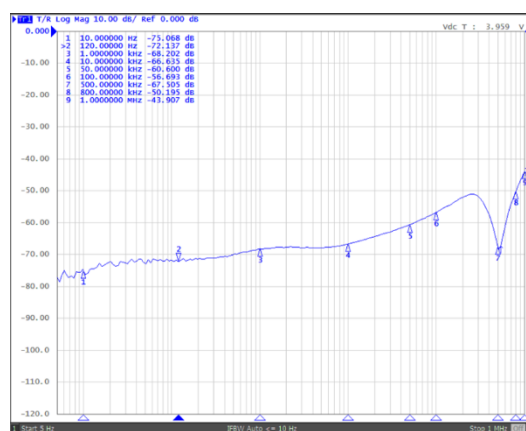
Output Voltage VS  $V_{IN}$  Voltage



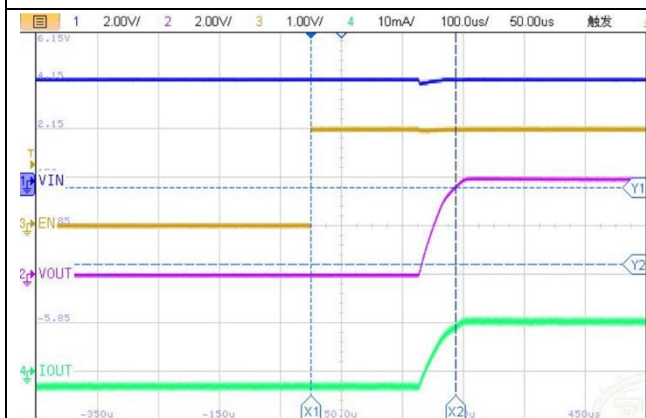
Output Voltage VS Output Current



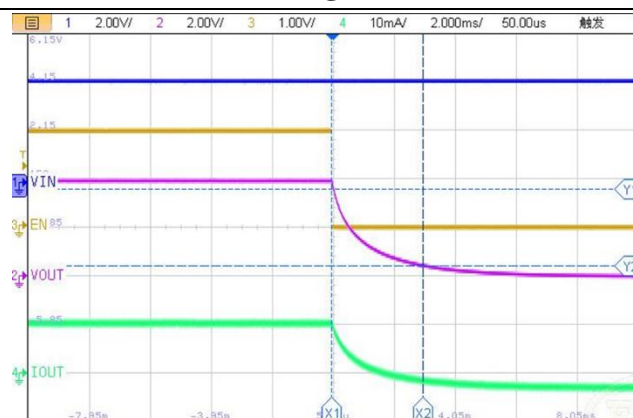
Drop Voltage VS Output Current



PSRR @ 30mA

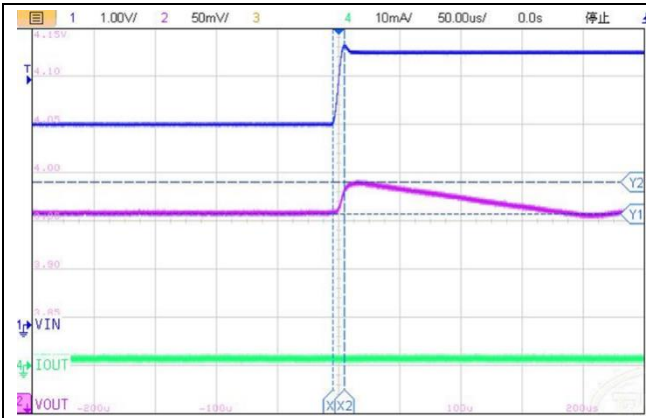


Turn On Speed VS EN Voltage ( $I_{OUT}=10mA$ )

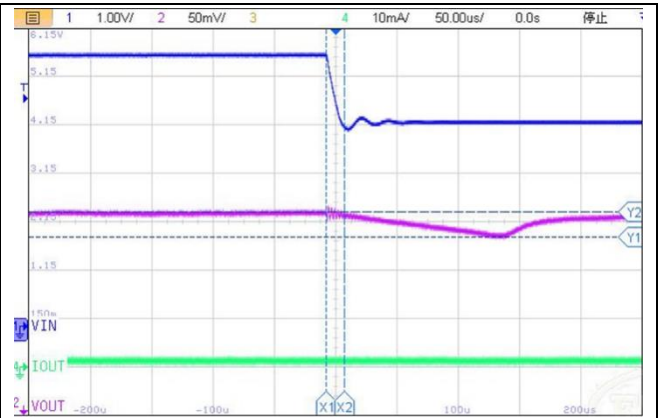


Turn Off Speed VS EN Voltage ( $I_{OUT}=10mA$ )

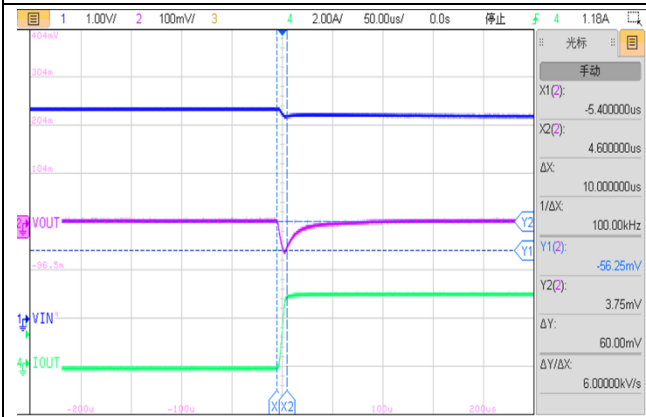
# ET5C001YB



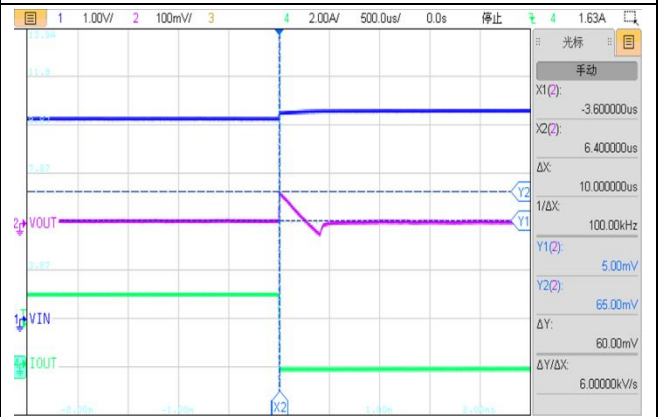
Line Transient Response  
 $V_{IN}=4.25V\sim 5.5V$ ,  $V_{OUT}=3.95V$ ,  $I_{OUT}=1mA$



Line Transient Response  
 $V_{IN}=5.5V\sim 4.25V$ ,  $V_{OUT}=3.95V$ ,  $I_{OUT}=1mA$



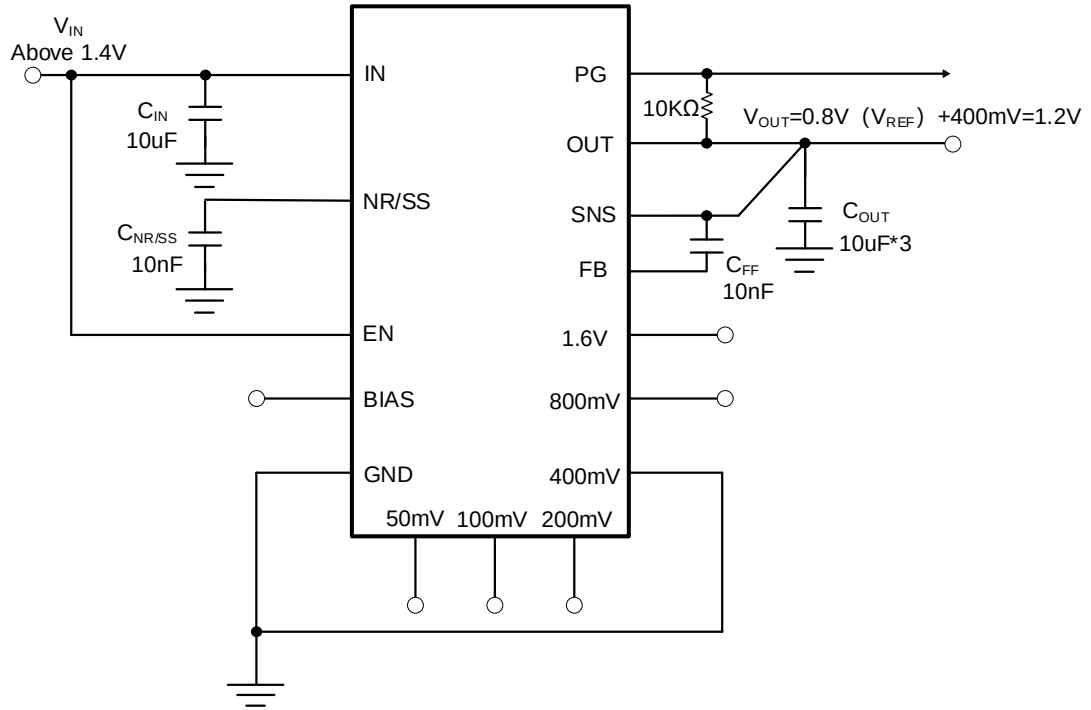
Load Transient Response  
 $V_{IN}=4.25V$ ,  $V_{OUT}=3.95V$ ,  $I_{OUT}=1mA\sim 3000mA$



Load Transient Response  
 $V_{IN}=4.25V$ ,  $V_{OUT}=3.95V$ ,  $I_{OUT}=3000mA\sim 1mA$

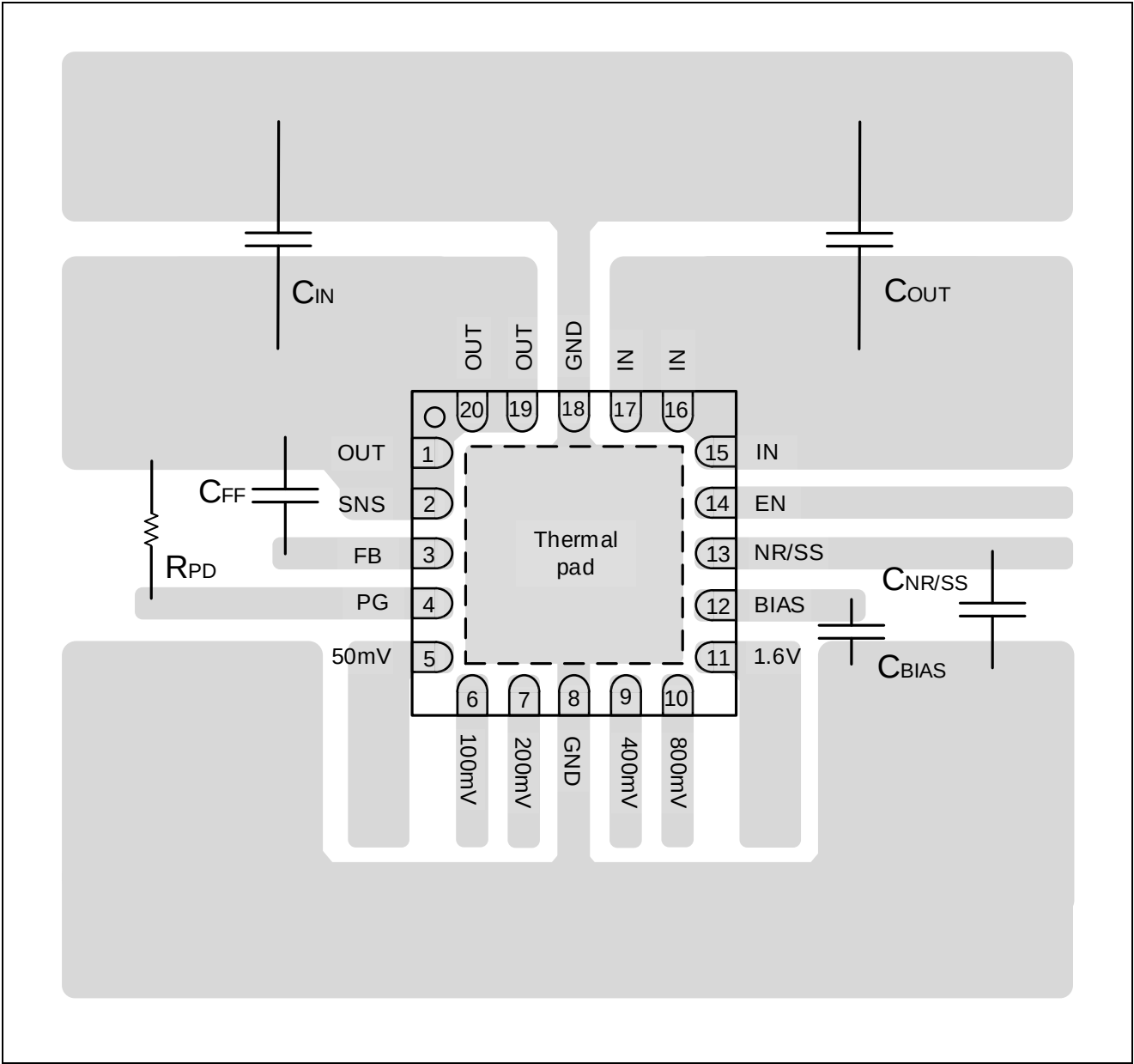
# ET5C001YB

## Application Circuits



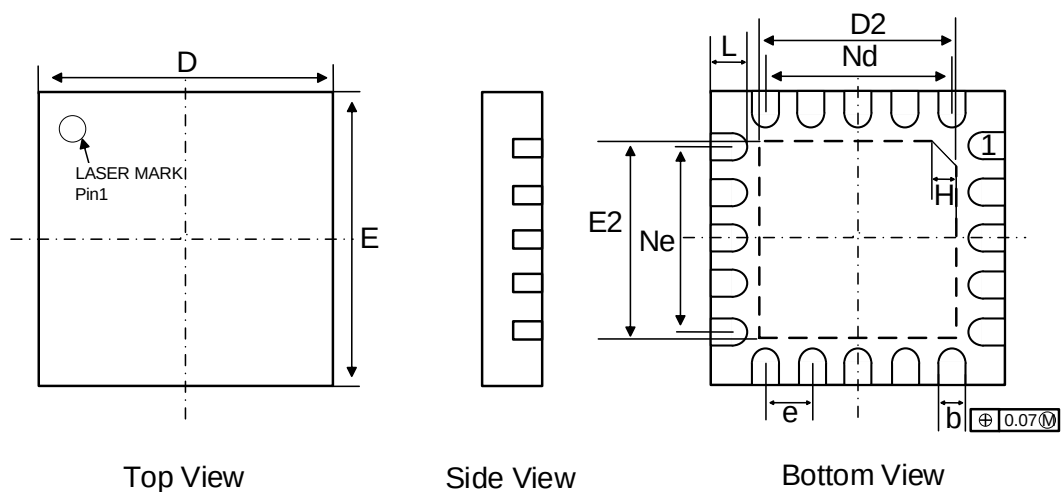
# ET5C001YB

## PCB Layout Guide



# ET5C001YB

## Package Dimension



Side View

| QFN20-5mm*5mm |          |      |      |
|---------------|----------|------|------|
| Symbol        | Unit: mm |      |      |
|               | Min      | Nom  | Max  |
| A             | 0.70     | 0.75 | 0.80 |
| A1            | -        | 0.02 | 0.05 |
| A3            | 0.18     | 0.20 | 0.25 |
| b             | 0.25     | 0.30 | 0.35 |
| D             | 4.90     | 5.00 | 5.10 |
| E             | 4.90     | 5.00 | 5.10 |
| D2            | 3.05     | 3.15 | 3.25 |
| E2            | 3.05     | 3.15 | 3.25 |
| Nd            | 2.60BSC  |      |      |
| Ne            | 2.60BSC  |      |      |
| e             | 0.65BSC  |      |      |
| L             | 0.45     | 0.55 | 0.65 |
| H             | 0.30     | 0.35 | 0.40 |

## ET5C001YB

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**Revision History and Checking Table**

| Version | Date       | Revision Item                        | Modifier     | Function & Spec Checking | Package & Tape Checking |
|---------|------------|--------------------------------------|--------------|--------------------------|-------------------------|
| 1.0     | 2023-02-08 | Original Version                     | Li Huan      | Liu Yi Guo               | Li Huan                 |
| 1.1     | 2023-04-01 | Update Typeset                       | Yang Xiao Xu | Liu Yi Guo               | Yang Xiao Xu            |
| 1.2     | 2024-11-11 | Update characteristic curve          | Yang Xiao Xu | Liu Yi Guo               | Yang Xiao Xu            |
| 1.3     | 2026-05-12 | Update PSRR Test Condition and Value | Yang Xiao Xu | Liu Yi Guo               | Li Huan                 |