

Hex Non-Inverting Buffer

General Description

The ET74LVC34A is a high-performance hex non-inverting buffer gate operating from a 1.65V to 5.5V supply. This device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive.

Features

- Designed for 1.65V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- $\pm 32\text{mA}$ Balanced Output Sink and Source Capability
- ESD Protection Complies with JEDEC22 Standard
 - HBM: $\pm 4000\text{V}$ Pass (JEDEC JS-001)
 - CDM: $\pm 2000\text{V}$ Pass (JEDEC JS-002)
- Latch-up Performance Exceeds $\pm 100\text{mA}$ Per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74LVC34AM14	SOP14 (3.9mm $\times$ 8.65mm)	Tape and Reel, 4K/Reel	3
ET74LVC34AV	TSSOP14 (4.4mm $\times$ 5.0mm)	Tape and Reel, 4K/Reel	3

Pin Configuration

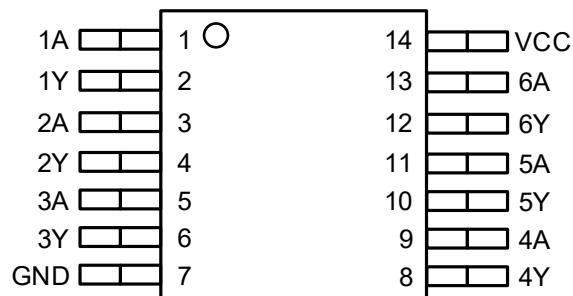


Figure1. Pin Configuration

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Pin Function

SOP14/TSSOP14

Pin No.	Pin Name	Function
1	1A	Channel 1, Input A
2	1Y	Channel 1, Output Y
3	2A	Channel 2, Input A
4	2Y	Channel 2, Output Y
5	3A	Channel 3, Input A
6	3Y	Channel 3, Output Y
7	GND	Ground
8	4Y	Channel 4, Output Y
9	4A	Channel 4, Input A
10	5Y	Channel 5, Output Y
11	5A	Channel 5, Input A
12	6Y	Channel 6, Output Y
13	6A	Channel 6, Input A
14	VCC	Supply Voltage

Block Diagram

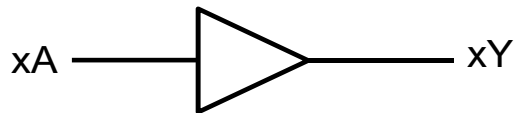


Figure2. Logic Symbol

Functional Table

Input	Output
xA	xY
L	L
H	H

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Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 6.5	V
V _I	DC Input Voltage ⁽¹⁾		-0.5 ≤ V _I ≤ 6.5	V
I _{IK}	DC Input Diode Current, V _I < GND		-50	mA
I _{OK}	DC Output Diode Current, V _O < GND, V _O > V _{CC}		-50	mA
I _O	DC Output Sink Current		±50	mA
I _{CC}	DC Supply Current Per Supply Pin		+100	mA
I _{GND}	DC Supply Current Per GND Pin		-100	mA
T _{STG}	Storage Temperature Range		-65 to 150	°C
V _{ESD}	ESD Classification	Human Body Model ⁽²⁾	±4000	V
		Charged Device Model ⁽³⁾	±2000	
I _{LU}	Max Latch Up Current Above V _{CC} and GND at 125°C ⁽⁴⁾		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch Up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage Operating	1.65	5.5	V
V _I	DC Input Voltage	0	V _{CC}	V
V _O	DC Output Voltage (High or Low State)	0	V _{CC}	V
T _A	Operating Temperature Range	-40	125	°C

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Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65~1.95	0.75V _{CC}			0.75V _{CC}		V
			2.3~5.5	0.7V _{CC}			0.7V _{CC}		
V _{IL}	Low-Level Input Voltage		1.65~1.95			0.25V _{CC}		0.25V _{CC}	V
			2.3~5.5			0.3V _{CC}		0.3V _{CC}	
V _{OH}	High-Level Output Voltage	I _{OH} = -100uA	1.65~5.5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V
		I _{OH} = -4mA	1.65	1.29	1.4		1.29		
		I _{OH} = -8mA	2.3	1.9	2.1		1.9		
		I _{OH} = -12mA	2.7	2.2	2.4		2.2		
		I _{OH} = -16mA	3.0	2.4	2.7		2.4		
		I _{OH} = -24mA	3.0	2.3	2.5		2.3		
		I _{OH} = -32mA	4.5	3.8	4.0		3.8		
V _{OL}	Low-Level Output Voltage	I _{OL} = 100uA	1.65~5.5		0.0	0.1		0.1	V
		I _{OL} = 4mA	1.65		0.08	0.24		0.24	
		I _{OL} = 8mA	2.3		0.20	0.3		0.3	
		I _{OL} = 12mA	2.7		0.22	0.4		0.4	
		I _{OL} = 16mA	3.0		0.28	0.4		0.4	
		I _{OL} = 24mA	3.0		0.38	0.55		0.55	
		I _{OL} = 32mA	4.5		0.42	0.55		0.55	
I _I	Input Leakage Current	V _I = 5.5V or GND	0~5.5			±0.1		±1.0	uA
I _{OFF}	Power Off Leakage Current	V _I = 5.5V or V _O = 5.5V	0			1		10	uA
I _{CC}	Quiescent Supply Current	V _I = 5.5V or GND	1.65~5.5			1		10	uA

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AC Electrical Characteristics

$t_r = t_f = 3\text{ns}$

Symbol	Parameter	Condition	$V_{CC}(\text{V})$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PD}	Propagation Delay (Figure3 and4)	$R_L = 1\text{k}\Omega$; $C_L = 30\text{pF}$	1.65~1.95		11.4	14.8		16.8	ns
		$R_L = 500\Omega$; $C_L = 30\text{pF}$	2.3~2.7		6.2	8		10	
		$R_L = 500\Omega$; $C_L = 50\text{pF}$	2.7		5.8	7.5		9.5	
		$R_L = 500\Omega$; $C_L = 50\text{pF}$	3.0~3.6		5.4	7		9	
		$R_L = 500\Omega$; $C_L = 50\text{pF}$	4.5~5.5		3.9	5.1		7.1	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5\text{V}$, $V_I = 0\text{V}$ or V_{CC}	2	pF
C_{PD}	Power Dissipation Capacitance ⁽⁵⁾	10MHz, $V_{CC} = 3.3\text{V}$, $V_I = 0\text{V}$ or V_{CC}	21	pF
		10MHz, $V_{CC} = 5.5\text{V}$, $V_I = 0\text{V}$ or V_{CC}	24	

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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AC Test Circuit

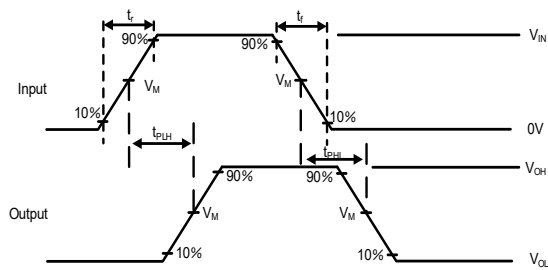


Figure3. Switching Waveform

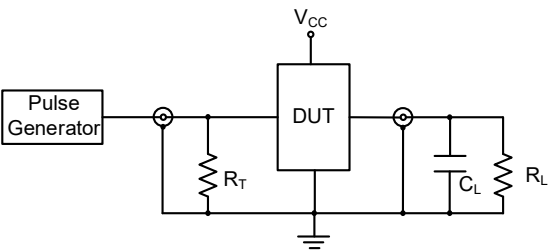


Figure4. Test Circuit

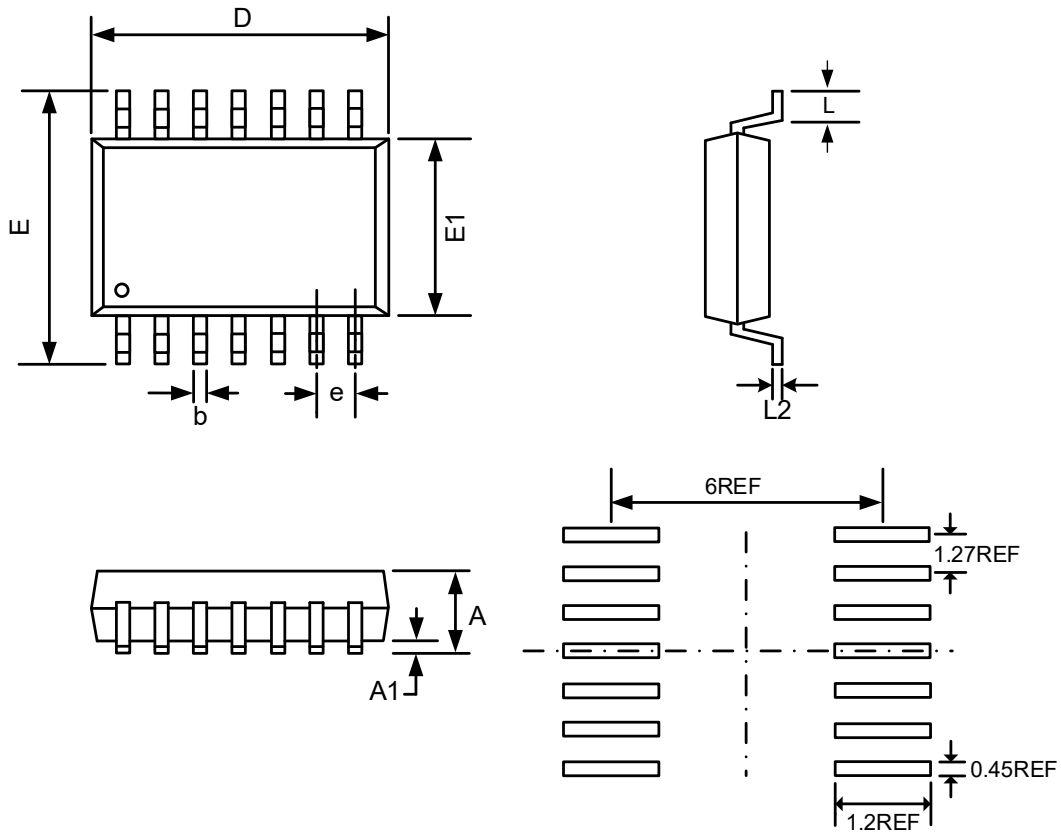
Table1. Measurement Points and Test Data

V_{CC}	V_I	t_r/t_f	V_M	C_L	R_L
$1.8V \pm 0.15V$	V_{CC}	$\leq 3ns$	$V_{CC} / 2$	30pF	1k Ω
$2.5V \pm 0.2V$	V_{CC}	$\leq 3ns$	$V_{CC} / 2$	30pF	500 Ω
$3.3V \pm 0.3V$	2.7V	$\leq 3ns$	1.5V	50pF	500 Ω
$5V \pm 0.5V$	V_{CC}	$\leq 3ns$	$V_{CC} / 2$	50pF	500 Ω

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Package Dimension

SOP14 (3.9mm × 8.65mm)



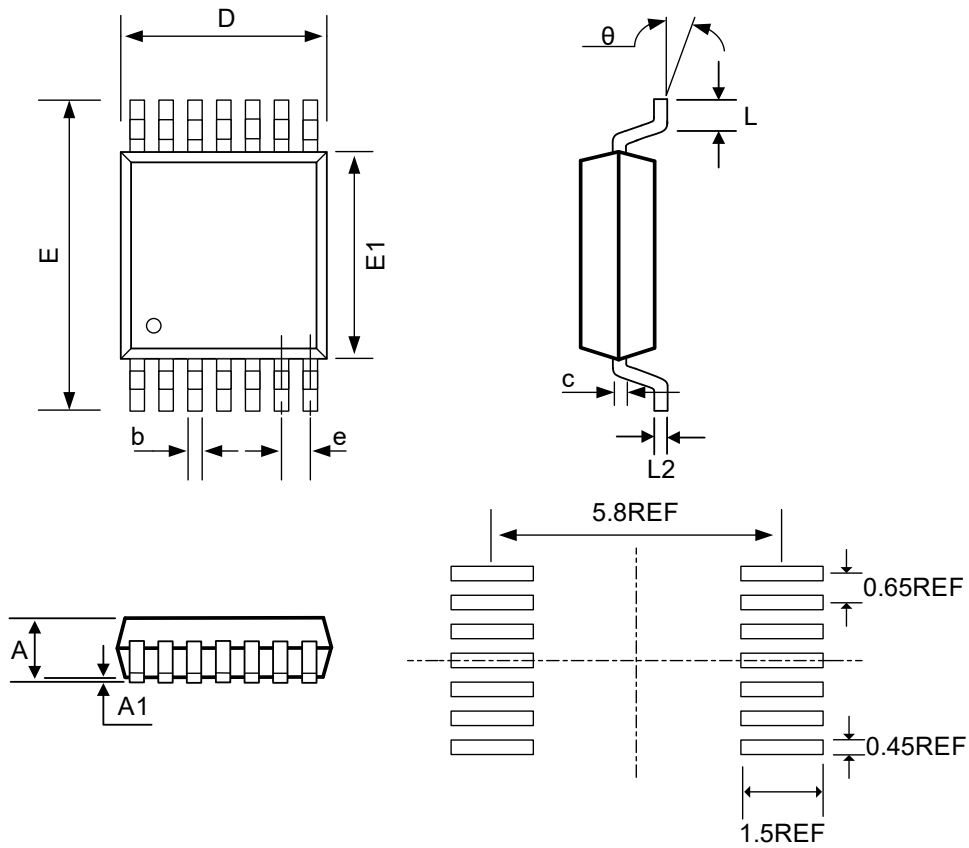
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	MAX
A	--	1.75
A1	0.10	0.25
b	0.36	0.51
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.22	1.32
L	0.45	0.75
L2	0.25 BSC	

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TSSOP14 (4.4mm × 5.0mm)



COMMON DIMENSIONS

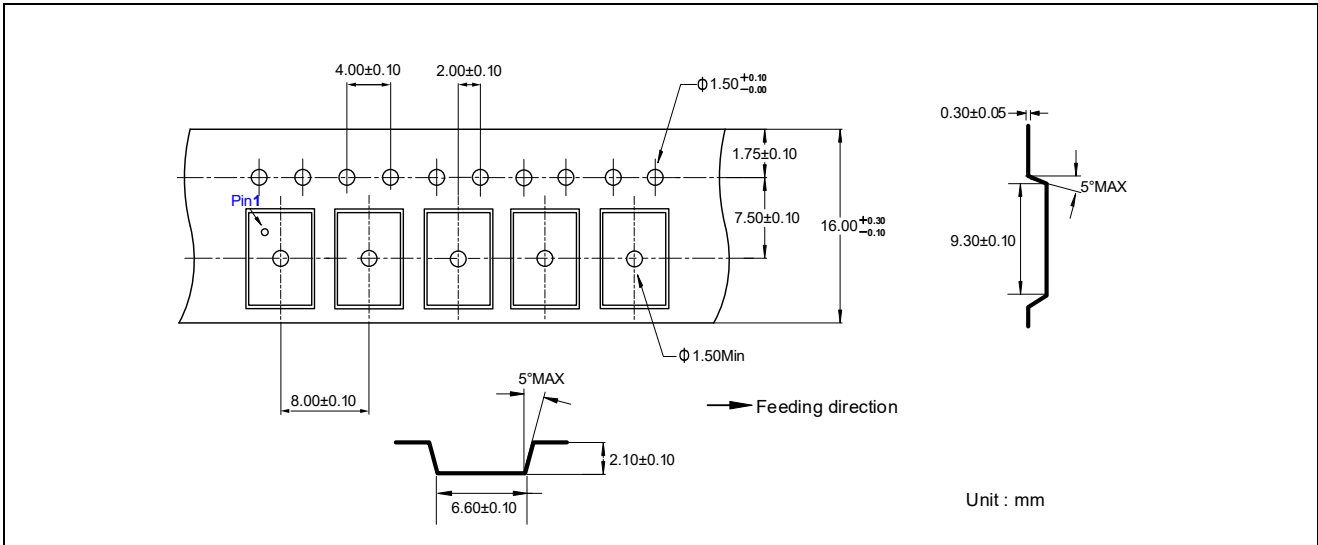
(Unit: mm)

SYMBOL	MIN	MAX
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 REF	
D	4.86	5.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L2	0.25 REF	
θ	0°	8°

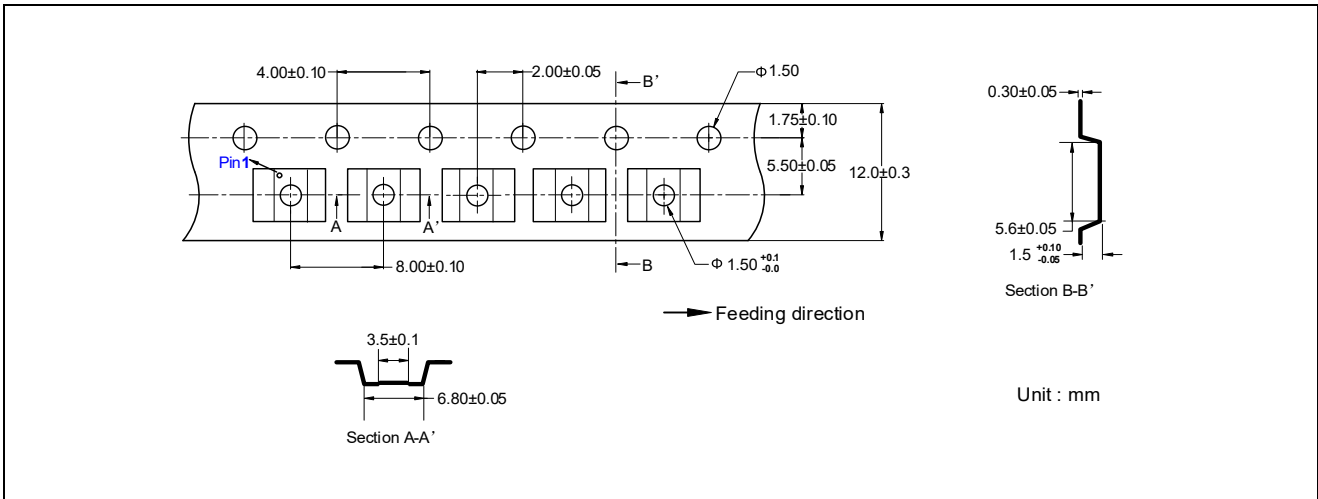
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Tape Information

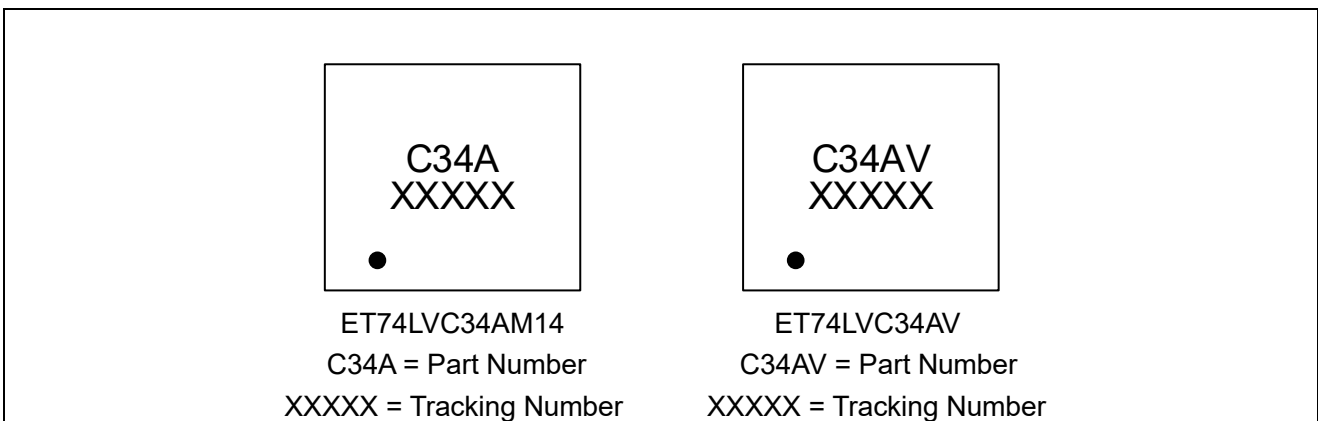
SOP14 (3.9mm × 8.65mm)



TSSOP14 (4.4mm × 5.0mm)



Marking Information



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Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-03-24	Official Version	Xu tao	Yang xiaoxu	Liu jiaying