Hex Schmitt-Triggered Buffer

General Description

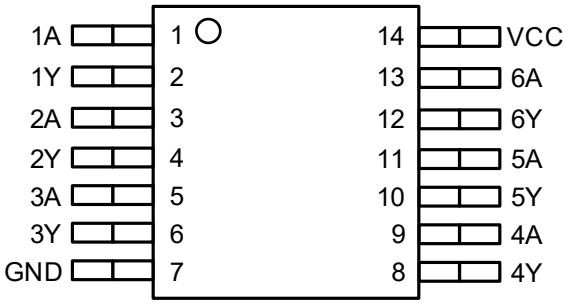
The ET74LVC17A is a high-performance, low-power, low-voltage, Si-gate CMOS device and provides six non-inverting buffers with Schmitt trigger action. It is capable for transforming slowly changing input signals into sharply defined, jitter-free output signals.

Features

- Designed for 1.65V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- ±32mA Balanced Output Sink and Source Capability
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±4000V Pass (JEDEC JS-001)
  -- CDM: ±2000V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA Per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74LVC17AM14	SOP14 (3.9mm × 8.65mm)	Tape and Reel, 4K/Reel	3
ET74LVC17AV	TSSOP14 (4.4mm × 5.0mm)	Tape and Reel, 4K/Reel	3

Pin Configuration



SOP14/TSSOP14

Figure1. Pin Configuration

Pin Function

SOP14/TSSOP14

Pin No.	Pin Name	Function
1	1A	Channel 1, Input A
2	1Y	Channel 1, Output Y
3	2A	Channel 2, Input A
4	2Y	Channel 2, Output Y
5	3A	Channel 3, Input A
6	3Y	Channel 3, Output Y
7	GND	Ground
8	4Y	Channel 4, Output Y
9	4A	Channel 4, Input A
10	5Y	Channel 5, Output Y
11	5A	Channel 5, Input A
12	6Y	Channel 6, Output Y
13	6A	Channel 6, Input A
14	VCC	Supply Voltage

Block Diagram

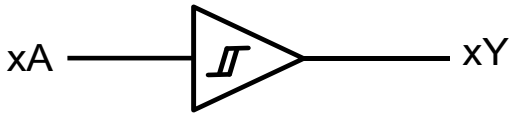


Figure2. Logic Symbol

Functional Table

Input	Output
xA	**xY**
L	L
H	H

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 6.5	V
V_I	DC Input Voltage (1)		-0.5 ≤ V_I ≤ 6.5	V
I_{IK}	DC Input Diode Current, V_I < GND		-50	mA
I_{OK}	DC Output Diode Current, V_O < GND, V_O > V_{CC}		-50	mA
I_O	DC Output Sink Current		±50	mA
I_{CC}	DC Supply Current Per Supply Pin		+100	mA
I_{GND}	DC Supply Current Per GND Pin		-100	mA
T_{STG}	Storage Temperature Range		-65 to 150	°C
V_{ESD}	ESD Classification	Human Body Model (2)	±4000	V
		Charged Device Model (3)	±2000	
I_{LU}	Max Latch Up Current Above V_{CC} and GND at 125°C (4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch Up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage Operating	1.65	5.5	V
V_I	DC Input Voltage	0	V_{CC}	V
V_O	DC Output Voltage (High or Low State)	0	V_{CC}	V
T_A	Operating Temperature Range	-40	125	°C

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		1.65	1.40			1.40		V
			2.3	1.70			1.70		
			3	2.20			2.20		
			4.5	3.10			3.10		
			5.5	3.70			3.70		
V_{IL}	Low-Level Input Voltage		1.65			0.30		0.30	V
			2.3			0.40		0.40	
			3			0.60		0.60	
			4.5			1.10		1.10	
			5.5			1.40		1.40	
V_{OH}	High-Level Output Voltage	I_{OH} = -100μA	1.65~5.5	V_{CC} - 0.1			V_{CC} - 0.1		V
		I_{OH} = -4mA	1.65	1.20			1.44		
		I_{OH} = -8mA	2.3	1.90			2.05		
		I_{OH} = -16mA	3	2.40			2.65		
		I_{OH} = -24mA		2.30			2.40		
		I_{OH} = -32mA	4.5	3.80			4.00		
V_{OL}	Low-Level Output Voltage	I_{OL} = 100μA	1.65~5.5			0.10		0.10	V
		I_{OL} = 4mA	1.65			0.45		0.45	
		I_{OL} = 8mA	2.3			0.30		0.30	
		I_{OL} = 16mA	3			0.40		0.40	
		I_{OL} = 24mA				0.55		0.55	
		I_{OL} = 32mA	4.5			0.55		0.55	
I_I	Input Leakage Current	V_I = V_{CC} or GND I_O = 0mA	1.65~5.5			±5		±5	μA
I_{CC}	Supply Current	V_I = V_{CC} or GND, I_O = 0mA	5.5			10		10	μA
ΔI_{CC}	Additional Quiescent Supply Current	One Input at V_{CC} - 0.6V, Other Inputs at V_{CC} or GND	3~5.5			500		500	μA

AC Electrical Characteristics

Over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Condition	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay nA to nY See Table1	V_{CC} = 1.8V ± 0.15V	3.9		9.3	1	11	ns
		V_{CC} = 2.5V ± 0.2V	1.9		5.7	1	7	ns
		V_{CC} = 3.3V ± 0.3V	2.2		5.4	1	5.5	ns
		V_{CC} = 5V ± 0.5V	1.5		4.3	1	4.3	ns

Capacitance Characteristics

Over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Condition	Typ	Unit
C_{PD}	Power Dissipation Capacitance per Buffer and Driver (5)	10MHz, V_{CC} = 1.8V	17	pF
		10MHz, V_{CC} = 2.5V	18	pF
		10MHz, V_{CC} = 3.3V	19	pF
		10MHz, V_{CC} = 5.0V	21	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

AC Test Circuit

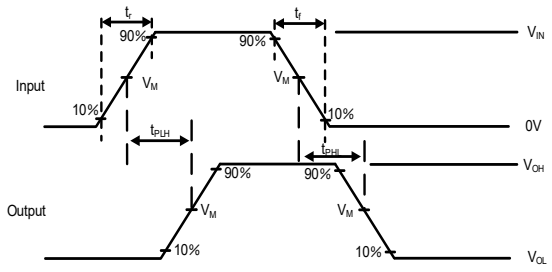


Figure3. Switching Waveform

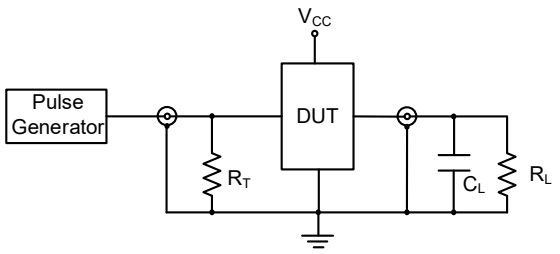


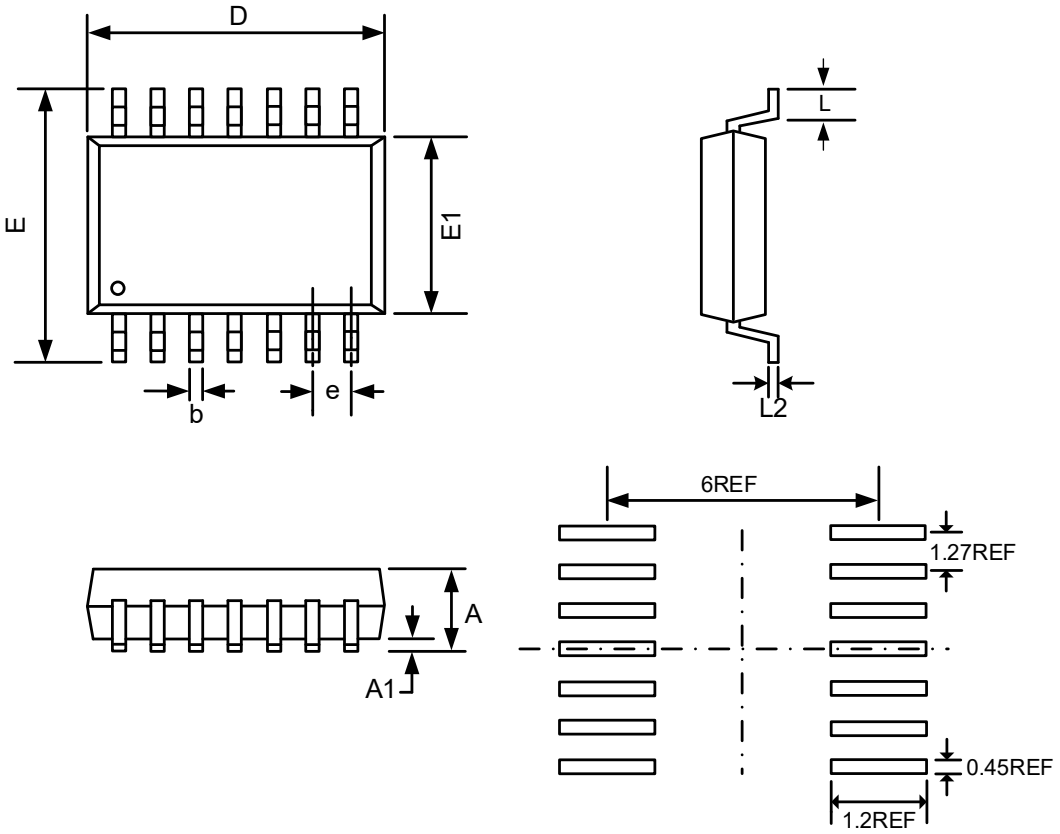
Figure4. Test Circuit

Table1. Measurement Points and Test Data

V_{CC}	V_I	t_r/t_f	V_M	C_L	R_L
1.8V ± 0.15V	V_{CC}	≤ 3ns	V_{CC} / 2	30pF	1kΩ
2.5V ± 0.2V	V_{CC}	≤ 3ns	V_{CC} / 2	30pF	500Ω
3.3V ± 0.3V	2.7V	≤ 3ns	1.5V	50pF	500Ω
5V ± 0.5V	V_{CC}	≤ 3ns	V_{CC} / 2	50pF	500Ω

Package Dimension

SOP14 (3.9mm × 8.65mm)

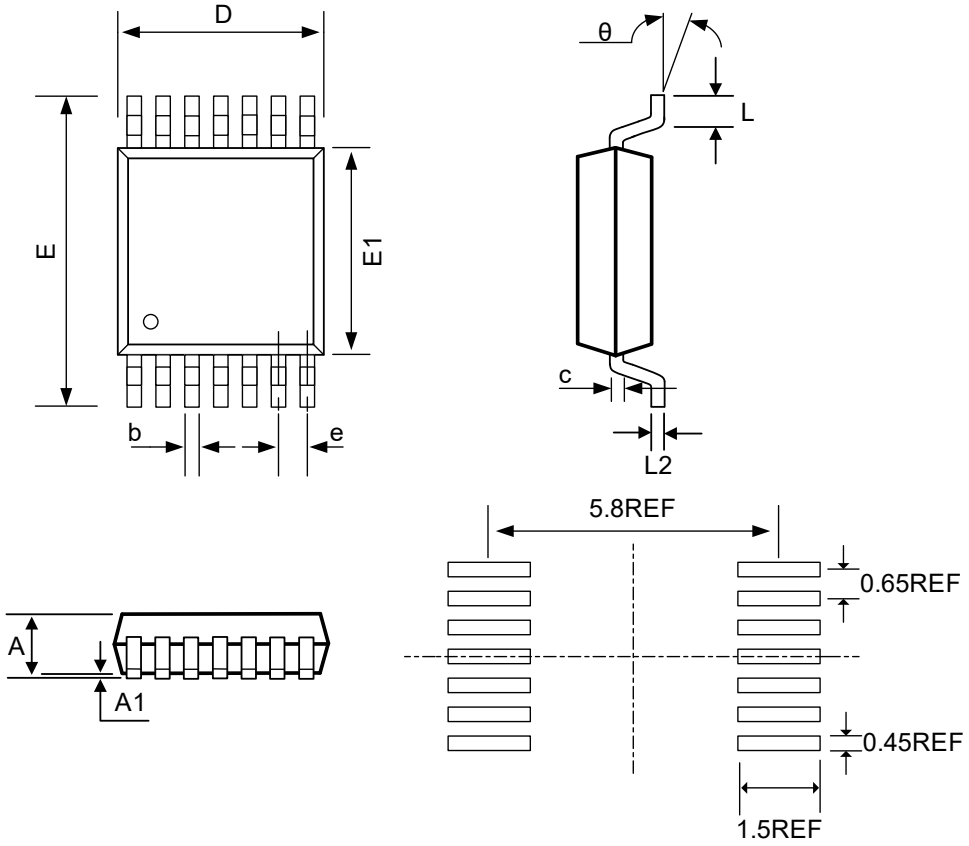


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	MAX
A	--	1.75
A1	0.10	0.25
b	0.36	0.51
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.22	1.32
L	0.45	0.75
L2	0.25 BSC	

TSSOP14 (4.4mm × 5.0mm)



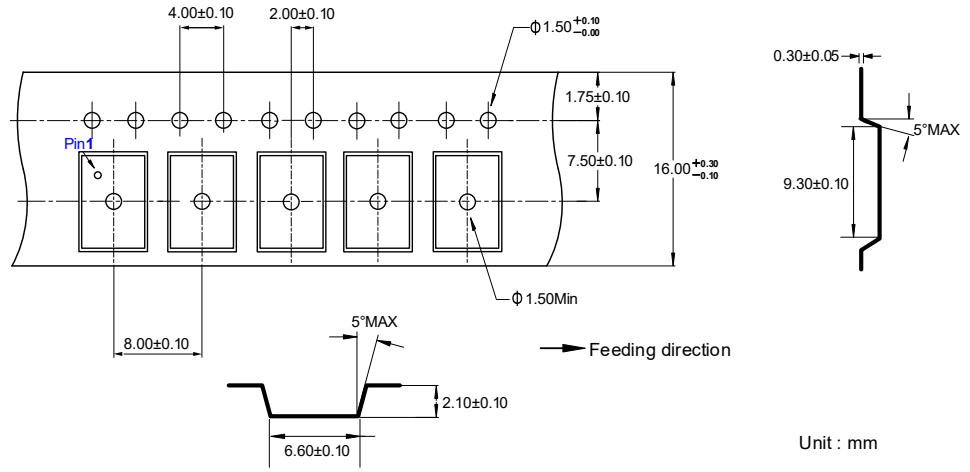
COMMON DIMENSIONS

(Unit: mm)

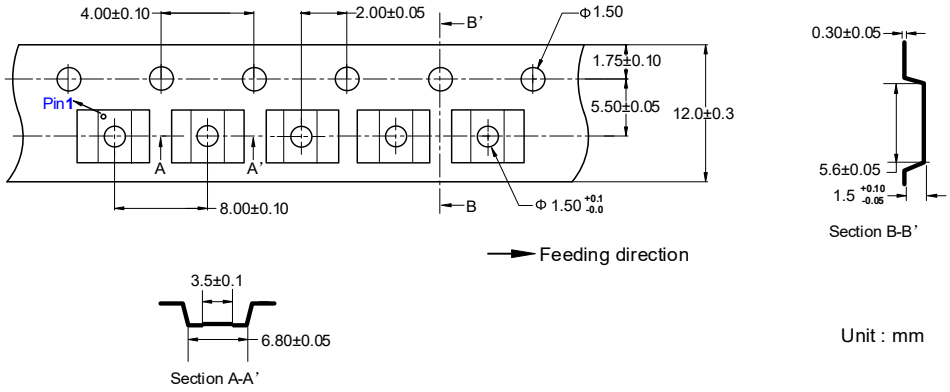
SYMBOL	MIN	MAX
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 REF	
D	4.86	5.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L2	0.25 REF	
θ	0°	8°

Tape Information

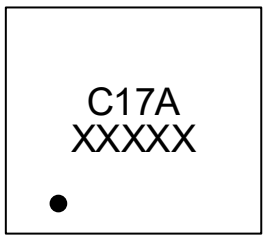
SOP14 (3.9mm × 8.65mm)



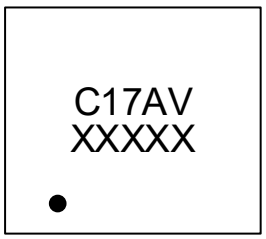
TSSOP14 (4.4mm × 5.0mm)



Marking Information



ET74LVC17AM14
C17A = Part Number
XXXXX = Tracking Number



ET74LVC17AV
C17AV = Part Number
XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2025-07-11	Preliminary Version	Zhang zixuan	Yang xiaoxu	Liu jiaying
1.0	2025-09-15	Official Version	Zhang zixuan	Yang xiaoxu	Liu jiaying
1.0.a	2026-03-24	Update Format, Add Tape and Marking	Xu tao	Yang xiaoxu	Liu jiaying