

Low-Power Configurable Multiple Function Gate

General Description

The ET74LVC1G58 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions AND, OR, NAND, NOR, XOR, inverter and buffer; using the 3-bit input. All inputs can be connected directly to V_{CC} or GND. Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in mixed 3.3V and 5V environments.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging back-flow current through the device when it is powered down.

Features

- Designed for 1.65V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- $\pm 32\text{mA}$ Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- ESD Protection Complies with JESD22 Standard
 - HBM: $\pm 2000\text{V}$ Pass (JEDEC JS-001)
 - CDM: $\pm 1500\text{V}$ Pass (JEDEC JS-002)
- Latch-up Performance Exceeds $\pm 100\text{mA}$ per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74LVC1G58	SC70-6 (1.3mm $\times$ 2.1mm)	Tape and Reel, 3K/Reel	3
ET74LVC1G58T	SOT23-6 (1.6mm $\times$ 2.9mm)	Tape and Reel, 3K/Reel	3

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Applications

- Active Noise Cancellation (ANC)
- Bar-code Scanners
- Blood Pressure Monitors
- CPAP Machines
- Cable Solutions
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- HVAC: Heating, Ventilating and Air Conditioning
- TVs: High-Definition (HDTV), LCD and Digital
- Video Communications Systems

Pin Configuration

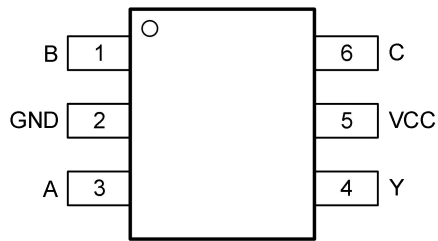


Figure1. Pin Configuration

Pin Function

SC70-6/SOT23-6

Pin No.	Pin Name	Function
1	B	Input B
2	GND	Ground
3	A	Input A
4	Y	Output Y
5	VCC	Supply Voltage
6	C	Input C

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Block Diagram

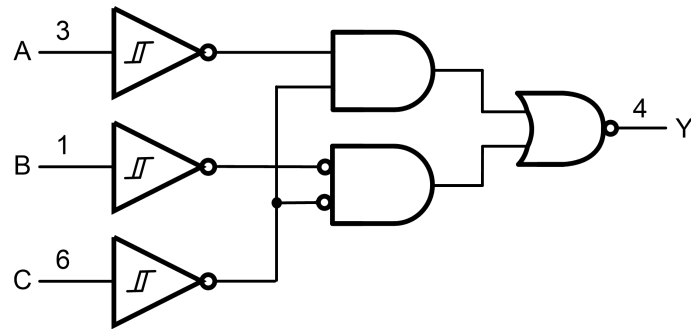


Figure2. Logic Symbol

Functional Table

Input			Output
C	B	A	Y
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

H = HIGH voltage level; L = LOW voltage level.

Function Selection Table

Logic function	Figure
2-input NAND	See Figure3
2-input NAND with both Inputs Inverted	See Figure6
2-input AND with Inverted Input	See Figure4 and Figure5
2-input NOR with Inverted Input	See Figure4 and Figure5
2-input OR	See Figure6
2-input OR with both Inputs Inverted	See Figure3
2-input XOR	See Figure7
Buffer	See Figure8
Inverter	See Figure9

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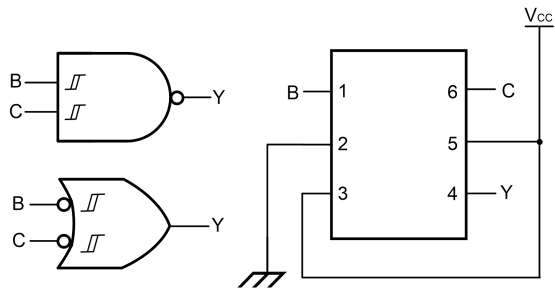


Figure3. 2-input NAND gate or
2-input OR gate with both inputs inverted

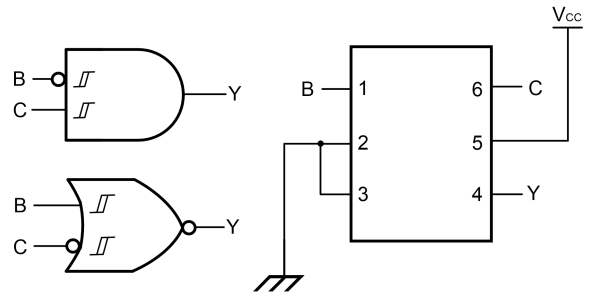


Figure4. 2-input AND gate with input B inverted or
2-input NOR gate with inverted C input

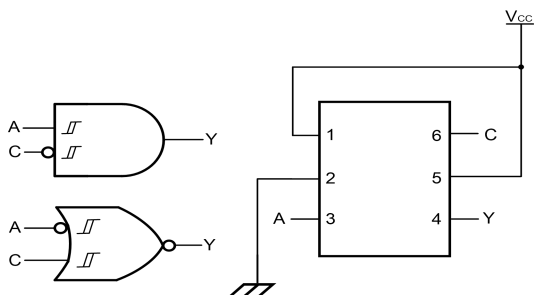


Figure5. 2-input AND gate with input C inverted or
2-input NOR gate with inverted A input

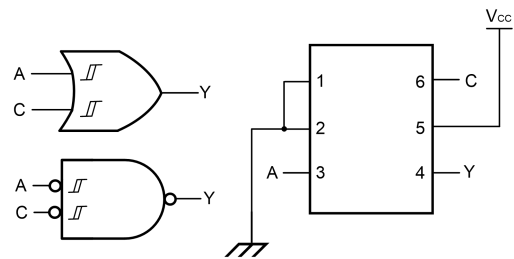


Figure6. 2-input OR gate or
2-input NAND gate with both inputs inverted

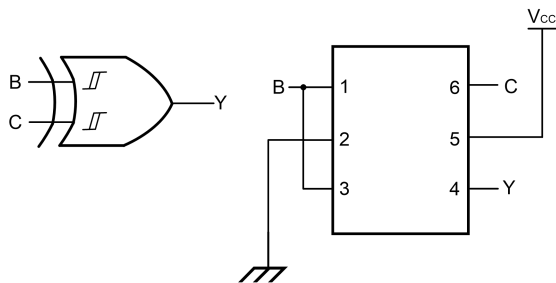


Figure7. 2-input XOR gate

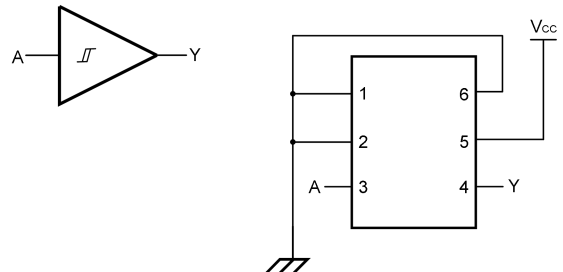


Figure8. Buffer

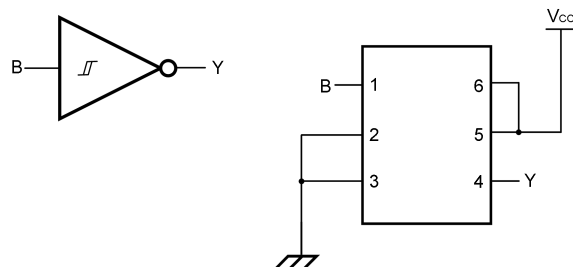


Figure9. Inverter

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Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 6.5	V
V _I	DC Input Voltage ⁽¹⁾		-0.5 ≤ V _I ≤ 6.5	V
V _O	DC Output Voltage Output in Higher or Low State		-0.5 to 6.5	V
I _{IK}	DC Input Diode Current, V _I < GND		-50	mA
I _{OK}	DC Output Diode Current, V _O < GND, V _O > V _{CC}		±50	mA
I _O	DC Output Sink Current		±50	mA
I _{CC}	DC Supply Current per Supply Pin		100	mA
I _{GND}	DC Ground Current per Supply Pin		-100	mA
T _{STG}	Storage Temperature Range		-65 to 150	°C
T _L	Lead Temperature, Soldering 10 Seconds		260	°C
T _J	Max Junction Temperature		150	°C
V _{ESD}	ESD Classification	Human Body Model ⁽²⁾	±2000	V
		Charged Device Model ⁽³⁾	±1500	
I _{LU}	Max Latch Up Current Above V _{CC} and GND at 125°C ⁽⁴⁾		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
R _{θJA}	SC70-6	Thermal Characteristics, Thermal Resistance, Junction-to-air	280	°C/W
	SOT23-6		180	
P _D	SC70-6	Power Dissipation in Still Air at 85°C	230	mW
	SOT23-6		360	

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage Operating	1.65	5.5	V
V _I	DC Input Voltage	0	V _{CC}	V
V _O	DC Output Voltage (High or Low State)	0	V _{CC}	V
T _A	Operating Temperature Range	-40	125	°C

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Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameters	Conditions	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{OL}	LOW-Level Output Voltage	V _I = V _{T+} or V _{T-}							
		I _{OL} = 100μA	1.65~5.5			0.1		0.10	V
		I _{OL} = 4mA	1.65			0.45		0.7	V
		I _{OL} = 8mA	2.3			0.3		0.45	V
		I _{OL} = 12mA	2.7			0.4		0.6	V
		I _{OL} = 24mA	3.0			0.55		0.8	V
		I _{OL} = 32mA	4.5			0.55		0.8	V
V _{OH}	HIGH-Level Output Voltage	V _I = V _{T+} or V _{T-}							
		I _{OH} = -100μA	1.65~5.5	V _{CC} - 0.1			V _{CC} - 0.1		V
		I _{OH} = -4mA	1.65	1.2			0.95		V
		I _{OH} = -8mA	2.3	1.9			1.7		V
		I _{OH} = -12mA	2.7	2.2			1.9		V
		I _{OH} = -24mA	3.0	2.3			2.0		V
		I _{OH} = -32mA	4.5	3.8			3.4		V
I _I	Input Leakage Current	V _I = 5.5V or GND	0~5.5		±0.1	±1		±1	μA
I _{OFF}	Power-Off Leakage Current	V _I = 5.5V or V _O = 5.5V	0		±0.1	±2		±2	μA
I _{CC}	Supply Current	V _I = 5.5V or GND; I _O = 0mA	1.65~5.5		0.1	4		4	μA
ΔI _{CC}	Additional Supply Current	Per Pin: V _I = V _{CC} - 0.6V; I _O = 0mA	2.3~5.5		5	500		500	μA

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Electrical Characteristics (Continued)

AC Electrical Characteristics

$t_r = t_f = 3\text{ns}$

Symbol	Parameter	Condition	$V_{CC}(V)$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PHL} , t_{PLH}	Propagation Delay (See Figure 10 and 11)	$R_L = 1\text{k}\Omega$; $C_L = 30\text{pF}$	1.65~1.95	2.0	10.1	19.8	2.0	21.9	ns
		$R_L = 500\Omega$; $C_L = 30\text{pF}$	2.3~2.7	1.5	6.0	11.5	1.5	14.2	
		$R_L = 500\Omega$; $C_L = 50\text{pF}$	2.7	1.5	5.0	9.6	1.5	10.8	
		$R_L = 500\Omega$; $C_L = 50\text{pF}$	3.0~3.6	1.5	4.5	9.2	1.5	10.2	
		$R_L = 500\Omega$; $C_L = 50\text{pF}$	4.5~5.5	1.5	3.9	7.4	1.5	8.1	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5\text{V}$, $V_I = 0\text{V}$ or V_{CC}	3.8	pF
C_{PD}	Power Dissipation Capacitance ⁽⁵⁾	10MHz, $V_{CC} = 3.3\text{V}$, $V_I = 0\text{V}$ or V_{CC}	10	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

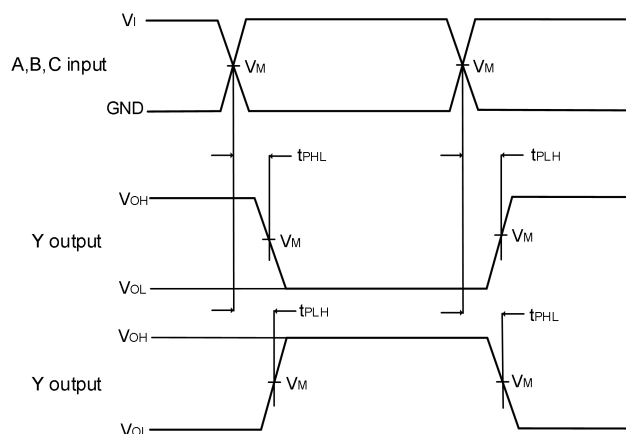
V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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Test Waveform



Measurement points are given in [Table1](#).

V_{OL} and V_{OH} is typical output voltage levels that occur with the output load.

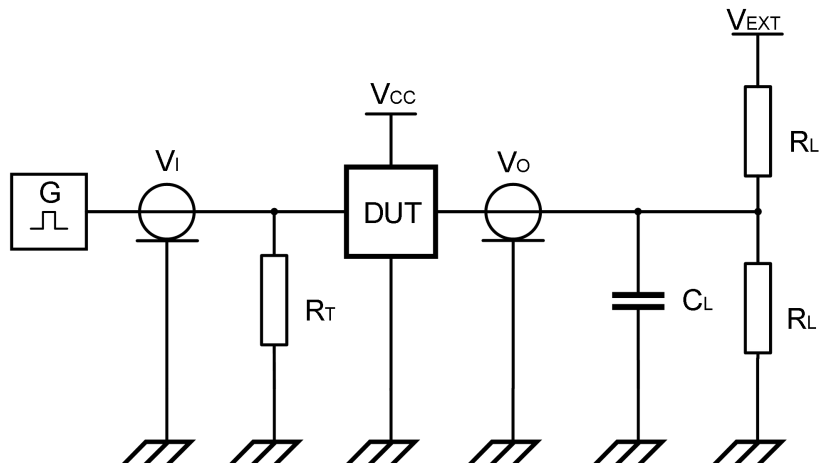
Figure10. Input A, B, C to Output xY Propagation Delay Times

Table1. Measurement Points

Supply Voltage	Input	Output
V_{CC}	V_M	V_M
1.65V to 1.95V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3V to 2.7V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7V	1.5V	1.5V
3.0V to 3.6V	1.5V	1.5V
4.5V to 5.5V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

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Test Circuit



Measurement points are given in [Table2](#).

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Figure11. Test Circuit for Measuring Switching Times

Table2. Test Data

Supply Voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65V to 1.95V	V_{CC}	3.0ns	30pF	1k Ω	OPEN
2.3V to 2.7V	V_{CC}	3.0ns	30pF	500 Ω	OPEN
2.7V	2.7V	3.0ns	50pF	500 Ω	OPEN
3.0V to 3.6V	2.7V	3.0ns	50pF	500 Ω	OPEN
4.5V to 5.5V	V_{CC}	3.0ns	50pF	500 Ω	OPEN

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Electrical Characteristics(Continued)

Transfer Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameters	Conditions	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	
V _{T+}	Positive-going Threshold Voltage	See Figure12, 13, 14, 15						
		V _{CC} = 1.8V	0.85	1.1	1.45	0.75	1.4	V
		V _{CC} = 2.3V	1.05	1.3	1.75	0.95	1.7	V
		V _{CC} = 3.0V	1.4	1.7	2.15	1.3	2.1	V
		V _{CC} = 4.5V	2.0	2.3	2.95	1.9	2.9	V
		V _{CC} = 5.5V	2.4	2.7	3.35	2.3	3.3	V
V _{T-}	Negative-going Threshold Voltage	See Figure12, 13, 14, 15						
		V _{CC} = 1.8V	0.4	0.6	0.8	0.4	0.83	V
		V _{CC} = 2.3V	0.58	0.8	1	0.58	1.03	V
		V _{CC} = 3.0V	0.8	1.05	1.3	0.8	1.33	V
		V _{CC} = 4.5V	1.21	1.5	1.9	1.21	1.93	V
		V _{CC} = 5.5V	1.5	1.8	2.34	1.5	2.36	V
V _H	Hysteresis Voltage	See Figure12, 13, 14, 15						
		V _{CC} = 1.8V	0.3	0.47	0.95	0.25	0.95	V
		V _{CC} = 2.3V	0.4	0.52	0.97	0.33	0.97	V
		V _{CC} = 3.0V	0.5	0.6	1.05	0.44	1.05	V
		V _{CC} = 4.5V	0.6	0.77	1.3	0.54	1.3	V
		V _{CC} = 5.5V	0.7	0.87	1.55	0.64	1.55	V

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Wave-forms Transfer Characteristics

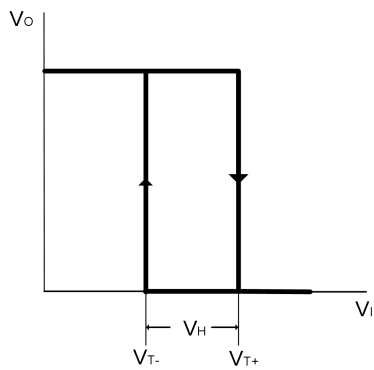
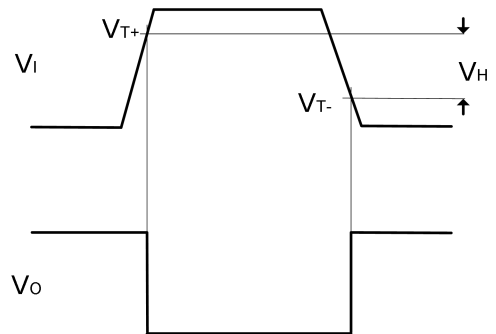


Figure12. Transfer characteristic



V_{T+} and V_{T-} limits are at 70% and 20%
Figure13. Definition of V_{T+} , V_{T-} and V_H

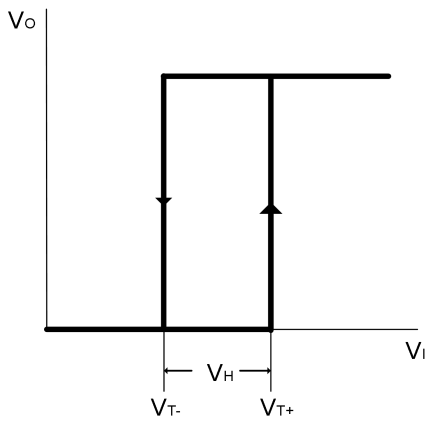
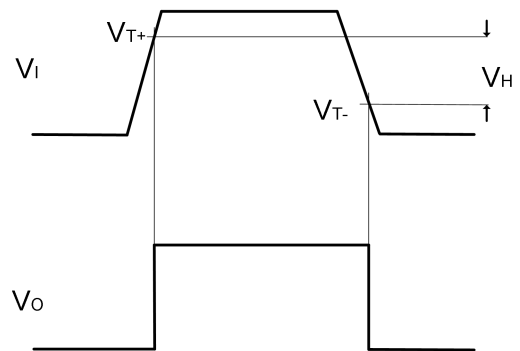


Figure14. Transfer characteristic



V_{T+} and V_{T-} limits are at 70% and 20%
Figure15. Definition of V_{T+} , V_{T-} and V_H

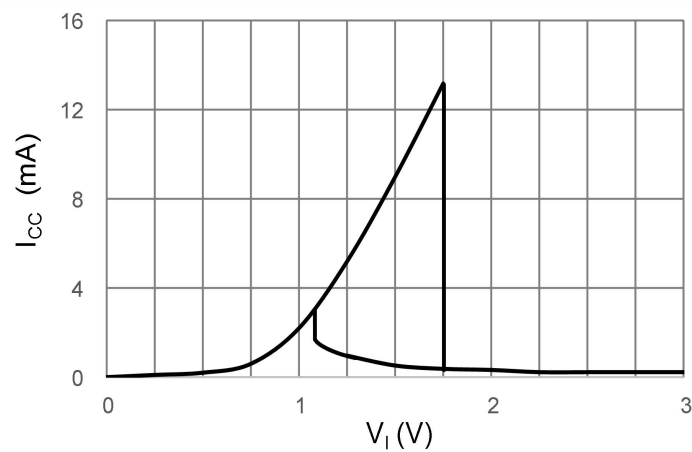


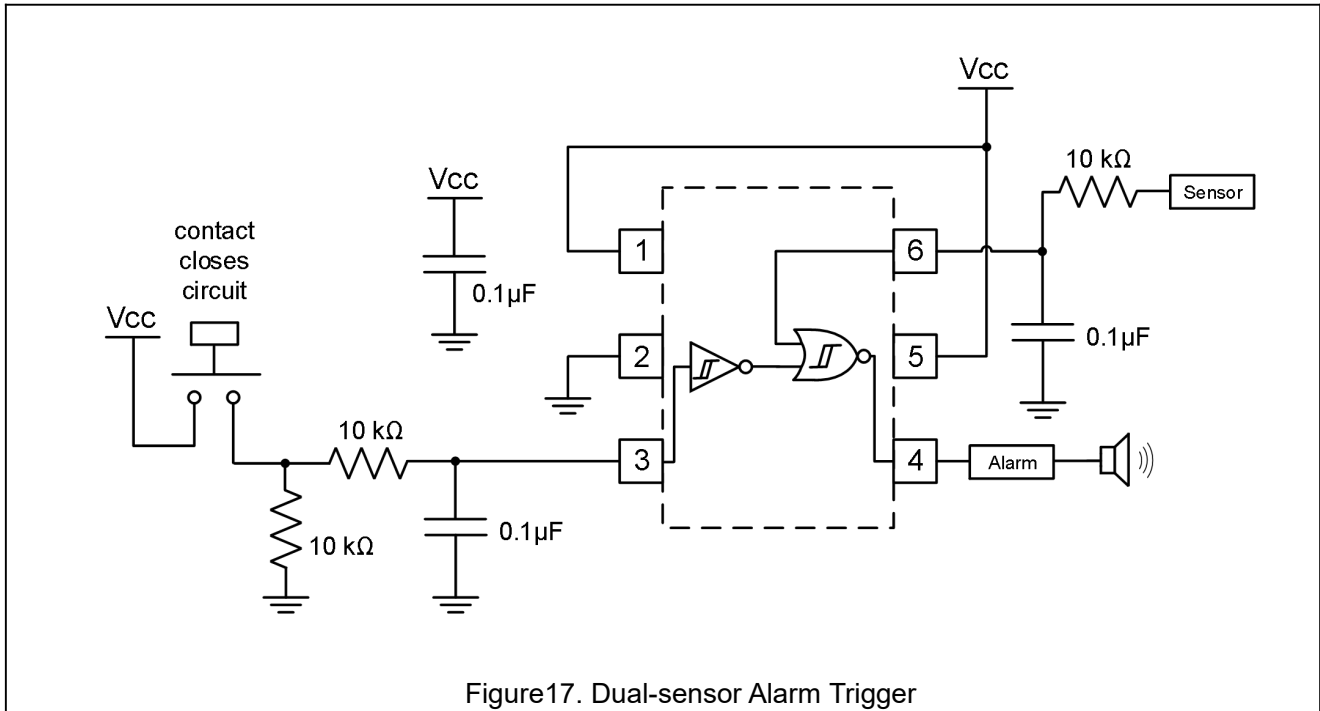
Figure16. Typical ET74LVC1G58 transfer characteristic; $V_{CC} = 3.0V$

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Application Circuits

This application shows the ET74LVC1G58 configured as an NOR gate with an inverted input. This particular configuration is helpful for dual sensor or switch applications where one of the inputs is normally closed or a logic high 1. Normally this application would require two external gates, but because the ET74LVC1G58 can be configured to meet this function the application can be implemented with a single chip solution.

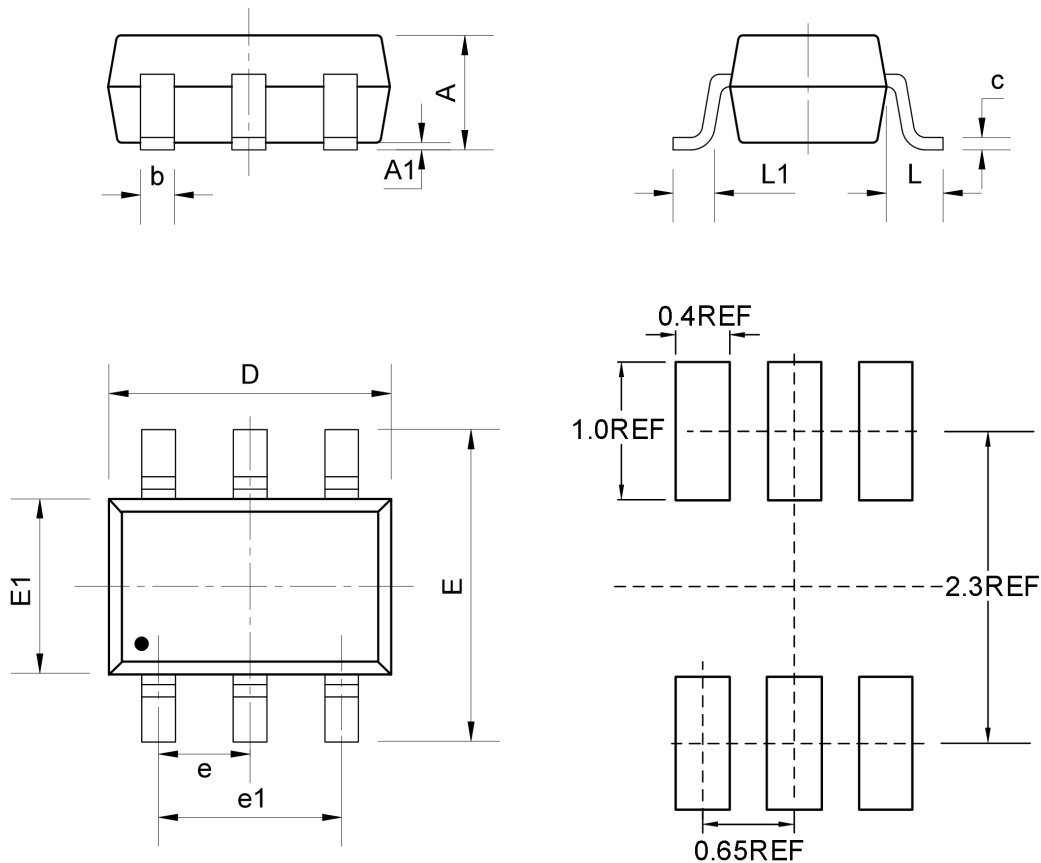
This application circuit is for reference only.



ET74LVC1G58

Package Dimension

SC70-6 (1.3mm × 2.1mm)



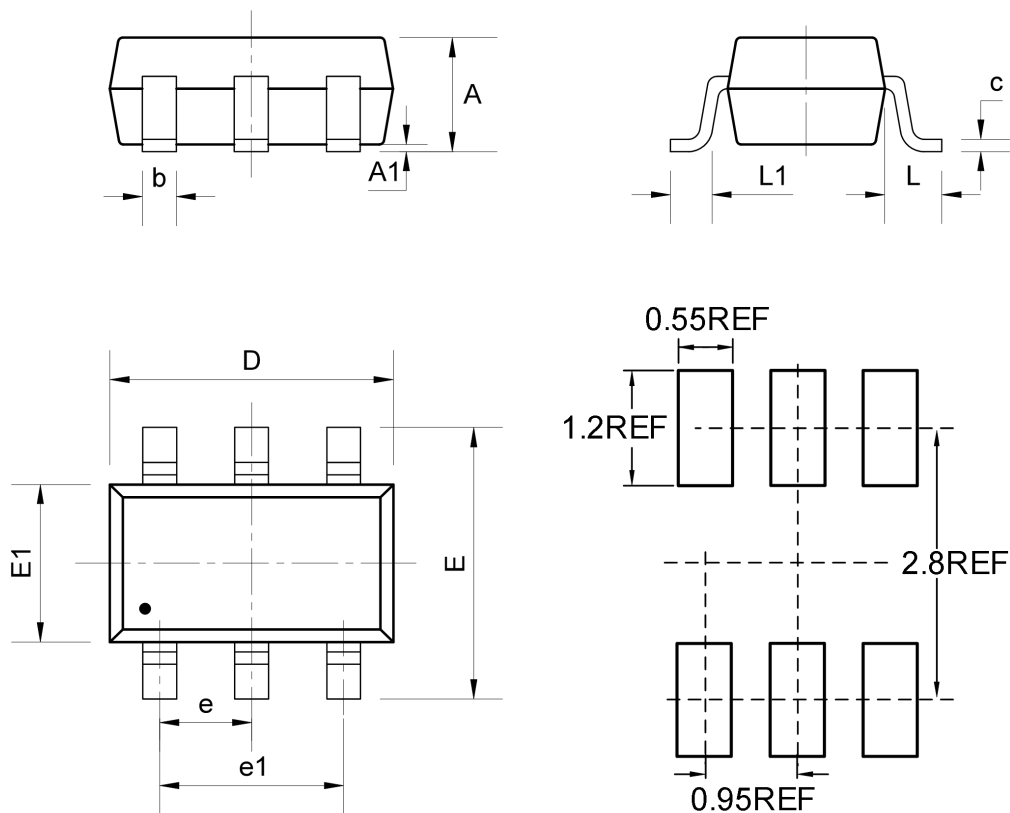
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
b	0.15	-	0.35
c	0.08	-	0.20
D	2.00	2.10	2.30
e	0.65BSC		
e1	1.30BSC		
E	2.15	2.30	2.50
E1	1.15	1.30	1.45
L	0.50REF		
L1	0.33REF		

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SOT23-6 (1.6mm × 2.9mm)



COMMON DIMENSIONS

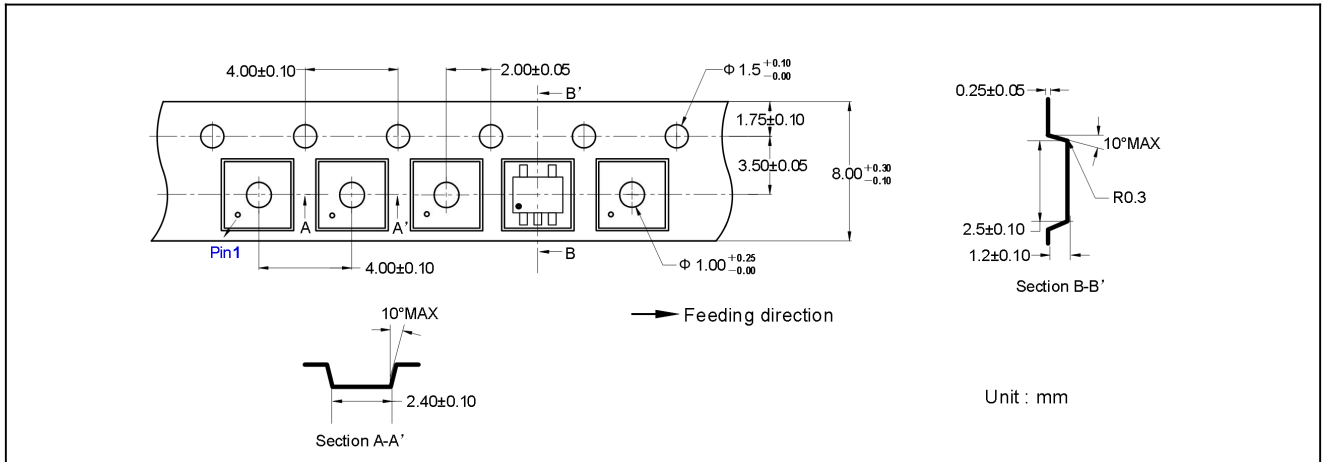
(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0.00	-	0.15
b	0.28	0.35	0.50
c	0.08	0.15	0.22
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

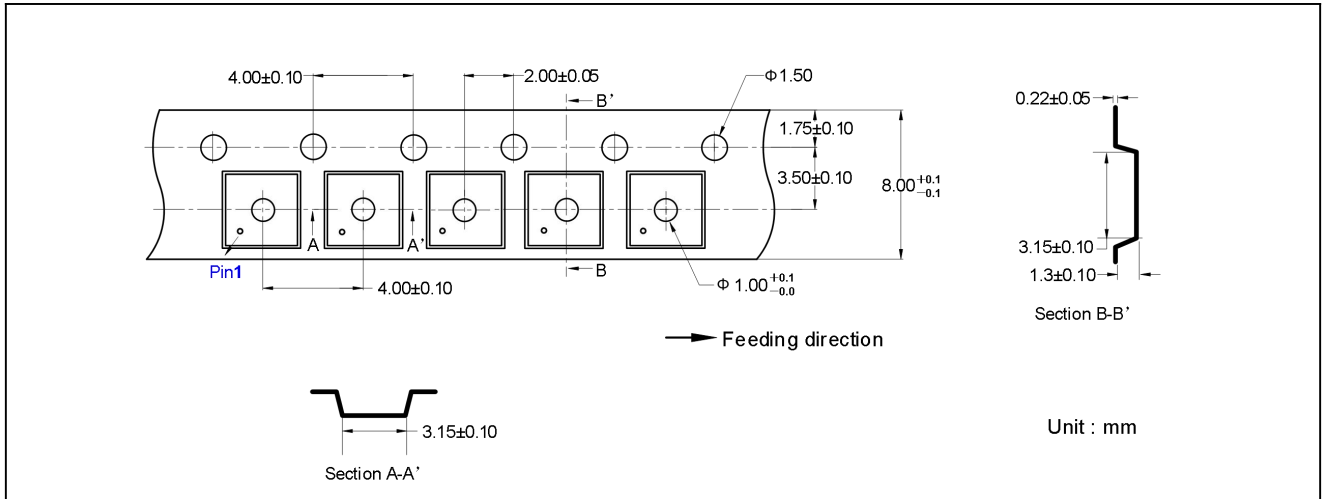
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Tape Information

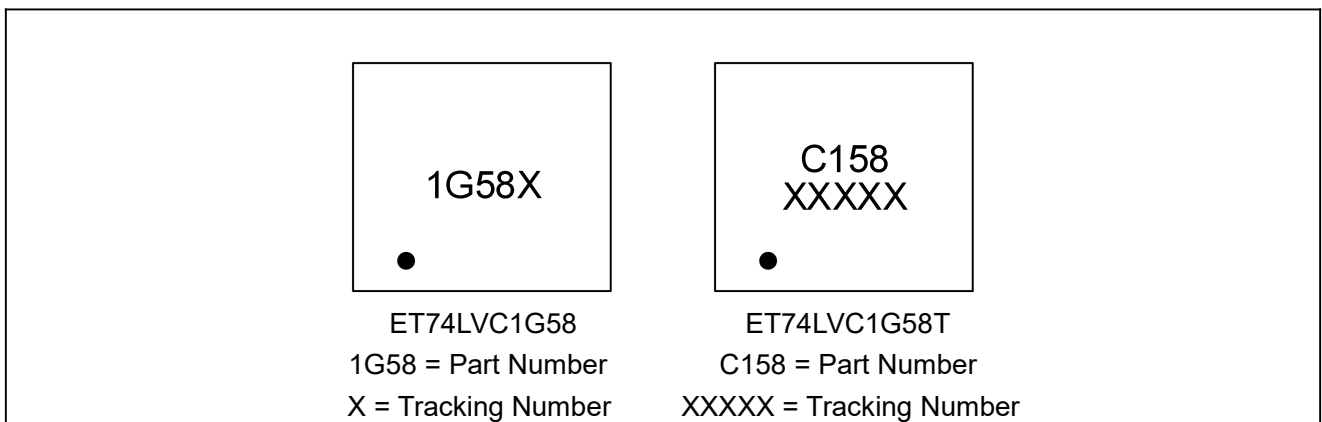
SC70-6 (1.3mm × 2.1mm)



SOT23-6 (1.6mm × 2.9mm)



Marking Information



ET74LVC1G58

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-05-18	Preliminary Version	Wang anran	Tu guozhu	Liu jiaying
0.1	2024-11-21	Update HBM and Transfer Characteristics	Wang anran	Tu guozhu	Liu jiaying
0.2	2025-05-27	Add Packing Option	Yang xiaoxu	Yang xiaoxu	Liu jiaying
1.0	2025-06-13	Official Version	Wang anran	Yang xiaoxu	Liu jiaying
1.0.a	2025-11-19	Update Format	Yang xiaoxu	Yang xiaoxu	Liu jiaying
1.1	2025-12-01	Update Format and EC table Characteristics	Xu tao	Yang xiaoxu	Liu jiaying