

Hex Non-Inverting Buffer

General Description

The ET74HC34 is a high-performance hex non-inverting buffer gate operating from a 2.0V to 6.0V supply. This device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive.

Features

- Designed for 2.0V to 6.0V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 6.0V
- $\pm 5.2\text{mA}$ Balanced Output Sink and Source Capability
- CMOS Low-Power Consumption and High Noise Immunity
- I_{OFF} Supports Partial-Power-Down Mode Operation
- ESD Protection Complies with JESD22 Standard
 - HBM: $\pm 4000\text{V}$ Pass (JEDEC JS-001)
 - CDM: $\pm 1000\text{V}$ Pass (JEDEC JS-002)
- Latch-up Performance Exceeds $\pm 100\text{mA}$ Per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	MSL
ET74HC34M	SOP14 (3.9mm × 8.65mm)	3
ET74HC34V	TSSOP14 (4.4mm × 5.0mm)	3

Pin Configuration

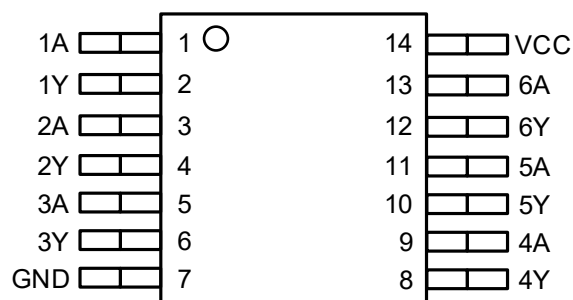


Figure1. Pin Configuration

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Pin Function

SOP14/TSSOP14

Pin No.	Pin Name	Function
1	1A	Channel 1, Input A
2	1Y	Channel 1, Output Y
3	2A	Channel 2, Input A
4	2Y	Channel 2, Output Y
5	3A	Channel 3, Input A
6	3Y	Channel 3, Output Y
7	GND	Ground
8	4Y	Channel 4, Output Y
9	4A	Channel 4, Input A
10	5Y	Channel 5, Output Y
11	5A	Channel 5, Input A
12	6Y	Channel 6, Output Y
13	6A	Channel 6, Input A
14	VCC	Supply Voltage

Block Diagram

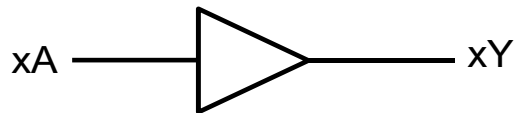


Figure2. Logic Symbol

Functional Table

Input	Output
xA	xY
L	L
H	H

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Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 7.0	V
V _I	DC Input Voltage ⁽¹⁾		-0.5 ≤ V _I ≤ 7.0	V
I _{IK}	DC Input Diode Current, V _I < GND		±20	mA
I _{OK}	DC Output Diode Current, V _O < GND, V _O > V _{CC}		±20	mA
I _O	DC Output Sink Current		±25	mA
I _{CC}	DC Supply Current per Supply Pin		50	mA
I _{GND}	DC Supply Current GND Pin		-50	mA
T _{STG}	Storage Temperature Range		-65 to 150	°C
V _{ESD}	ESD Classification	Human Body Model ⁽²⁾	±4000	V
		Charged Device Model ⁽³⁾	±1000	
I _{LU}	Max Latch Up Current Above V _{CC} and GND at 125°C ⁽⁴⁾		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage Operating	2	6	V
V _I	DC Input Voltage	0	V _{CC}	V
V _O	DC Output Voltage (High or Low State)	0	V _{CC}	V
T _A	Operating Temperature Range	-40	125	°C

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Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V _{IL}	Low-Level Input Voltage		2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V _{OH}	High-Level Output Voltage	I _{OH} = -20μA	2	1.9	1.998		1.9		V
			4.5	4.4	4.499		4.4		
			6	5.9	5.999		5.9		
		I _{OH} = -4mA	4.5	3.98	4.3		3.84		
		I _{OH} = -5.2mA	6	5.48	5.8		5.34		
V _{OL}	Low-Level Output Voltage	I _{OL} = 20μA	2		0.002	0.1		0.1	V
			4.5		0.001	0.1		0.1	
			6		0.001	0.1		0.1	
		I _{OL} = 4mA	4.5		0.17	0.26		0.33	
		I _{OL} = 5.2mA	6		0.15	0.26		0.33	
I _I	Input Leakage Current	V _I = 6V or GND	6		±0.1	±100		±1000	nA
I _{CC}	Quiescent Supply Current	V _I = 6V or GND	6			2		20	μA

AC Electrical Characteristics

t_r = t_f = 3ns

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay (Figure3 and 4)	C _L = 50pF	2.0		31	121		141	ns
		C _L = 50pF	4.5		11	25		29	
		C _L = 15pF	5.0		9				
		C _L = 50pF	6.0		10	22		25	

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Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	$V_{CC} = 6V, V_I = 0V \text{ or } V_{CC}$	2.5	pF
C_{PD}	Power Dissipation Capacitance ⁽⁵⁾	10MHz, $V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	21	pF
		10MHz, $V_{CC} = 6V, V_I = 0V \text{ or } V_{CC}$	21	

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

AC Test Circuit

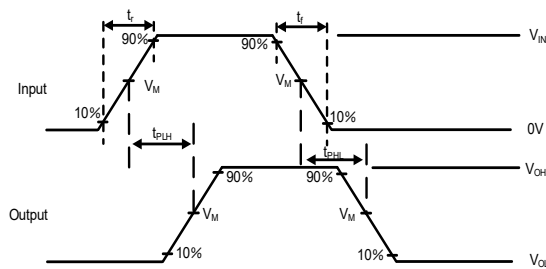


Figure3. Switching Waveform

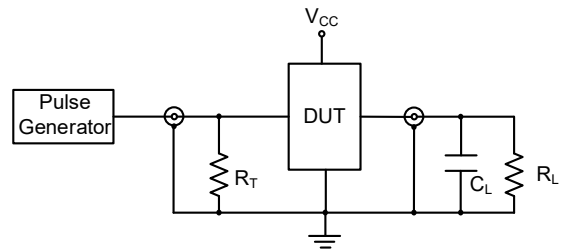
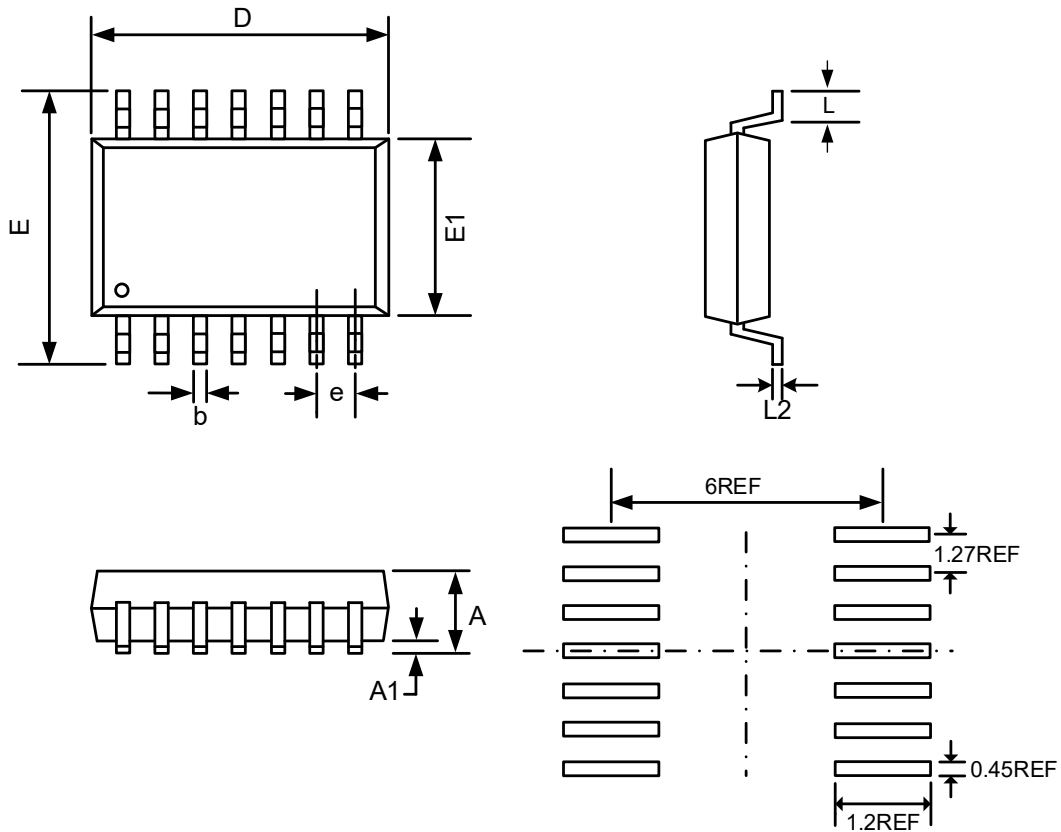


Figure4. Test Circuit

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Package Dimension

SOP14 (3.9mm × 8.65mm)



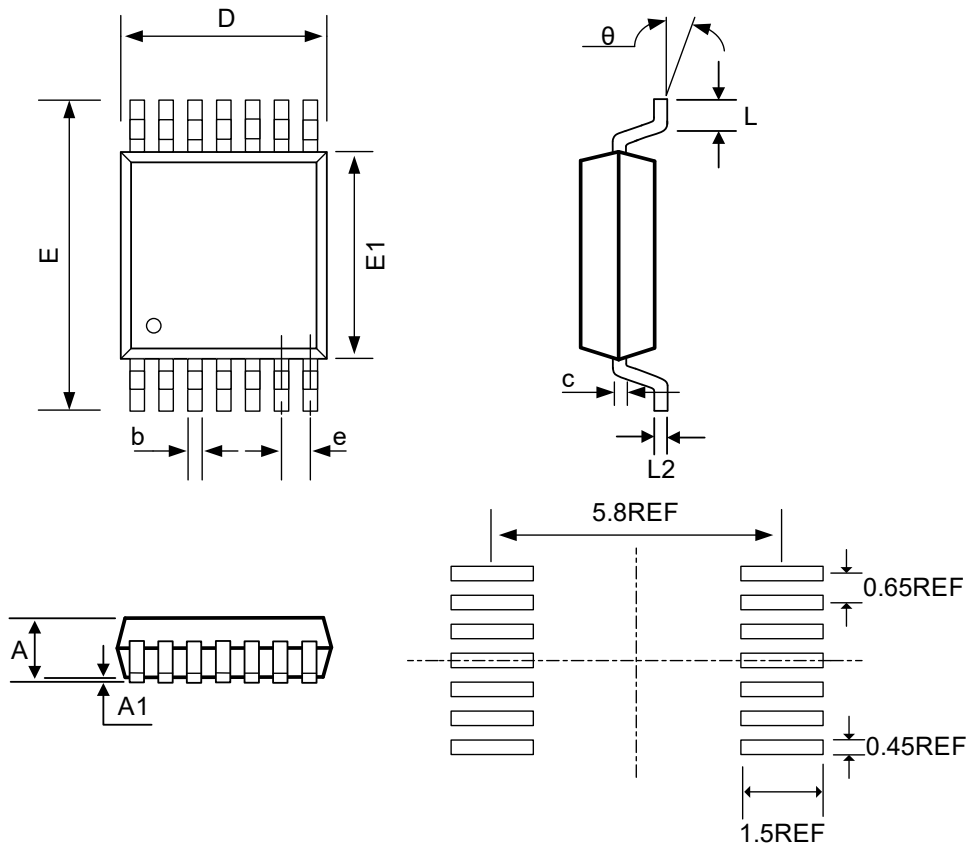
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	MAX
A	--	1.75
A1	0.10	0.25
b	0.36	0.51
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.22	1.32
L	0.45	0.75
L2	0.25 BSC	

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TSSOP14 (4.4mm × 5.0mm)



COMMON DIMENSIONS

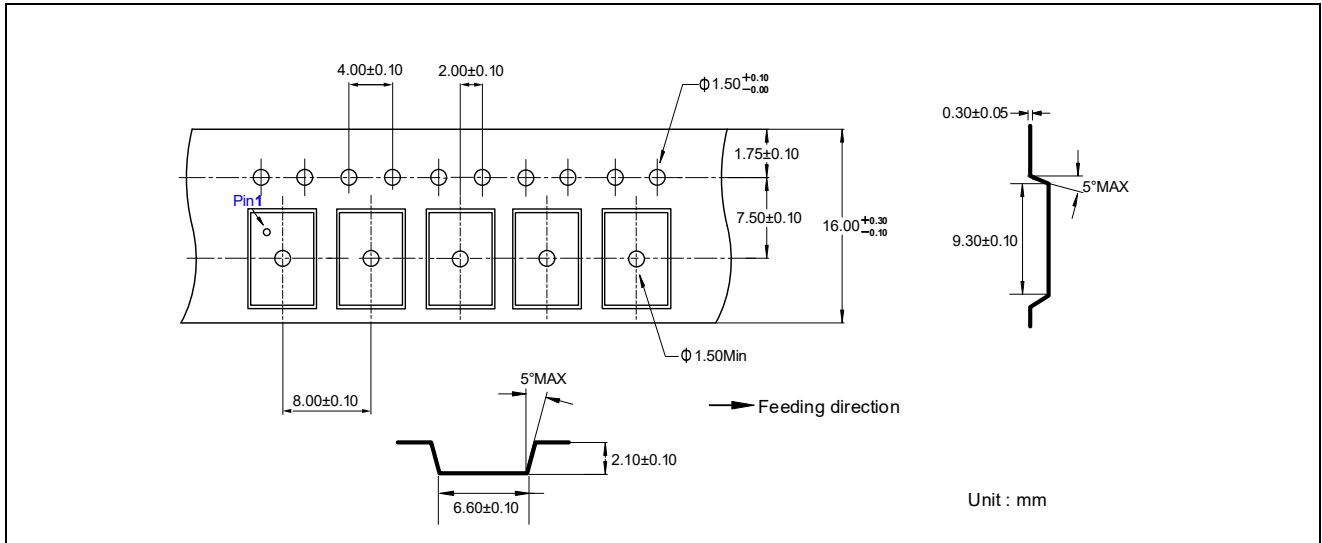
(Unit: mm)

SYMBOL	MIN	MAX
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 REF	
D	4.86	5.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L2	0.25 REF	
θ	0°	8°

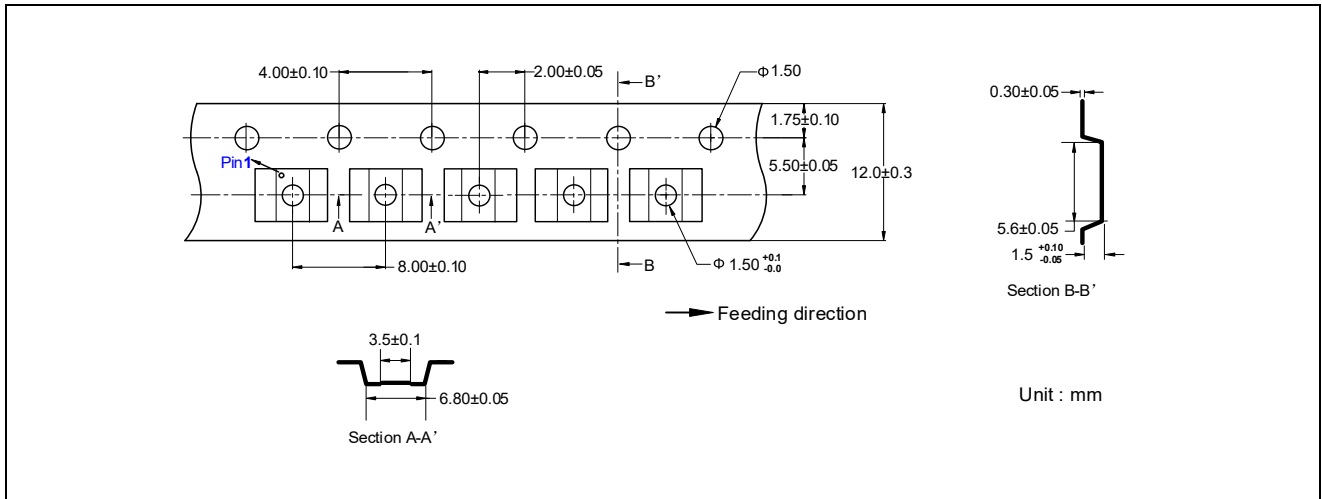
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Tape Information

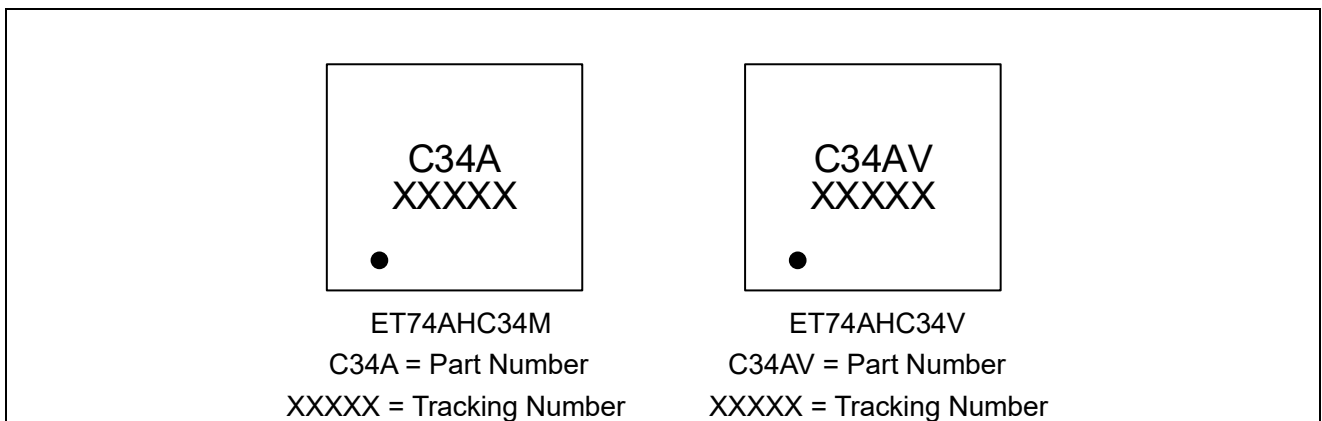
SOP14 (3.9mm × 8.65mm)



TSSOP14 (4.4mm × 5.0mm)



Marking Information



ET74HC34

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-03-24	Official Version	Xu tao	Yang xiaoxu	Liu jiaying