

Dual 2-Input Positive-OR Gate

General Description

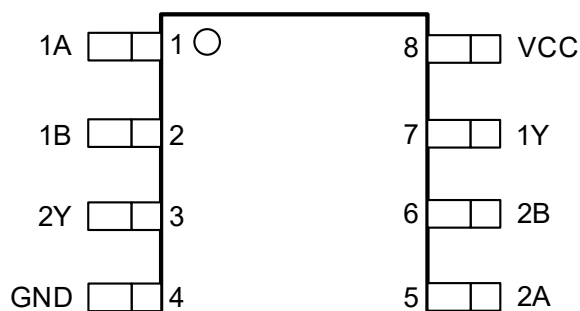
The ET74HC2G32 is a dual 2-input positive-OR gate operating from a 2V to 6V supply. This device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive.

Features

- Designed for 2V to 6V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 6V
- $\pm 5.2\text{mA}$ Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- ESD Protection Complies with JESD22 Standard
 - HBM: $\pm 2000\text{V}$ Pass (JEDEC JS-001)
 - CDM: $\pm 1000\text{V}$ Pass (JEDEC JS-002)
- Latch-up Performance Exceeds $\pm 100\text{mA}$ per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74HC2G32U	VSSOP8 (2.0mm $\times$ 2.3mm)	Tape and Reel, 3K/Reel	3
ET74HC2G32U1	MSOP8 (3.0mm $\times$ 3.0mm)	Tape and Reel, 3K/Reel	3

Pin Configuration



VSSOP8/MSOP8

Figure1. Pin Configuration

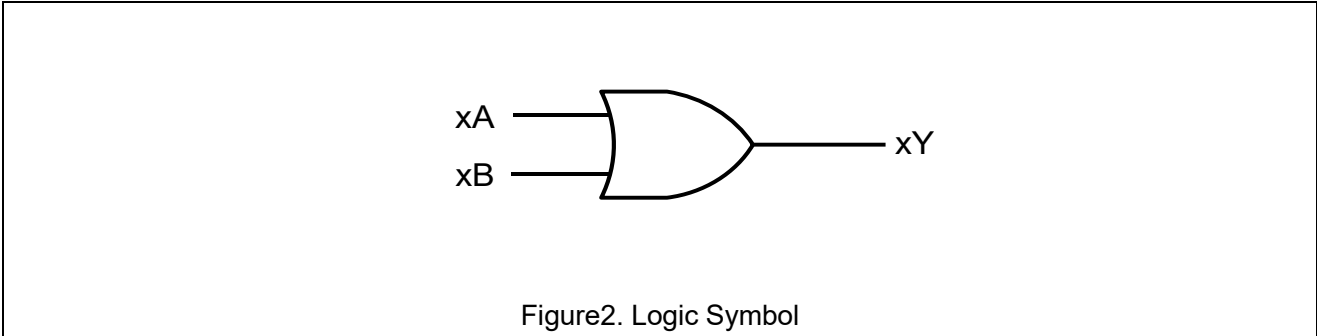
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Pin Function

VSSOP8/MSOP8

Pin No.	Pin Name	Function
1	1A	Channel 1, Input A
2	1B	Channel 1, Input B
3	2Y	Channel 2, Output Y
4	GND	Ground
5	2A	Channel 2, Input A
6	2B	Channel 2, Input B
7	1Y	Channel 1, Output Y
8	VCC	Supply Voltage

Block Diagram



Functional Table

Input		Output
xA	xB	xY
L	L	L
L	H	H
H	L	H
H	H	H

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Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 7.0	V
I _{IK}	DC Input Diode Current, V _I < GND		-50	mA
V _I	DC Input Voltage ⁽¹⁾		-0.5 ≤ V _I ≤ 7.0	V
I _{OK}	DC Output Diode Current, V _O < GND		±50	mA
V _O	DC Output Voltage Output in Higher or Low State		-0.5 to V _{CC} + 0.5	V
I _O	DC Output Sink Current, V _O = -0.5V to V _{CC} + 0.5V		±50	mA
I _{CC}	DC Supply Current per Supply Pin		100	mA
I _{GND}	DC Ground Current per Supply Pin		-100	mA
T _J	Max Junction Temperature		150	°C
T _{STG}	Storage Temperature Range		-65 to 150	°C
V _{ESD}	ESD Classification	Human Body Model ⁽²⁾	±2000	V
		Charged Device Model ⁽³⁾	±1000	
I _{LU}	Max Latch Up Current Above V _{CC} and GND at 125°C ⁽⁴⁾		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage Operating		2	6	V
V _I	DC Input Voltage		0	V _{CC}	V
V _O	DC Output Voltage (High or Low State)		0	V _{CC}	V
T _A	Operating Temperature Range		-40	125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2.0V		625	ns/V
		V _{CC} = 4.5V		139	
		V _{CC} = 6.0V		83	

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Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0	1.5	1.2		1.5		V
			4.5	3.15	2.4		3.15		
			6.0	4.2	3.2		4.2		
V _{IL}	Low-Level Input Voltage		2.0		0.8	0.5		0.5	V
			4.5		2.1	1.35		1.35	
			6.0		2.8	1.8		1.8	
V _{OH}	High-Level Output Voltage	I _{OH} = -20uA	2~6	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V
		I _{OH} = -4mA	4.5	4.13	4.32		3.7		
		I _{OH} = -5.2mA	6.0	5.63	5.81		5.2		
V _{OL}	Low-Level Output Voltage	I _{OL} = 100uA	2~6		0.0	0.1		0.1	V
		I _{OL} = 4mA	4.5		0.15	0.33		0.4	
		I _{OL} = 5.2mA	6.0		0.16	0.33		0.4	
I _I	Input Leakage Current	V _I = 6V or GND	0~6		±0.1			±1.0	μA
I _{CC}	Quiescent Supply Current	V _I = 6V or GND	6			1		20	μA

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AC Electrical Characteristics

$t_r = t_f = 3\text{ns}$, $R_L = 1\text{k}\Omega$

Symbol	Parameter	Condition	$V_{CC}(\text{V})$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure3 and 4)	$C_L = 50\text{pF}$	2.0		17	22		22.8	ns
		$C_L = 50\text{pF}$	4.5		3.9	5.1		5.5	
		$C_L = 50\text{pF}$	6.0		3.6	4.6		5.1	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	$V_{CC} = 6\text{V}$, $V_I = 0\text{V}$ or V_{CC}	5	pF
C_{PD}	Power Dissipation Capacitance (5)	10MHz, $V_{CC} = 3.3\text{V}$, $V_I = 0\text{V}$ or V_{CC}	25	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

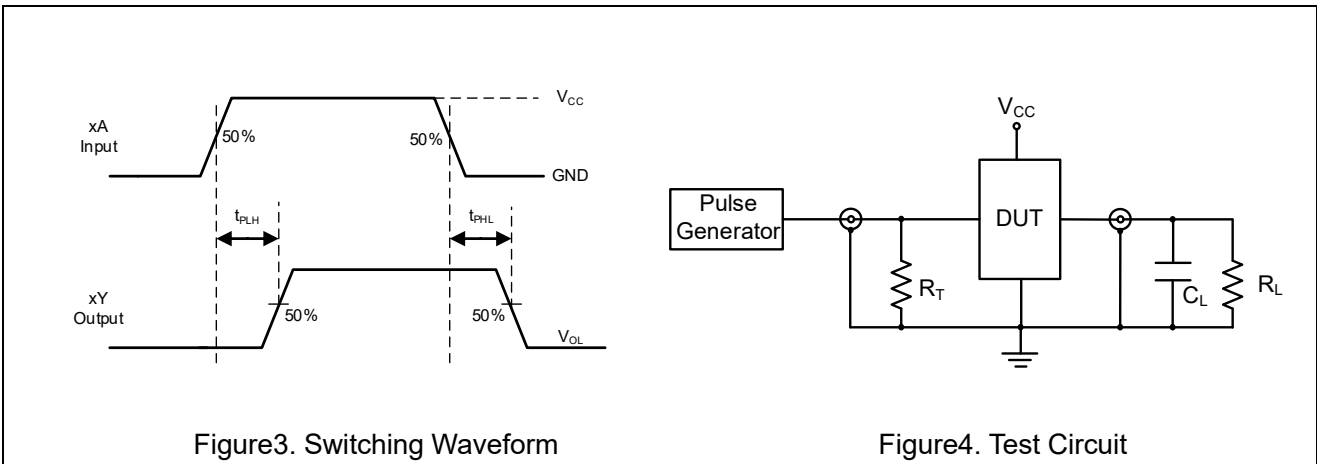
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

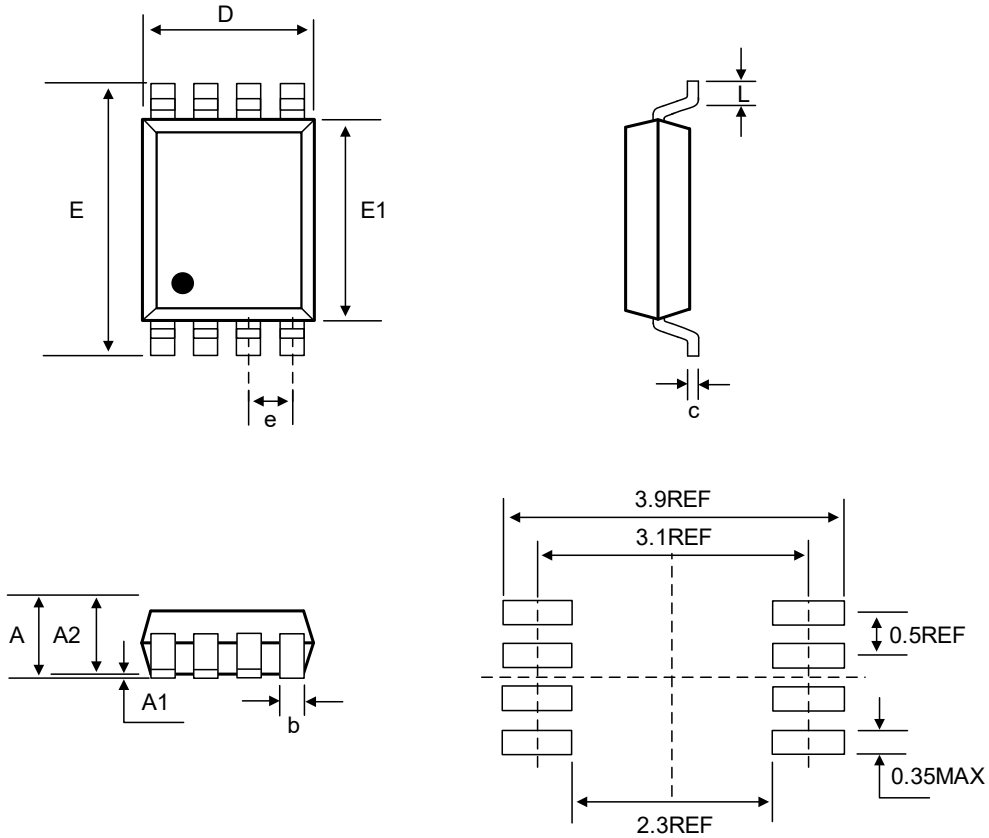
AC Test Circuit



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Package Dimension

VSSOP8 (2.0mm × 2.3mm)



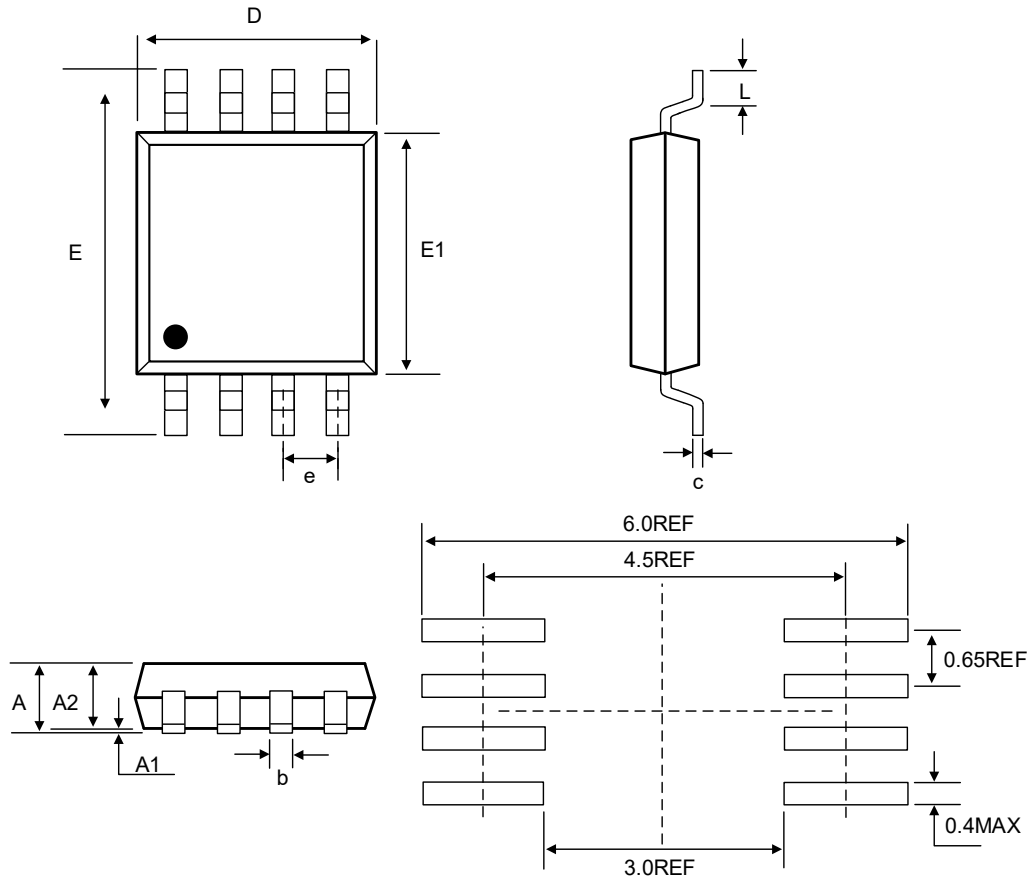
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	0.90
A1	0.00	-	0.10
A2	0.65	0.75	0.80
b	0.17	-	0.27
c	0.08	-	0.20
D	1.90	2.00	2.10
E	3.00	3.10	3.20
E1	2.20	2.30	2.40
e	0.50BSC		
L	0.20	-	0.35

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MSOP8 (3.0mm × 3.0mm)



COMMON DIMENSIONS
(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
A2	0.75	0.85	0.95
b	0.22	0.30	0.38
c	0.08	0.1	0.20
D	2.90	3.00	3.10
E	3.90	-	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.33	-	0.7

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Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-11-14	Official Version	Xu tao	Yang xiaoxu	Liu jiaying