

Single Bus Buffer Gate with 3-State Output

General Description

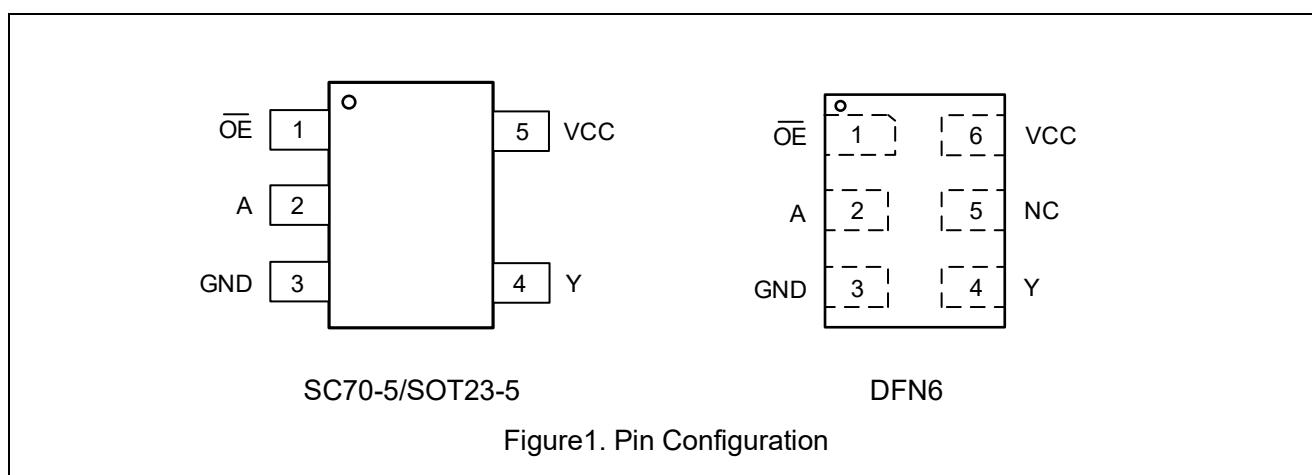
The ET74AHC1G125 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, data is passed from the A input to the Y output.

Features

- Designed for 2V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- $\pm 8\text{mA}$ Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- 3-State OE Input is Active-Low
- ESD Protection Complies with JESD22 Standard
 - HBM: $\pm 4000\text{V}$ Pass (JEDEC JS-001)
 - CDM: $\pm 1000\text{V}$ Pass (JEDEC JS-002)
- Latch-up Performance Exceeds $\pm 100\text{mA}$ per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74AHC1G125	SC70-5 (1.3mm × 2.1mm)	Tape and Reel, 3K/Reel	1
ET74AHC1G125T	SOT23-5 (1.6mm × 2.9mm)	Tape and Reel, 3K/Reel	3
ET74AHC1G125Y	DFN6 (1.0mm × 1.5mm)	Tape and Reel, 3K/Reel	1

Pin Configuration



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Pin Function

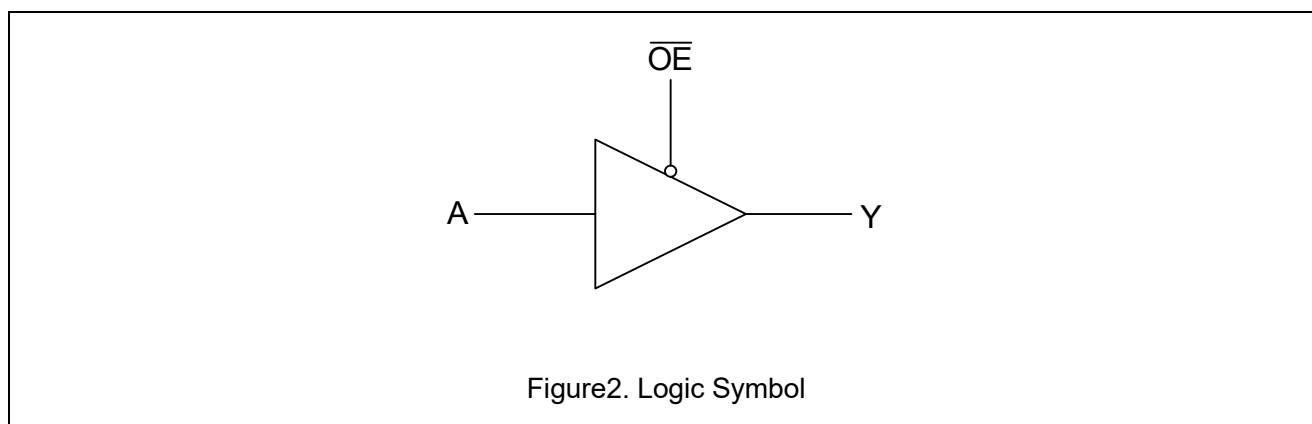
SC70-5/ SOT23-5

Pin No.	Pin Name	Function
1	$\overline{\text{OE}}$	Enable Input
2	A	Input
3	GND	Ground
4	Y	Output
5	VCC	Supply Voltage

DFN6

Pin No.	Pin Name	Function
1	$\overline{\text{OE}}$	Enable Input
2	A	Input
3	GND	Ground
4	Y	Output
5	NC	No Connect
6	VCC	Supply Voltage

Block Diagram



Function Table

Input		Output
$\overline{\text{OE}}$	A	Y
L	L	L
L	H	H
H	X	Z

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Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 7.0	V
V_I	DC Input Voltage ⁽¹⁾		$-0.5 \leq V_I \leq 7.0$	V
V_O	DC Output Voltage Output in Higher or Low State		$-0.5 \leq V_O \leq V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current, $V_I < GND$		-50	mA
I_{OK}	DC Output Diode Current, $V_O < GND$, $V_O > V_{CC}$		± 50	mA
I_O	DC Output Sink Current		± 50	mA
I_{CC}	DC Supply Current Per Supply Pin		100	mA
I_{GND}	DC Ground Current Per Supply Pin		-100	mA
T_{STG}	Storage Temperature Range		-65 to 150	°C
T_L	Lead Temperature, Soldering 10 Seconds		260	°C
T_J	Max Junction Temperature		150	°C
V_{ESD}	ESD Classification	Human Body Model ⁽²⁾	± 4000	V
		Charged Device Model ⁽³⁾	± 1000	
I_{LU}	Max Latch Up Current Above V_{CC} and GND at 125°C ⁽⁴⁾		± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch Up Current Maximum Rating tested per JEDEC JESD78F.

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SC70-5	Thermal Characteristics, Thermal Resistance, Junction-to-Air	300	°C/W
	SOT23-5		250	
	DFN6		440	
P_D	SC70-5	Power Dissipation in Still Air at 85°C	215	mW
	SOT23-5		260	
	DFN6		150	

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Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage Operating	2	5.5	V
V _I	DC Input Voltage	0	V _{CC}	V
V _O	DC Output Voltage (High or Low State)	0	V _{CC}	V
T _A	Operating Temperature Range	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied.

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0	1.5			1.5		V
			3.0	2.1			2.1		
			5.5	3.85			3.85		
V _{IL}	Low-Level Input Voltage		2.0			0.5		0.5	V
			3.0			0.9		0.9	
			5.5			1.65		1.65	
V _{OH}	High-Level Output Voltage	I _{OH} = -50uA	2~5.5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V
		I _{OH} = -4mA	3	2.58			2.4		
		I _{OH} = -8mA	4.5	3.54			3.7		
V _{OL}	Low-Level Output Voltage	I _{OL} = 50uA	2~5.5			0.1		0.1	V
		I _{OL} = 4mA	3			0.36		0.55	
		I _{OL} = 8mA	4.5			0.36		0.55	
I _{IN}	Input Leakage Current	V _I = 5.5V Or GND	0~5.5			0.1		2.0	uA
I _{OFF}	Power Off Leakage Current	V _I = 5.5V or V _O = 5.5V	0			1		10	μA
I _{CC}	Quiescent Supply Current	V _I = 5.5V or GND	5.5			1		40	uA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC Electrical Characteristics

$t_r = t_f = 3\text{ns}$, $R_L = 1\text{k}\Omega$;

Symbol	Parameter	Condition	$V_{CC}(\text{V})$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure3 and 4)	$C_L = 15\text{pF}$	3~3.6		7.5	11	1.0	13.5	ns
		$C_L = 50\text{pF}$	3~3.6		9.5	16	1.0	19	
		$C_L = 15\text{pF}$	4.5~5.5		6.4	8.4	1.0	9.9	
		$C_L = 50\text{pF}$	4.5~5.5		7.9	10.4	1.0	12.4	
t_{PZL} t_{PZH}	Output Enable Time (Figure5 and 6)	$C_L = 15\text{pF}$	3~3.6		8.1	11.4	1.0	14.9	ns
		$C_L = 50\text{pF}$	3~3.6		10	15	1.0	18	
		$C_L = 15\text{pF}$	4.5~5.5		5.8	7.9	1.0	9.4	
		$C_L = 50\text{pF}$	4.5~5.5		7.2	9.9	1.0	11.9	
t_{PLZ} t_{PHZ}	Output Disable Time (Figure5 and 6)	$C_L = 15\text{pF}$	3~3.6		10.2	13.9	1.0	16.9	ns
		$C_L = 50\text{pF}$	3~3.6		12.5	17.5	1.0	20.8	
		$C_L = 15\text{pF}$	4.5~5.5		7.4	10.1	1.0	11.8	
		$C_L = 50\text{pF}$	4.5~5.5		9	12.1	1.0	14.3	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5\text{V}$, $V_I = 0\text{V}$ or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance ⁽⁵⁾	10MHz, $V_{CC} = 3.3\text{V}$, $V_I = 0\text{V}$ or V_{CC}	15	pF
		10MHz, $V_{CC} = 5.5\text{V}$, $V_I = 0\text{V}$ or V_{CC}	15	

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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AC Test Circuit

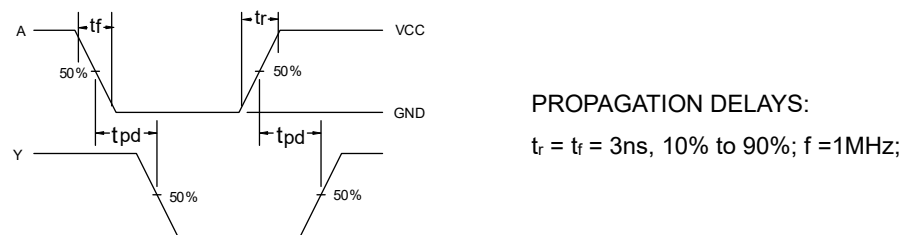
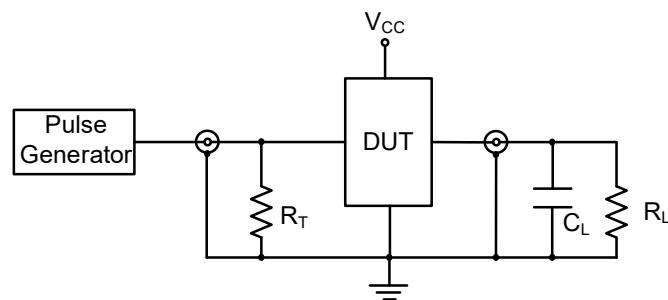


Figure3. Switch Waveform



$R_T = 50\Omega(\text{Typ})$

Figure4. Test Circuit

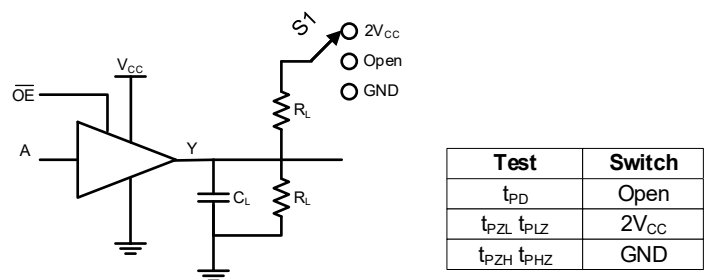


Figure5. Output Enable/Disable Time Test Circuit

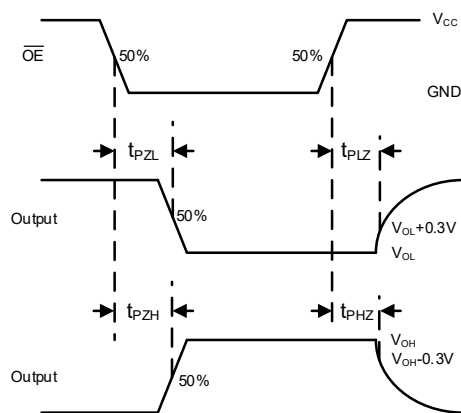
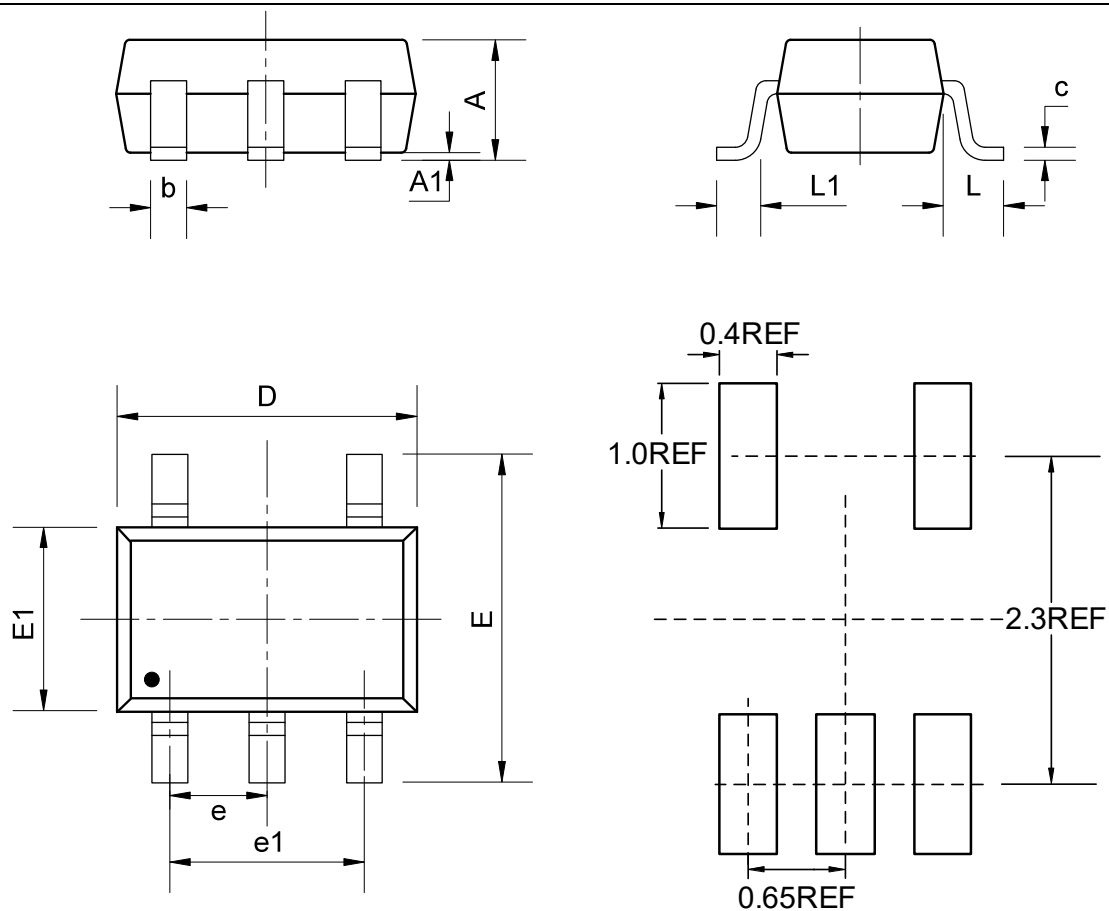


Figure6. Output Enable/Disable Waveform

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Package Dimension

SC70-5 (1.3mm × 2.1mm)



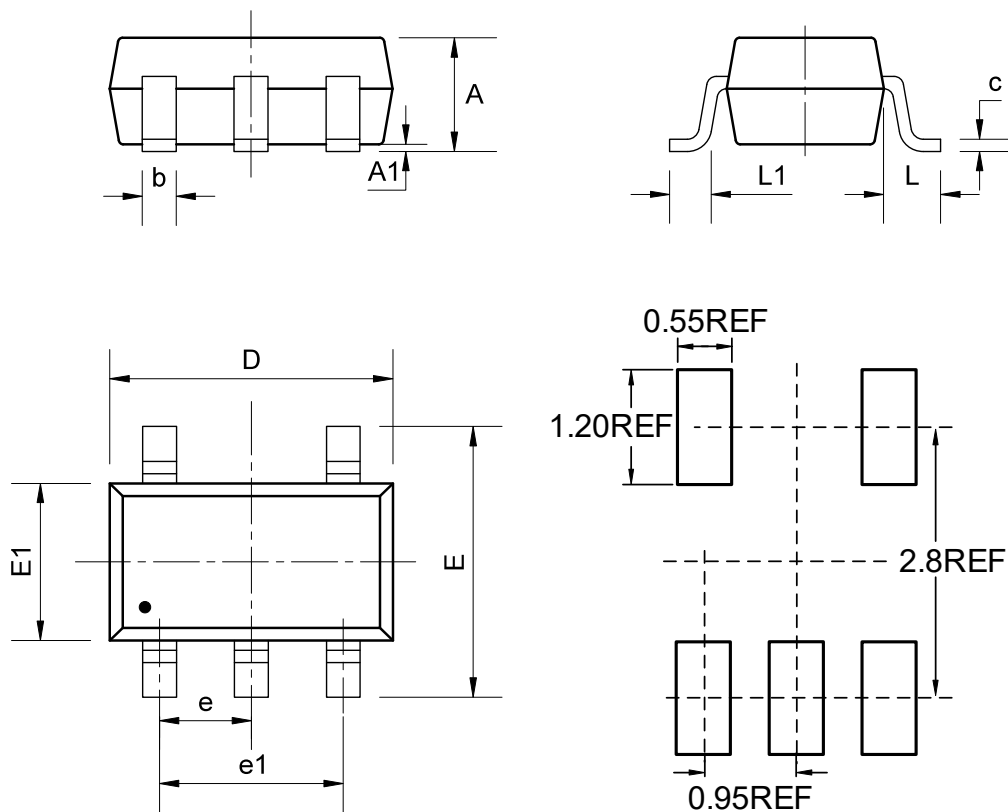
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
b	0.15	-	0.35
c	0.08	-	0.20
D	2.00	2.10	2.30
e	0.65BSC		
e1	1.30BSC		
E	2.15	2.30	2.50
E1	1.15	1.30	1.45
L	0.50REF		
L1	0.33REF		

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SOT23-5(1.6mm × 2.9mm)



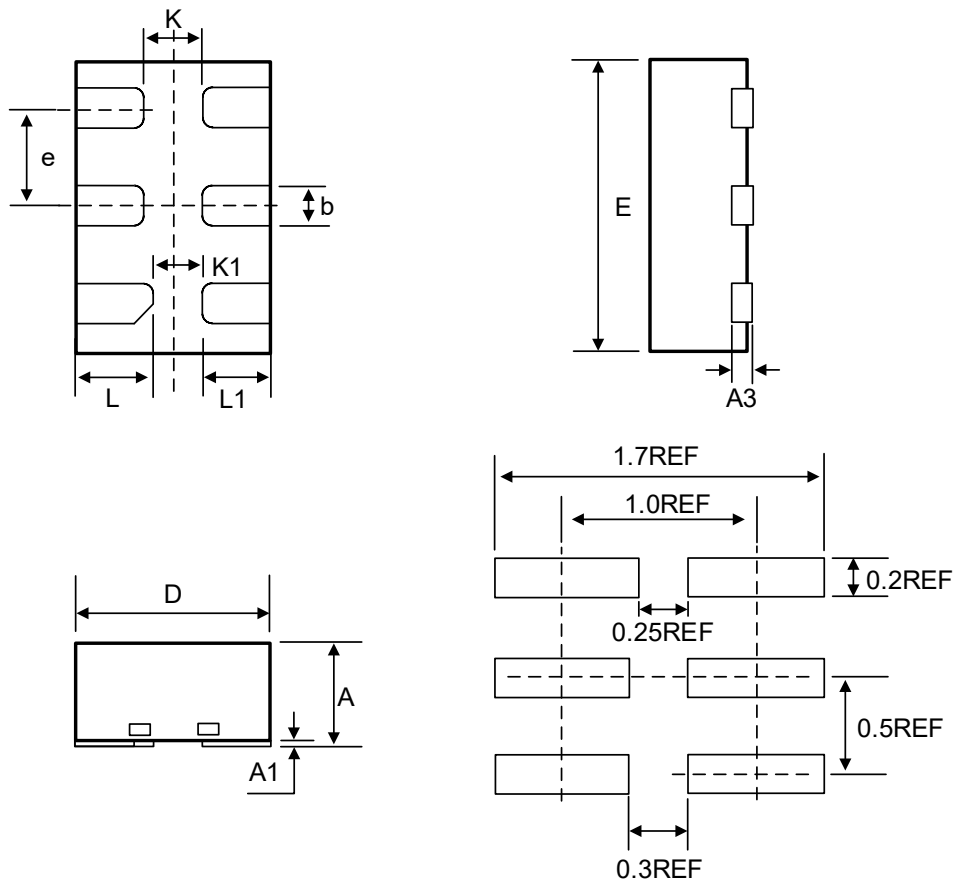
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0.00	-	0.15
b	0.28	0.35	0.50
c	0.08	0.15	0.22
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

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DFN6 (1.0mm × 1.5mm)



COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	0.50	--	0.60
A1	0.00	0.02	0.05
A3	0.10REF		
b	0.15	0.20	0.25
D	0.90	1.00	1.10
E	1.40	1.50	1.60
e	0.50BSC		
K	0.30REF		
K1	0.25REF		
L	0.35	0.40	0.45
L1	0.30	0.35	0.40

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Marking Information

G125X ET74AHC1G125 G125 = Part Number X = Tracking Number	1G125 XXXXX ET74AHC1G125T 1G125 = Part Number XXXXX = Tracking Number
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Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-09-06	Official Version	Wang anran	Yang xiaoxu	Liu jiaying
1.1	2026-04-17	Update Title, Format and Marking	Xu tao	Yang xiaoxu	Liu jiaying