

Low-Power Configurable Multiple Function Gate

General Description

The ET74AHC1G98 is a configurable multiple function gate with Schmitt trigger inputs. The device can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer; using the 3-bit input. All inputs can be connected to V_{CC} or GND.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in mixed 3.3V and 5V environments.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging back-flow current through the device when it is powered down.

Features

- Designed for 2V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- $\pm 8\text{mA}$ Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- ESD Protection Complies with JEDEC JESD22 Standard
 - HBM: $\pm 4000\text{V}$ Pass (JEDEC JS-001)
 - CDM: $\pm 1000\text{V}$ Pass (JEDEC JS-002)
- Latch-up Performance Exceeds $\pm 100\text{mA}$ per JEDEC JESD78F
- Part No. and Package Information

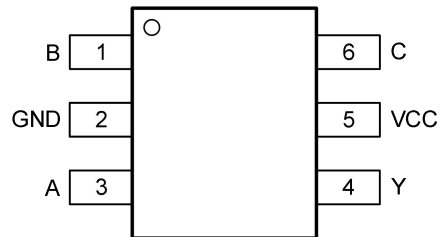
Part No.	Package	Packing Option	MSL
ET74AHC1G98	SC70-6 (1.3mm × 2.1mm)	Tape and Reel, 3K/Reel	3
ET74AHC1G98T	SOT23-6 (1.6mm × 2.9mm)	Tape and Reel, 3K/Reel	3

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Applications

- Active Noise Cancellation (ANC)
- Bar-code Scanners
- Blood Pressure Monitors
- CPAP Machines
- Cable Solutions
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- HVAC: Heating, Ventilating and Air Conditioning
- TVs: High-Definition (HDTV), LCD and Digital
- Video Communications Systems

Pin Configuration



SC70-6/SOT23-6

Figure1. Pin Configuration

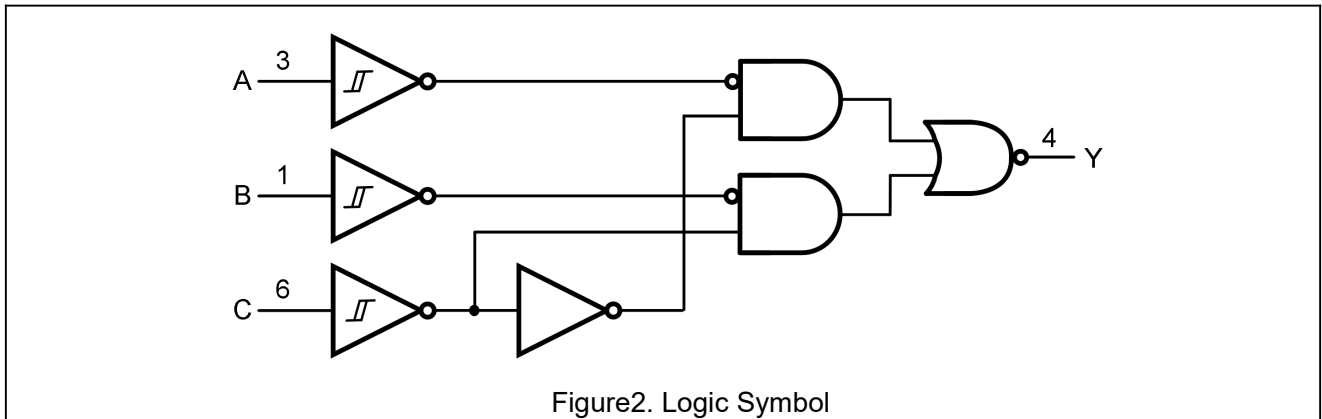
Pin Function

SC70-6/SOT23-6

Pin No.	Pin Name	Function
1	B	Input B
2	GND	Ground
3	A	Input A
4	Y	Output Y
5	VCC	Supply Voltage
6	C	Input C

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Block Diagram



Functional Table

Input			Output
C	B	A	Y
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

H = HIGH voltage level; L = LOW voltage level.

Function Selection Table

Logic function	Figure
2-input MUX with Inverted Output	See Figure3
2-input NAND	See Figure4
2-input NOR with One Input Inverted	See Figure5
2-input AND with One Input Inverted	See Figure5
2-input NAND with One Input Inverted	See Figure6
2-input OR with One Input Inverted	See Figure6
2-input NOR	See Figure7
Buffer	See Figure8
Inverter	See Figure9

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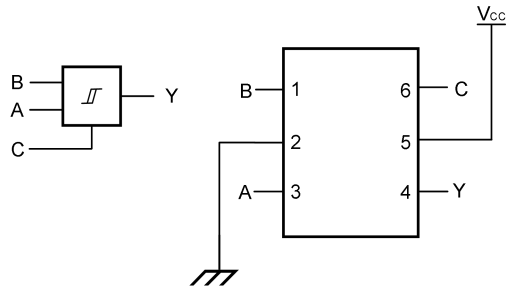


Figure3. 2-input MUX with inverted output

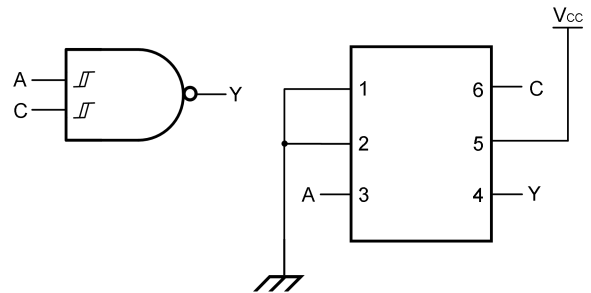


Figure4. 2-input NAND

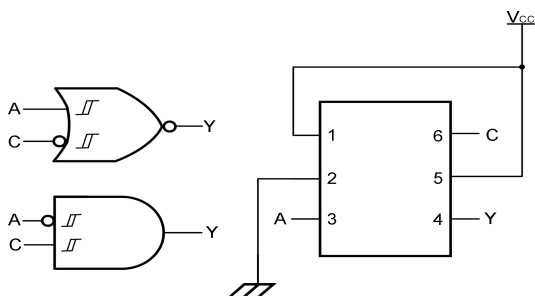


Figure5. 2-input AND gate with input A inverted or 2-input NOR gate with input C inverted

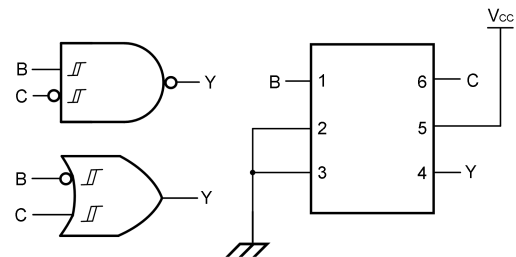


Figure6. 2-input OR gate with input B inverted or 2-input NAND gate with input C inverted

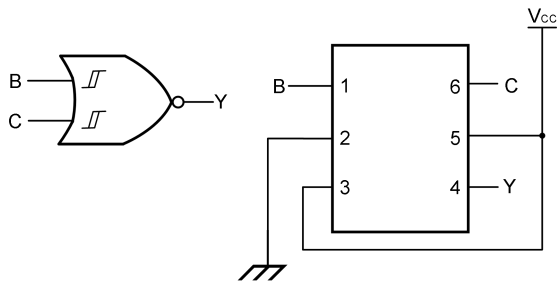


Figure7. 2-input NOR gate

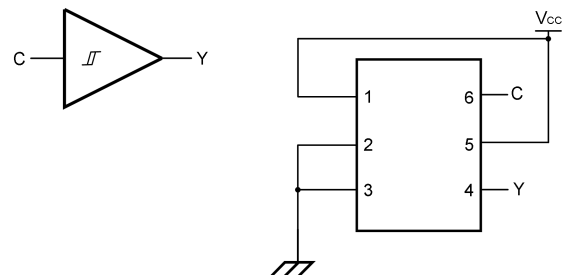


Figure8. Buffer

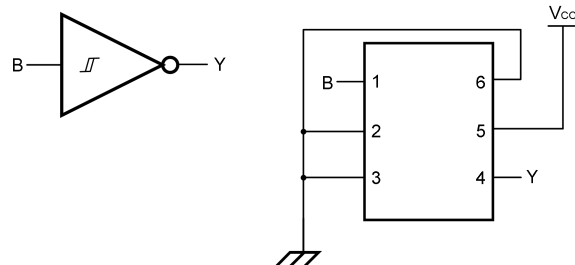


Figure9. Inverter

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Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 7.0	V
V _I	DC Input Voltage ⁽¹⁾		-0.5 ≤ V _I ≤ 7.0	V
V _O	DC Output Voltage Output in Higher or Low State		-0.5 to 7.0	V
I _{IK}	DC Input Diode Current, V _I < GND		-50	mA
I _{OK}	DC Output Diode Current, V _O < GND, V _O > V _{CC}		±50	mA
I _O	DC Output Sink Current		±50	mA
I _{CC}	DC Supply Current per Supply Pin		100	mA
I _{GND}	DC Ground Current per Supply Pin		-100	mA
T _{STG}	Storage Temperature Range		-65 to 150	°C
T _L	Lead Temperature, Soldering 10 Seconds		260	°C
T _J	Max Junction Temperature		150	°C
V _{ESD}	ESD Classification	Human Body Model ⁽²⁾	±4000	V
		Charged Device Model ⁽³⁾	±1000	
I _{LU}	Max Latch Up Current Above V _{CC} and GND at 125°C ⁽⁴⁾		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
R _{θJA}	SC70-6	Thermal Characteristics, Thermal Resistance, Junction-to-air	280	°C/W
	SOT23-6		180	
P _D	SC70-6	Power Dissipation in Still Air at 85°C	230	mW
	SOT23-6		360	

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage Operating	2	5.5	V
V _I	DC Input Voltage	0	V _{CC}	V
V _O	DC Output Voltage (High or Low State)	0	V _{CC}	V
T _A	Operating Temperature Range	-40	125	°C

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Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameters	Conditions	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{OL}	LOW - Level Output Voltage	V _I = V _{T+} or V _{T-}							
		I _{OL} = 100μA	2			0.1		0.1	V
		I _{OL} = 4mA	3			0.36		0.55	V
		I _{OL} = 8mA	5.5			0.36		0.55	V
V _{OH}	HIGH - Level Output Voltage	V _I = V _{T+} or V _{T-}							
		I _{OH} = -100μA	2	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V
		I _{OH} = -4mA	3	2.58			2.4		V
		I _{OH} = -8mA	5.5	3.54			3.7		V
I _I	Input Leakage Current	V _I = 5.5V or GND	0~5.5		±0.1	±1		±1	μA
I _{OFF}	Power-Off Leakage Current	V _I = 5.5V or V _O = 5.5V	0		±0.1	±2		±2	μA
I _{CC}	Supply Current	V _I = 5.5V or GND; I _O = 0mA	5.5		0.1	4		4	μA
ΔI _{CC}	Additional Supply Current	Per Pin: V _I = V _{CC} - 0.6V; I _O = 0mA	2.3~5.5		5	500		500	μA

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Electrical Characteristics (Continued)

AC Electrical Characteristics

$t_r = t_f = 3\text{ns}$, $R_L = 1\text{k}\Omega$

Symbol	Parameter	Condition	$V_{CC}(\text{V})$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PD}	Propagation Delay (Figure10 and 11)	$C_L = 15\text{pF}$	3~3.6		3.6	7.0	1	10.5	ns
		$C_L = 50\text{pF}$	3~3.6		4.1	8.0	1	11.8	
		$C_L = 15\text{pF}$	4.5~5.5		2.5	4.9	1	7.2	
		$C_L = 50\text{pF}$	4.5~5.5		3.0	5.7	1	7.8	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5\text{V}$, $V_I = 0\text{V}$ or V_{CC}	3	pF
C_{PD}	Power Dissipation Capacitance (5)	10MHz, $V_{CC} = 3.3\text{V}$, $V_I = 0\text{V}$ or V_{CC}	17	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

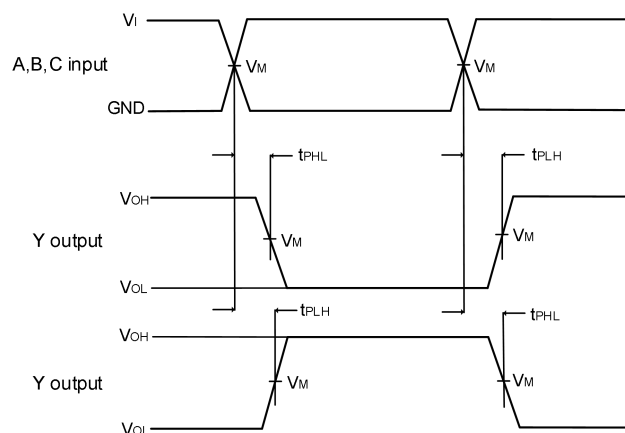
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Test Waveform



Measurement points are given in Table1.

V_{OL} and V_{OH} is typical output voltage levels that occur with the output load.

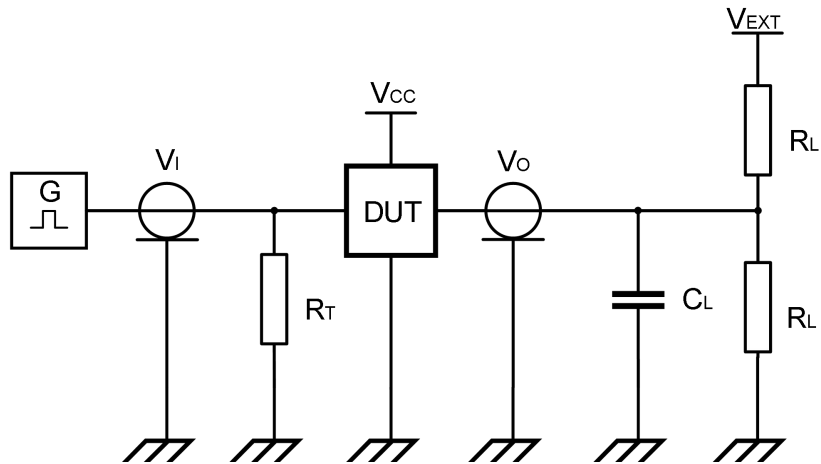
Figure10. Input A, B, C to Output xY Propagation Delay Times

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Table1. Measurement Points

Supply Voltage	Input	Output
V_{CC}	V_M	V_M
3.0V to 3.6V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
4.5V to 5.5V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

Test Circuit



Measurement points are given in [Table2](#).

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Figure11. Test Circuit for Measuring Switching Times

Table2. Test Data

Supply Voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
3.0V to 3.6V	V_{CC}	3.0ns	15pF, 50pF	1k Ω	OPEN
4.5V to 5.5V	V_{CC}	3.0ns	15pF, 50pF	1k Ω	OPEN

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Electrical Characteristics (Continued)

Transfer Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameters	Conditions	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	
V _{T+}	Positive-going Threshold Voltage	See Figure12, 13, 14, 15						
		V _{CC} = 2.0V	0.78		1.30	0.74	1.30	V
		V _{CC} = 2.3V	1.11		1.6	1.08	1.6	V
		V _{CC} = 3.0V	1.5		2	1.47	2	V
		V _{CC} = 4.5V	2.16		2.74	2.13	2.74	V
		V _{CC} = 5.5V	2.61		3.33	2.58	3.33	V
V _{T-}	Negative-going Threshold Voltage	See Figure12, 13, 14, 15						
		V _{CC} = 2.0V	0.35		0.80	0.35	0.83	V
		V _{CC} = 2.3V	0.58		1	0.58	1.03	V
		V _{CC} = 3.0V	0.8		1.3	0.8	1.33	V
		V _{CC} = 4.5V	1.21		1.9	1.21	1.93	V
		V _{CC} = 5.5V	1.45		2.29	1.45	2.32	V
V _H	Hysteresis Voltage	See Figure12, 13, 14, 15						
		V _{CC} = 2.0V	0.35		0.68	0.28	0.68	V
		V _{CC} = 2.3V	0.4		0.8	0.34	0.8	V
		V _{CC} = 3.0V	0.5		1	0.44	1	V
		V _{CC} = 4.5V	0.71		1.2	0.65	1.2	V
		V _{CC} = 5.5V	0.71		1.4	0.65	1.4	V

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Wave-forms Transfer Characteristics

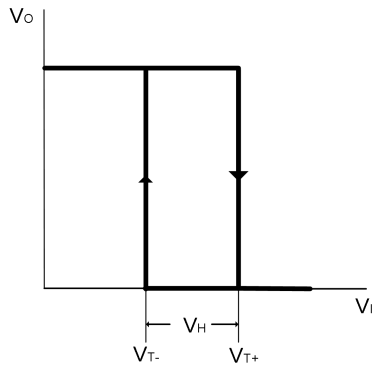
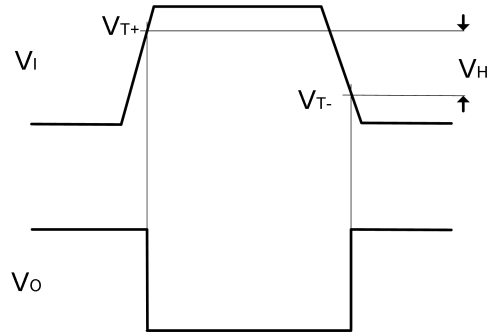


Figure12. Transfer characteristic



V_{T+} and V_{T-} limits are at 70% and 20%
Figure13. Definition of V_{T+} , V_{T-} and V_H

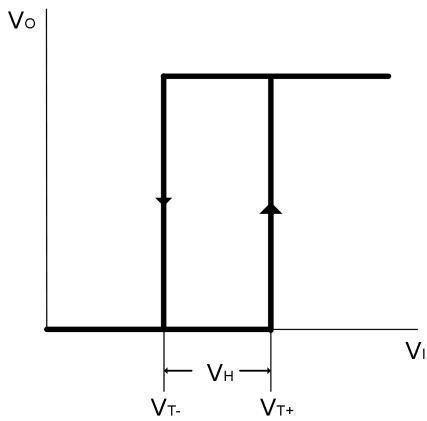
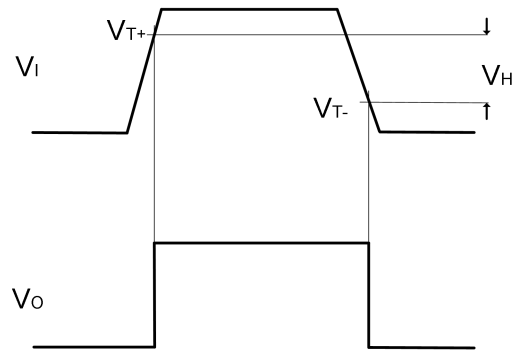


Figure14. Transfer characteristic



V_{T+} and V_{T-} limits are at 70% and 20%
Figure15. Definition of V_{T+} , V_{T-} and V_H

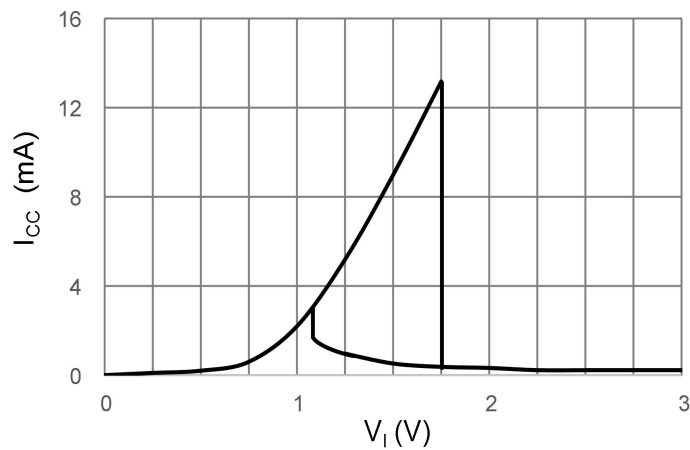


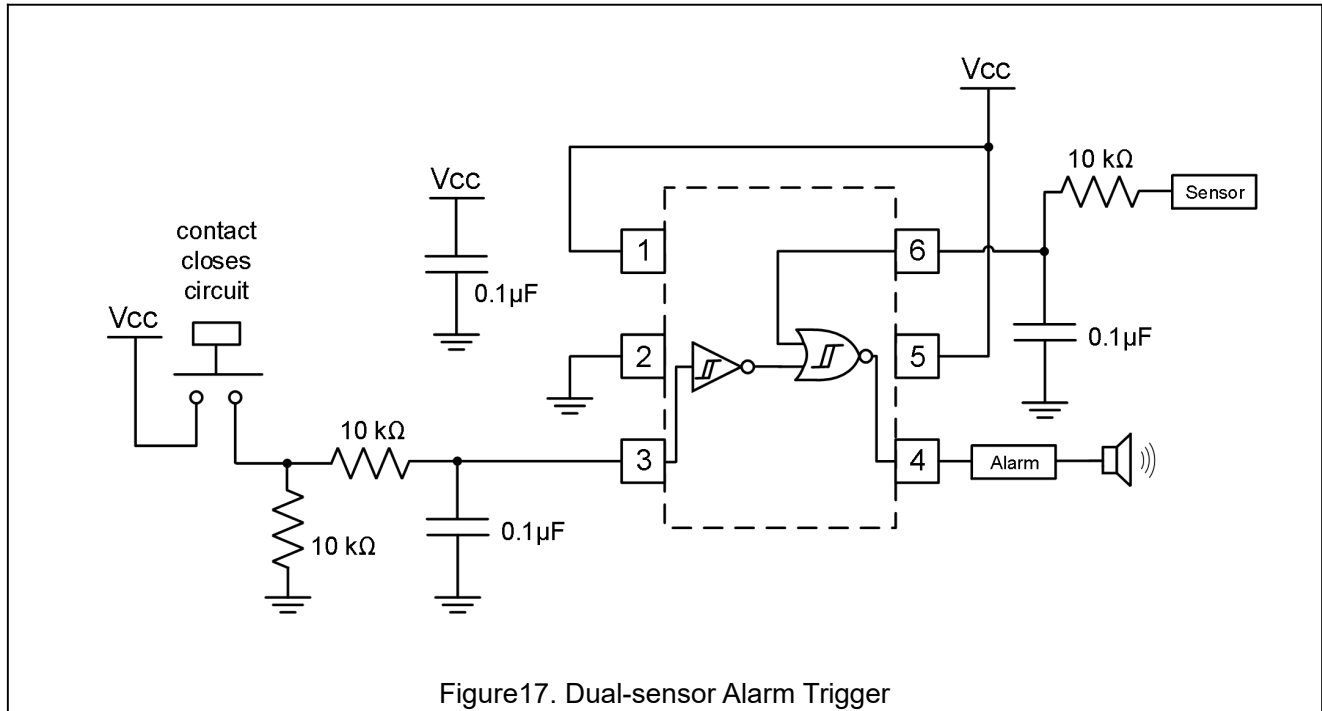
Figure16. Typical ET74AHC1G98 transfer characteristic; $V_{CC} = 3.0V$

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Application Circuits

This application shows the ET74AHC1G98 configured as an NOR gate with an inverted input. This particular configuration is helpful for dual sensor or switch applications where one of the inputs is normally closed or a logic high 1. Normally this application would require two external gates, but because the ET74AHC1G98 can be configured to meet this function the application can be implemented with a single chip solution.

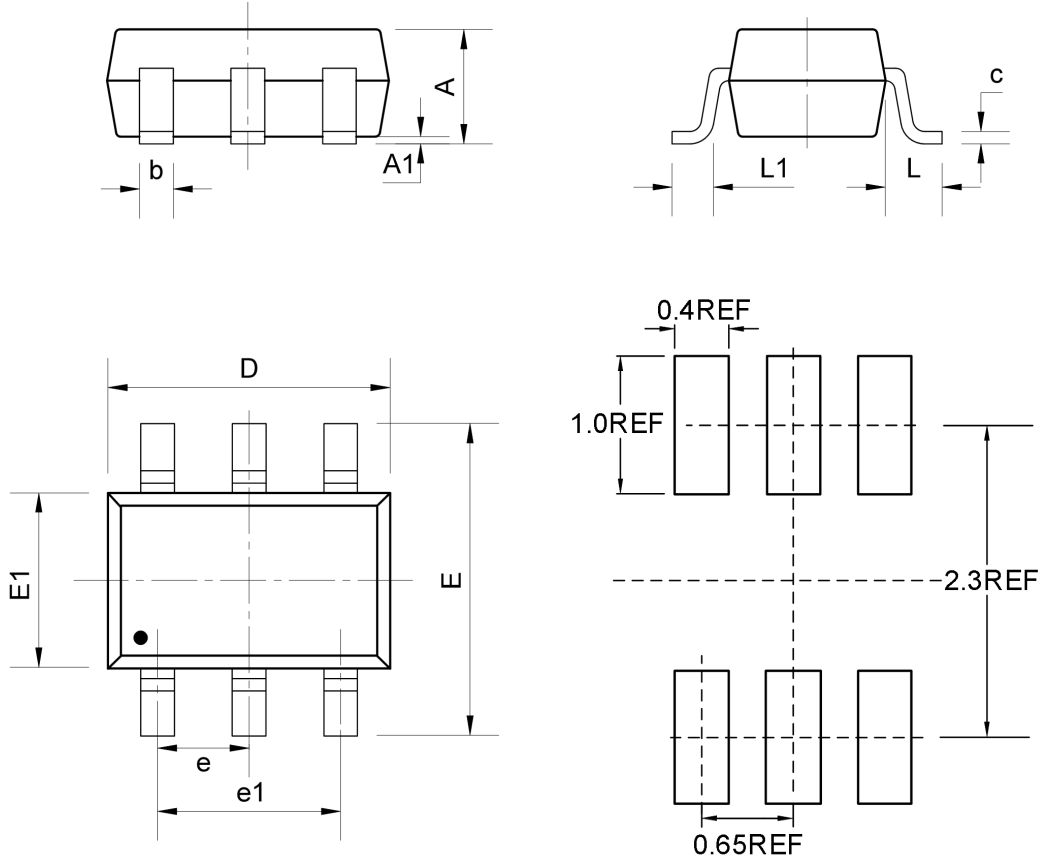
This application circuit is for reference only.



ET74AHC1G98

Package Dimension

SC70-6 (1.3mm × 2.1mm)



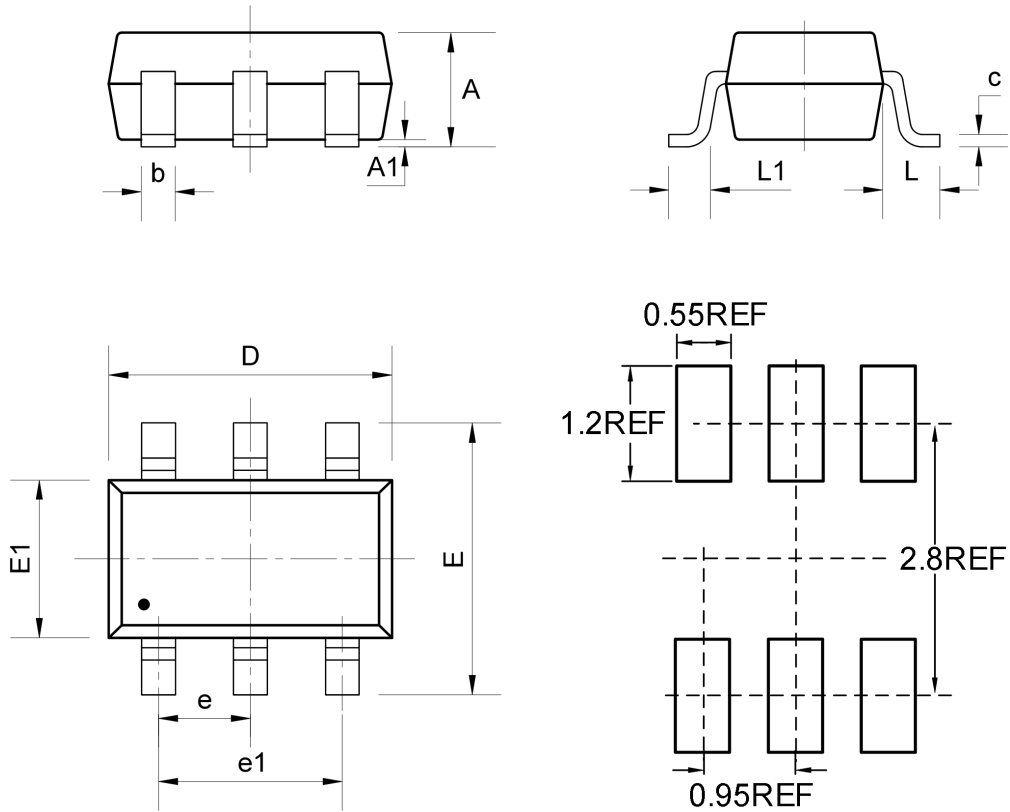
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
b	0.15	-	0.35
c	0.08	-	0.20
D	2.00	2.10	2.30
e	0.65BSC		
e1	1.30BSC		
E	2.15	2.30	2.50
E1	1.15	1.30	1.45
L	0.50REF		
L1	0.33REF		

ET74AHC1G98

SOT23-6 (1.6mm × 2.9mm)



COMMON DIMENSIONS

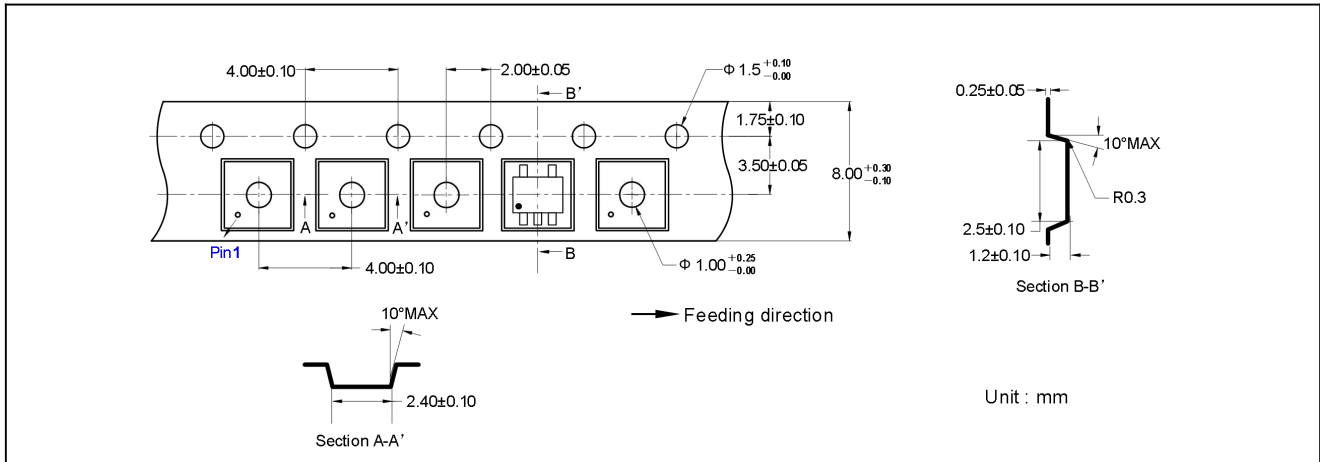
(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0.00	-	0.15
b	0.28	0.35	0.50
c	0.08	0.15	0.22
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

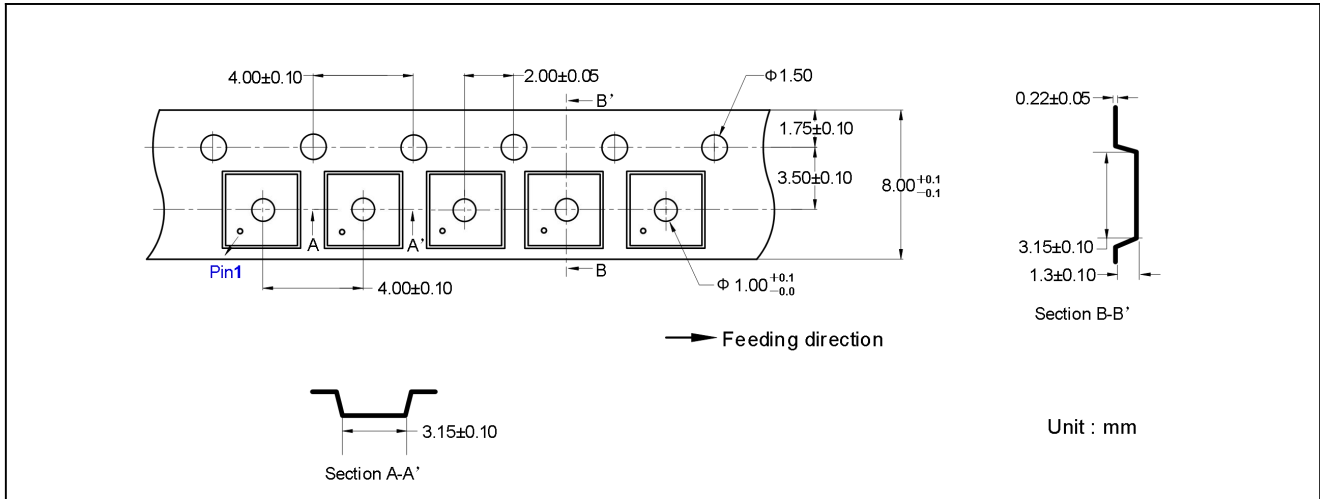
ET74AHC1G98

Tape Information

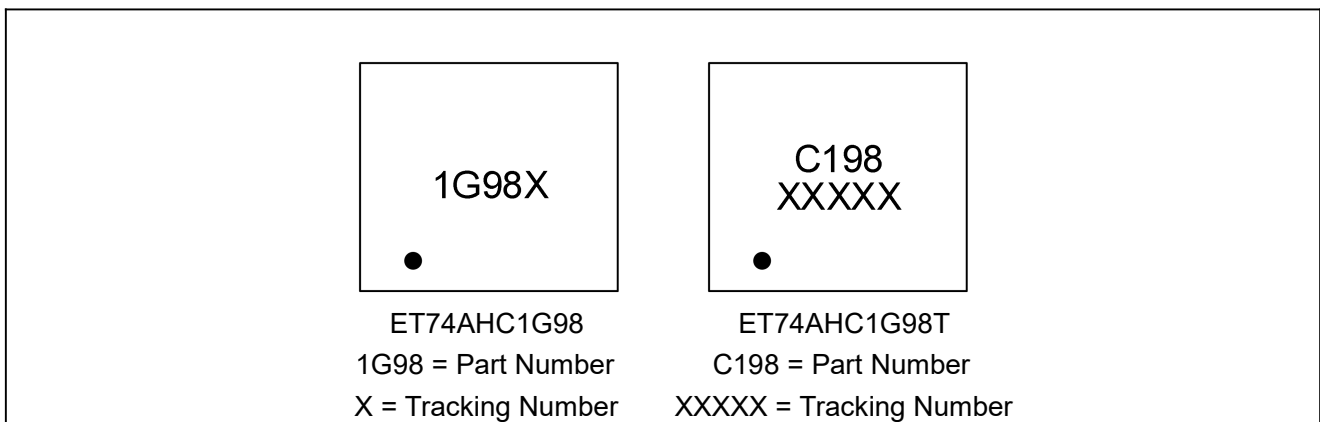
SC70-6 (1.3mm × 2.1mm)



SOT23-6 (1.6mm × 2.9mm)



Marking Information



ET74AHC1G98

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-11-19	Official Version	Xu tao	Yang xiaoxu	Liu jiaying