1A, High PSRR, Low Dropout LDO

General Description

The ETQ5A7ADJY1 is a 1A low−dropout linear regulators (LDOs) offering high power−supply ripple rejection (PSRR) and Power Good open collector output. This LDO uses an advanced BiCMOS process to achieve very good electrical performance. It is an ideal choice for noise sensitive Analog RF Front−Ends used in Telecom Equipment.

The ETQ5A7ADJY1 is available in the DFN8 (3mm x 3mm) package.

Features

- Wide Input Voltage Range: 2.2V ~ 5.5V
- Output Voltage Range: 0.8V ~ 5.0V (adjustable)
- Ground Pin Current: 60μA (Typ) at 0.1mA
- Low Dropout: 160mV (Typ) at 1A, V_{OUT} = 3.3V
- Built-in Current Limiting and Thermal Shutdown Circuit
- Built-in Under Voltage Lock-out
- Automotive AEC-Q100 Grade 1 Qualified

  -- Ambient Temperature Range of -40°C to +125°C

  -- ESD HBM 4kV PASS, Tested Per AEC-Q100-002(JEDEC JS-001)

  -- ESD CDM 1.5kV PASS, Tested Per AEC-Q100-011(JEDEC JS-002)
- Part No. and Package Information

Part No.	Package	MSL
ETQ5A7ADJY1	DFN8 (3mm x 3mm)	Level 1

Applications

- Telecom Infrastructure
- Automotive Infotainment Systems
- High−Speed I/F (PLL/VCO)

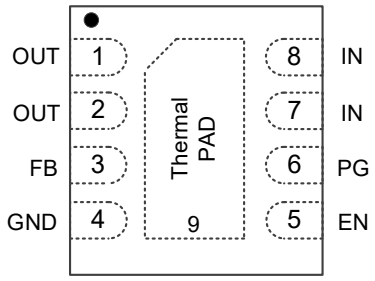
ETQ5A7ADJY1

Device information

ETQ 5A7 ADJ Y1

ADJ Output Voltage		**Y1 Package**	
ADJ	Adjust Output	Y1	DFN8 (3mm x 3mm)

Pin Configuration



ETQ5A7ADJY1

Figure1. Top View

Pin Function

Pin No.	Pin Name	Pin Function
1,2	OUT	The Power Output of The Device.
3	FB	Adjustable Output Feedback Pin.
4	GND	Ground Pin.
5	EN	Enable Input. Driving EN high turns on the regulator. Driving EN low turns off the regulator. This pin must be pulled high by an external resistor connected to IN pin if EN pin is not used.
6	PG	Power Good, Open Collector. Use 10 kΩ to 100 kΩ pull−up resistor connected to output or input voltage.
7,8	IN	Input Voltage Pin. Large bulk capacitance should be placed closely to this pin. A 4.7μF ceramic capacitor is recommended at this pin.
9	Thermal Pad	Thermal Pad. Connect to GND plane for better power dissipation.

Block Diagram

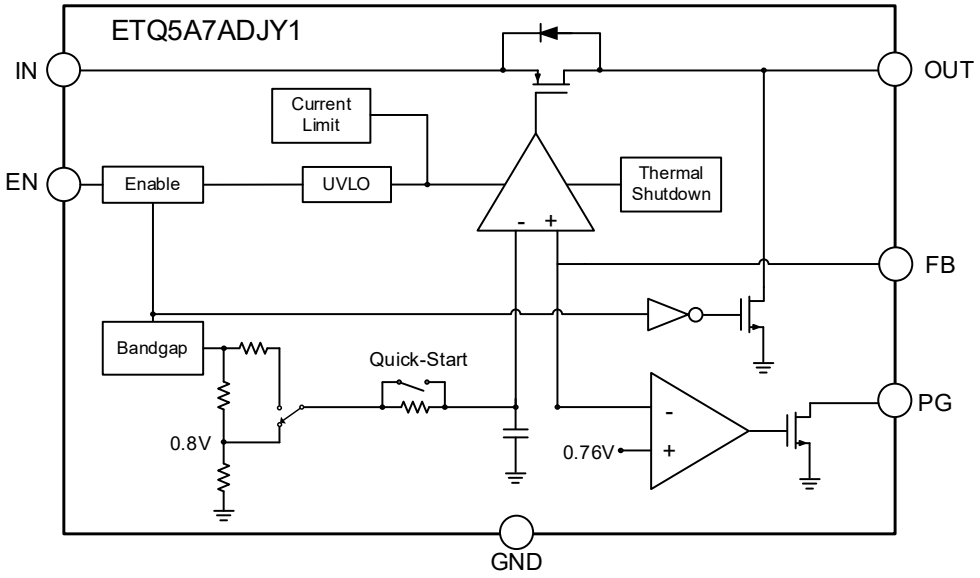


Figure2. ETQ5A7ADJY1 Block diagram

Functional Description

The ETQ5A7ADJY1 is the member of new family of high output current and low dropout regulators which delivers low quiescent and ground current consumption, good noise and power supply ripple rejection ratio performance. The ETQ5A7ADJY1 incorporates EN pin and power good output for simple controlling by MCU or logic. Standard features include current limiting, soft−start feature and thermal protection.

Capacitors Selection

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1 μF to 1.0 μF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. The ETQ5A7ADJY1 is designed to be stable with standard ceramic output capacitors of capacitance values 4.7 μF up to 10 μF.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool down. When the junction temperature reduces to approximately +140°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Power Dissipation

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C.

Under-Voltage Lock-Out (UVLO)

The ETQ5A7ADJY1 uses an under-voltage lock-out circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that it typically ignores undershoot transients on the input if they are less than 50μs duration.

Enable Pin Operation

The ETQ5A7ADJY1 is turned on by setting the EN pin to “H”. The threshold limits are covered in the electrical characteristics table in this datasheet. When the EN pin is not used, connect the EN pin with IN to keep the LDO in operating mode.

Input Power Supply

The input power supply range is from 2.2V to 5.5V. VIN must be larger than (V_{OUT} + V_{DROP}) in application. The input ceramic capacitor must be placed as close as possible to the IN pin, this C_{IN} can help improve the output noise performance of LDO.

Current Limit Protection

When output current of OUT pin is higher than current limit threshold or the OUT pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

Output Voltage Setting

The required output voltage of Adjustable devices can be adjusted from V_{REF} to 5 V using two external resistors. Typical application schematics is shown blow.

$$\mathbf{V_{OUT} = V_{REF} * (1 + R1 / R2)}$$

Typical value of V_{REF} is 0.8V. It is recommended to keep the total serial resistance of resistors (R1 + R2) no greater than 100 kΩ.

The output voltage needs to take into account the error caused by the resistance accuracy.

Power Good Output Connection

The ETQ5A7ADJ has a power-good function that works by toggling the state of the PG output pin. When the output voltage falls below the PG threshold voltage, the PG pin open-drain output engages (low impedance to GND). When the output voltage exceeds the PG threshold voltage by an amount greater than VHYS (PG), the PG pin becomes high-impedance. By connecting a pull-up resistor to an external supply, any downstream device can receive PG as a logic signal. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices.

Absolute Maximum Ratings

Symbol	Parameters (Items)	Value	Unit
V_{IN}	Input Voltage (IN Pin)(1)	-0.3 to 6.0	V
V_{EN}	Input Voltage (EN Pin)	-0.3 to 6.0	V
V_{FB}	Feedback Voltage (FB Pin)	-0.3 to 6.0	V
V_{PG}	Power Good Voltage (PG Pin)	-0.3 to 6.0	V
V_{OUT}	Output Voltage (OUT Pin)	-0.3 to (V_{IN}+0.3) ≤6.0	V
I_{MAX}	Maximum Load Current	Internally Limited	mA
P_{D_MAX}	Maximum Power Consumption	2000	mW
T_J(2)	Operating Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	°C
T_{SLOD}	Lead Temperature (Soldering, 10 sec)	300	°C
V_{ESD}(3)	HBM Capability	±4000	V
	CDM Capability	±1500	V
I_{LU}(3)	Latch up Current Maximum Rating	±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: Refer to Electrical Characteristics and Application Information for Safe Operating Area and IN port needs to be powered on before the EN port.

Note2: When T_J > 125°C, there will be a large deviation in voltage accuracy.

Note3: This device series incorporates ESD protection and is tested by the following methods:

HBM tested per AEC-Q100-002(JEDEC JS-001).

CDM tested per AEC-Q100-011(JEDEC JS-002).

Latch up Current Maximum Rating tested per AEC-Q100-004(JEDEC JESD78F).

Recommended Operating Conditions

Symbol	Parameters	Rating	Unit
V_{IN}	Input Voltage	2.2 to 5.5	V
V_{OUT}	Output Voltage	0.8 to 5.0	V
I_{OUT}	Output Current	0 to 1000	mA
T_A	Operating Ambient Temperature	-40 to 125	ºC
C_{IN}	Effective Input Ceramic Capacitor Value	0.1 to 1	μF
C_{OUT}	Effective Output Ceramic Capacitor Value	4.7 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

Electrical Characteristics

(Unless otherwise noted, V_{IN} = V_{OUT} + 0.5V or 2.2V(whichever is greater), V_{EN} = 2.2V, I_{OUT} = 1mA, C_{IN} = 1μF, C_{OUT} = 4.7μF. For ADJ version, tested at V_{OUT} = 0.8V and V_{OUT} = 5V. T_J = -40ºC to +125ºC, typical values are at T_A = +25ºC)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IN}[4]	Input Voltage Range		2.2		5.5	V
V_{UVLO}	Under-voltage Lock-out	V_{IN} Rising, RL = 1kΩ	1.86	2	2.1	V
V_{UVLO_H}		Hysteresis, V_{IN} Falling, R_L = 1kΩ		75		mV
V_{OUT}[5]	V_{OUT} Voltage Accuracy	Output Voltage Range	0.8		5	V
		V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V, V_{IN} ≥ 2.2V, 1 mA ≤ I_{OUT} ≤1A, T_A = 25ºC	-0.3		0.3	%
		V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V, V_{IN} ≥ 2.2V, 1 mA ≤ I_{OUT} ≤1A, -40ºC ≤ T_J ≤ 125ºC	-2.5		2.5	%
Reg_{LINE}	Line Regulation	$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, V_{IN} ≥ 2.2V, I_{OUT} = 1mA		0.0045	0.05	%/V
Reg_{LOAD}	Load Regulation	1mA ≤ I_{OUT} ≤ 1A, V_{OUT}=3.3V		2	10	mV
V_{DROP}[6]	Dropout Voltage	$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, V_{IN} ≥ 2.2V, I_{OUT} = 500mA		80	120	mV
		$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, V_{IN} ≥ 2.2V, I_{OUT} = 750mA		120	180	
		$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, V_{IN} ≥ 2.2V, I_{OUT} = 1A		160	240	
I_{LIMIT}	Current Limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$, V_{IN} ≥ 3.3V		1600	2600	mA
I_{GND}	Ground Pin Current	I_{OUT} = 0.1mA		60	100	μA
		I_{OUT} = 1A		300	500	μA
I_{SHDN}	Shutdown Current	V_{EN} ≤ 0.4V, V_{IN} ≥ 2.2V, R_L = 1kΩ, -40ºC ≤ T_J ≤ 125ºC		0.2	2	μA
I_{FB}	FB Pin Current	V_{IN} = 5.5V, V_{FB} = 0.8V		0.02	1	μA
PSRR[7]	Power Supply Rejection Ratio	V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 750mA, f = 100Hz		77		dB
		V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 750mA, f = 1kHz		63		
		V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 750mA, f = 1MHz		27		
e_N[7]	Output Noise	V_{IN}= 4.3V, V_{OUT}= 3.3V, f= 100Hz to 100kHz, I_{OUT} = 100mA		15*V_{OUT}		μV_{RMS}
I_{EN}	Enable Input Current	V_{IN} = V_{EN} = 5.5V		0.27	1	μA

Electrical Characteristics(Continued)

(Unless otherwise noted, V_{IN} = V_{OUT} + 0.5V or 2.2V(whichever is greater), V_{EN} = 2.2V, I_{OUT} = 1mA, C_{IN} = 1μF, C_{OUT} = 4.7μF. For ADJ version, tested at V_{OUT} = 0.8V and V_{OUT} = 5V. T_J = -40ºC to +125ºC, typical values are at T_A = +25ºC)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{PGUP}[7]	Power Good Threshold Voltage	Output Voltage Raising		95		%
V_{PGDW}[7]		Output Voltage Falling		90		
V_{PGLO}	Power Good Output Voltage Low	I_{PG} = 1mA, Open Drain		30	100	mV
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage High	1.2			V
V_{ENL}		EN Input Voltage Low			0.4	
T_{ON}	Turn-On Time	V_{OUT} = 3.3V, R_L = 1kΩ, From EN = HIGH to V_{OUT}= 90% $V_{OUT(MON)}$		350		μs
T_{TSD}[7]	Thermal Shutdown Threshold	T_J Rising		160		ºC
T_{HYS}[7]	Thermal Shutdown Hysteresis	T_J Falling from Shutdown		30		ºC

Note4: Minimum V_{IN} = V_{OUT} + V_{DO} ≥ 2.2 V.

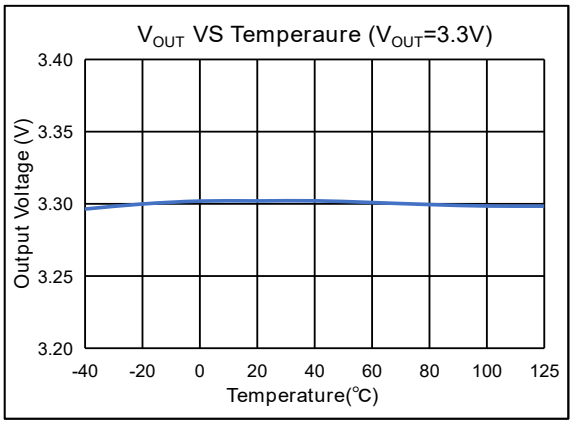
Note5: The ETQ5A7ADJY1 does not include external resistor tolerances and it is not tested at this condition: V_{OUT} = 0.8 V, 4.5V≤ V_{IN} = 5.5 V, and 750 mA ≤ I_{OUT} ≤ 1 A, because the power dissipation is greater than the maximum rating of the package.

Note6: V_{DROP} is not measured for fixed output voltage devices with V_{OUT} < 1.7 V because minimum V_{IN} = 2.2 V. V_{DROP} FT test method: test the V_{OUT} voltage at V_{set} + $V_{DROPMAX}$ with output current.

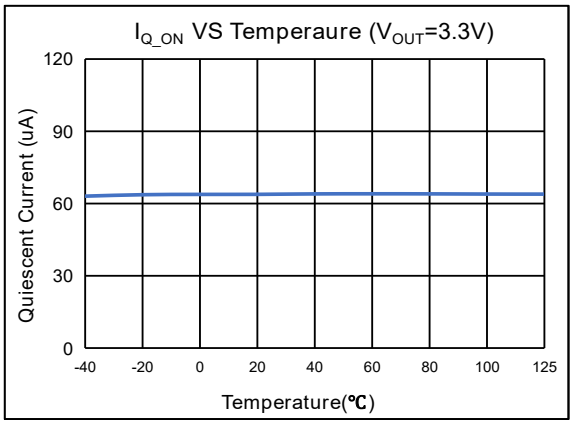
Note7: Guaranteed by design and characterization. not a FT item.

Typical Characteristics

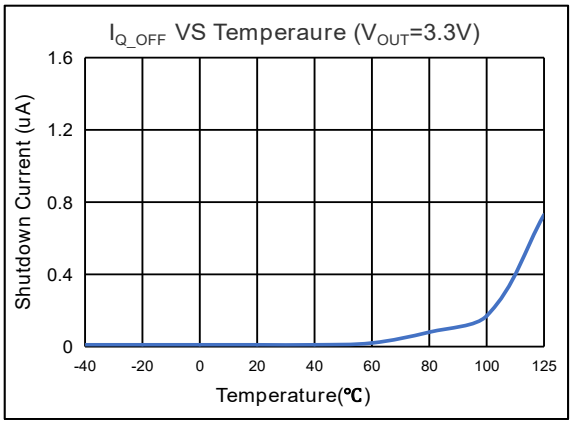
Voltage set 3.3V (V_{IN} = V_{OUT} + 0.5V, V_{EN} = 2.2V, I_{OUT} = 1mA, R1 = 312.5kΩ, R2 = 100kΩ, I_{OUT} = 1mA, C_{IN} = 1μF, C_{OUT} = 4.7μF, unless otherwise noted. Typical values are at T_A = +25°C).



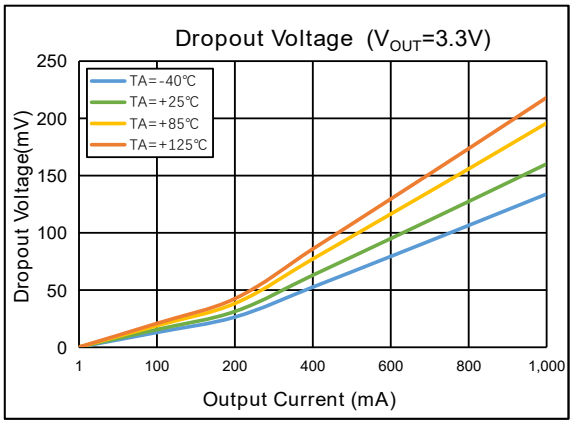
Output Voltage VS Temperature



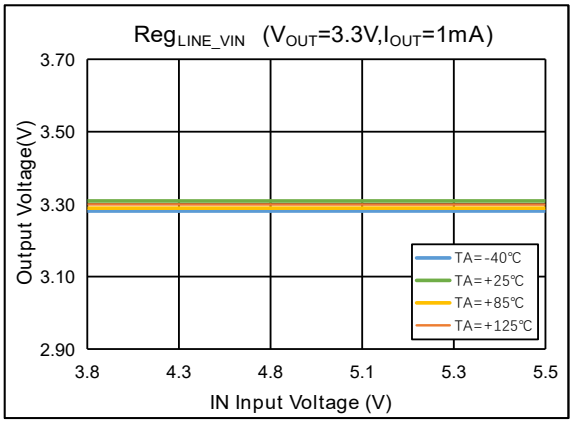
Quiescent Current VS Temperature



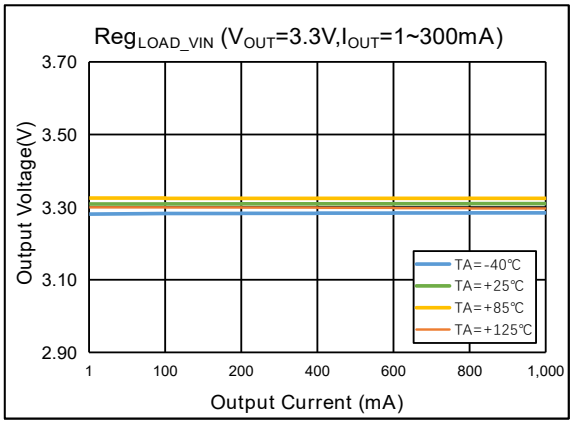
Standby Current VS Temperature



Dropout Voltage VS Output Current



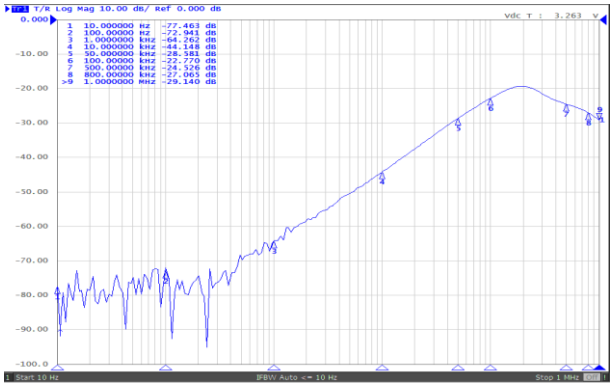
Output Voltage VS Input Voltage



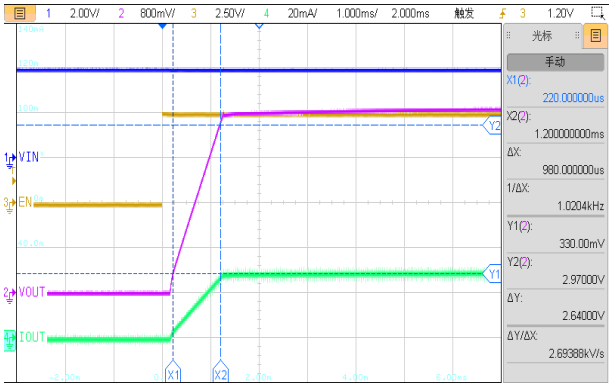
Output Voltage VS Output Current

Typical Characteristics (Continued)

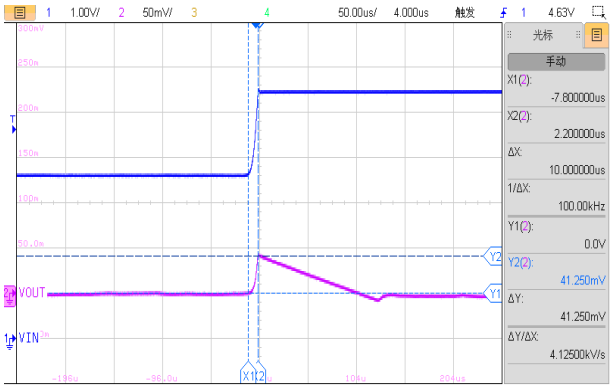
Voltage set 3.3V (V_{IN} = V_{OUT} + 0.5V, V_{EN} = 2.2V, I_{OUT} = 1mA, R1 = 312.5kΩ, R2 = 100kΩ, I_{OUT} = 1mA, C_{IN} = 1μF, C_{OUT} = 4.7μF, unless otherwise noted. Typical values are at T_A = +25°C).



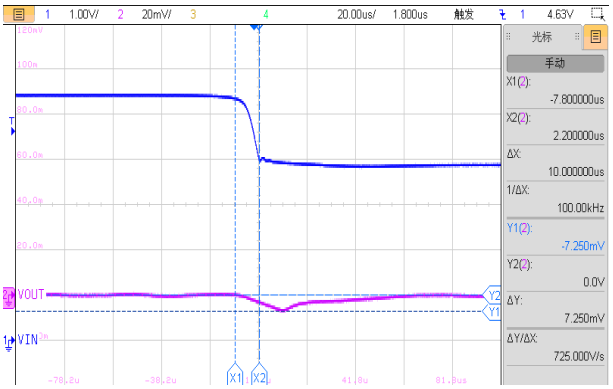
PSRR (I_{OUT} = 750mA)



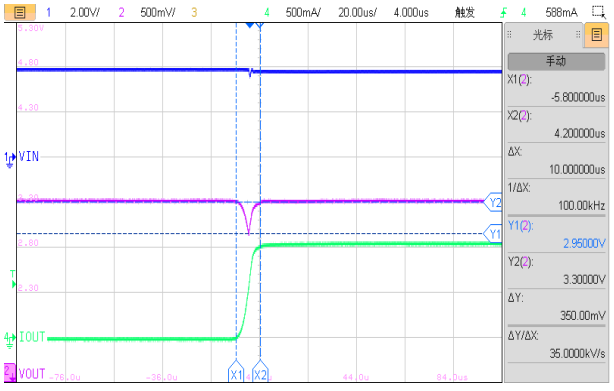
T_{ON} (I_{OUT} = 30mA)



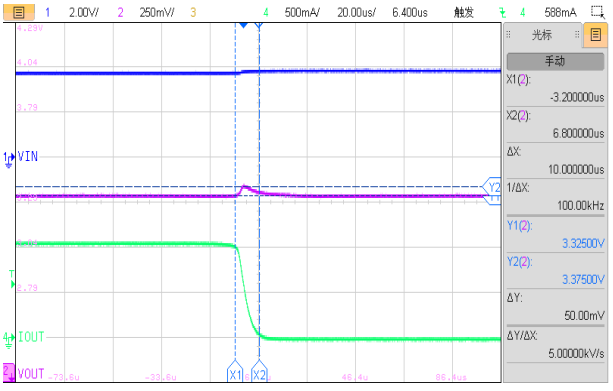
Input-Transient (3.8~5.5V, tr = 10μs, I_{OUT} = 1mA)



Input-Transient (5.5~3.8V, tf = 10μs, I_{OUT} = 1mA)



Load-Transient (V_{IN} = 3.8V, I_{OUT} = 1~1000mA, tr =10μs)



Load-Transient (V_{IN} = 3.8V, I_{OUT} = 1000~1mA, tf =10μs)

Application Circuit

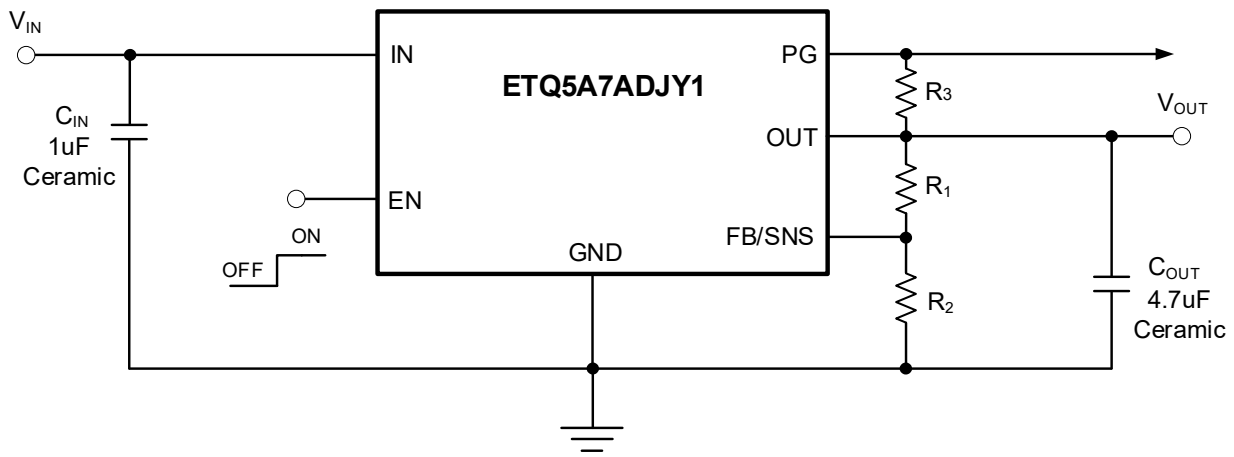


Figure3. Application circuit[8]

Note8: 1): V_{OUT} = 0.8*(1+R1/R2), (R1+R2) no greater than 100kΩ.

R3: Use a pull-up resister from 10kΩ to 100kΩ for the best.

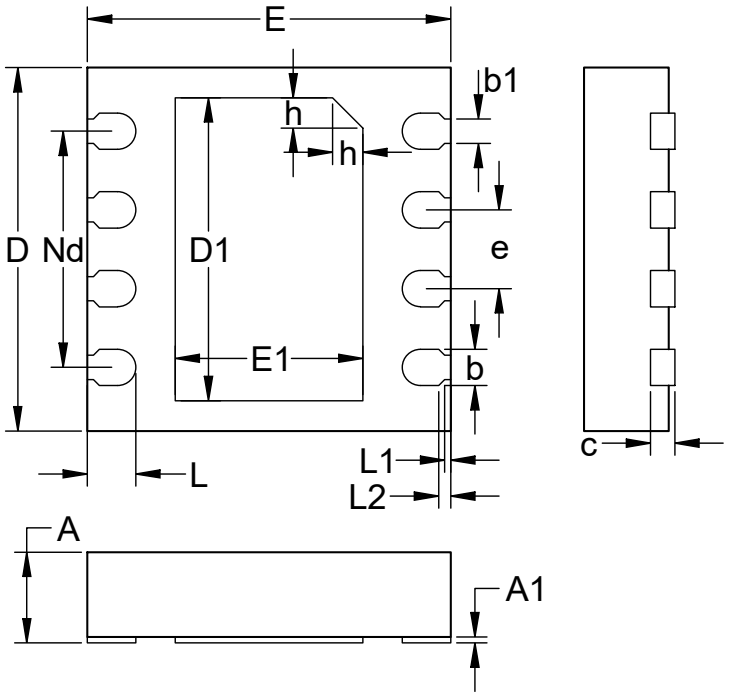
2): Recommended Capacitor Values: C_{IN} = 1μF, C_{OUT} = 4.7μF.

3): Recommended Feedback Resistor Values for Common Output Voltages.

V_{OUT}(V)	R1(KΩ)	R2(KΩ)
0.8	0	10
1	2.5	10
1.2	5	10
1.5	8.9	10
1.8	12.5	10
2.5	21	10
3.3	31	10
5	52.3	10

Package Dimension

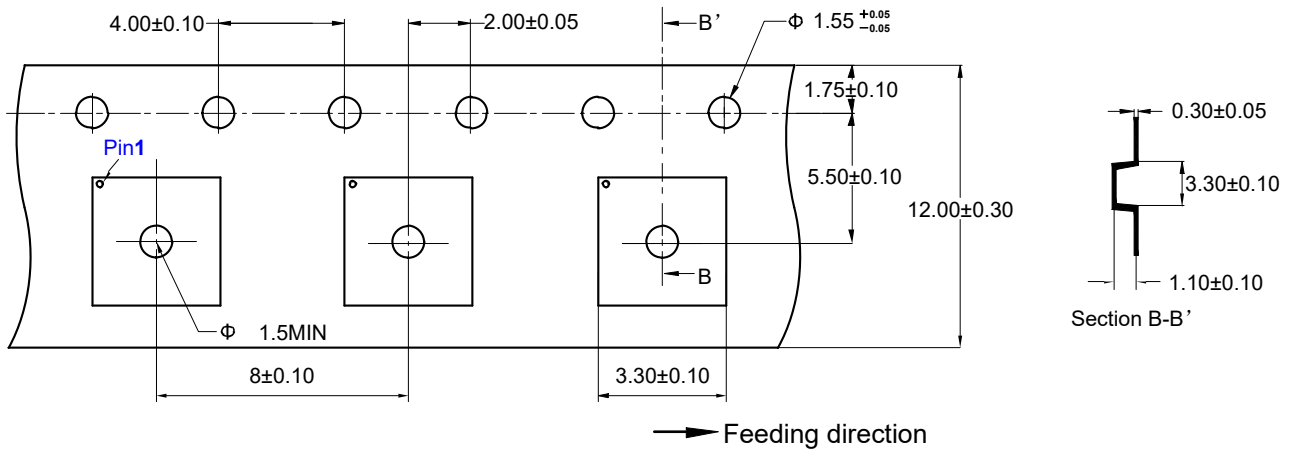
DFN8 (3mm x 3mm)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	-	0.95
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
b1		0.20REF	
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D1	2.40	2.50	2.60
e		0.65BSC	
Nd		1.95BSC	
E	2.90	3.00	3.10
E1	1.45	1.55	1.65
L	0.30	0.40	0.50
L1		0.05REF	
L2		0.10REF	
h	0.20	0.25	0.30

Tape Information



Marking

5A7O1 = Part Number
XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-12-25	Preliminary Version	Xut	Tugz	Liuyg
0.1	2025-04-18	Update Electrical Characteristics & Typical Characteristics	Pengjj	Tugz	Liuyg
1.0	2026-03-11	Official Version	Yangxx	Yangxx	Liuyg