4 Bit 100 Mbps Configurable Level Translator

General Description

The ET5014L is a 4-bit bidirectional level translator in which the input and output ports are switched automatically without direction control. The data path of each channel can be either from I/O_V_Ln to I/O_V_{CC}n or from I/O_V_{CC}n to I/O_V_Ln. All of the I/O ports are designed to track two different power supply rails, V_{CC} and V_L respectively. Both of the supply voltage are configurable from 1.08V to 5.0V. The V_{CC} and V_L supplies are independent which allows a logic signal on the V_L side to be translated to either a higher or a lower logic signal voltage on the V_{CC} side, and vice-versa.

The ET5014L has high output current capability, which allows the translator to drive high capacitive loads such as most high frequency EMI filters. The enable pin (EN) is used to reduce the power consumption. The EN pin can be used to disable both I/O ports by putting them in 3-state which significantly reduces the supply current from both V_{CC} and V_L. The EN signal is referenced to the V_L supply.

Features

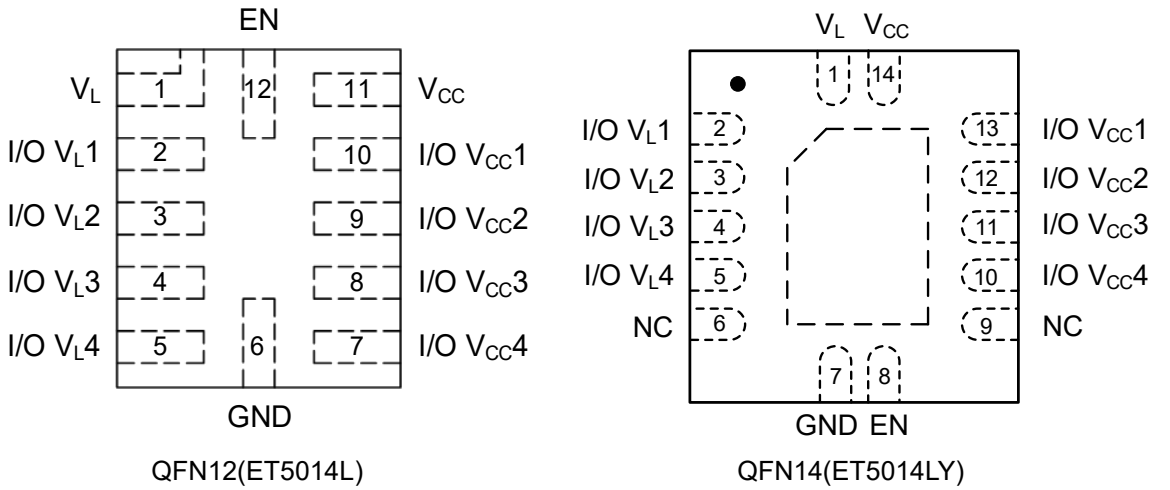
- Wide V_{CC}, V_L Operating Range: 1.08V to 5.0V
- V_L and V_{CC} are Independent
- V_L may be Greater than, Equal to, or Less than V_{CC}
- High 50pF Capacitive Drive Capability
- High-Speed with 100 Mbps Guaranteed Date Rate for V_{CC}, V_L > 1.8V
- Low Bit-to-Bit Skew
- Over-voltage Tolerant Enable and I/O Pins
- Non-preferential Power Up Sequencing
- Power-off Protection
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET5014L	QFN12 (1.7mm × 2.0mm)	Tape and Reel, 3K/Reel	1
ET5014LY	QFN14 (2.5mm × 3.0mm)	Tape and Reel, 3K/Reel	1

Application

- Infotainment and Cluster
- Pad Devices

Pin Configuration



Top View

Figure 1. Pin Configuration

Pin Function

Pin No.		Pin Name	Description
QFN12	QFN14		
11	14	V_{CC}	V_{CC} Input Voltage
1	1	V_L	V_L Input Voltage
6	7	GND	Ground
12	8	EN	Output Enable
7~10	10~13	I/O V_{CC}4～I/O V_{CC}1	I/O Port, Referenced to V_{CC}
2~5	2~5	I/O V_L1～I/O V_L4	I/O Port, Referenced to V_L
-	6,9	NC	Not Connected

Block Diagram

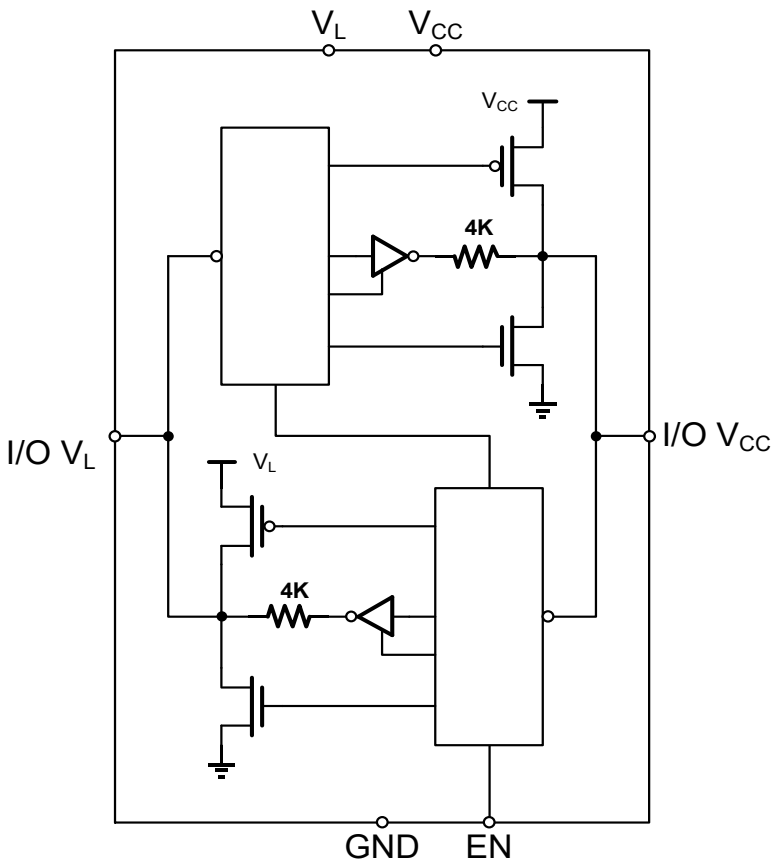


Figure 2. Simplified Functional Diagram (1 channel)

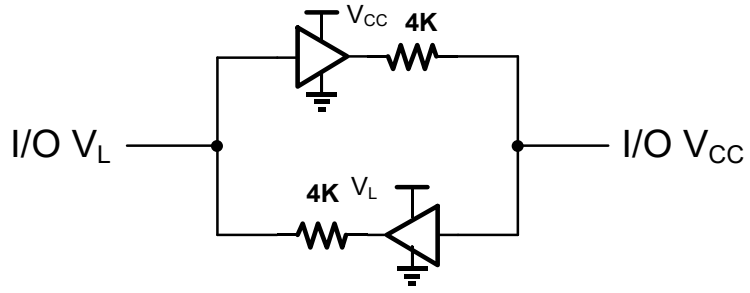


Figure 3. Logic Diagram (1 channel)

Function Description

The ET5014L auto-sense translator provides bi-directional logic voltage level shifting to transfer data in multiple supply voltage systems. These level translators have two supply voltages, V_L and V_{CC}, which set the logic levels on the input and output sides of the translator. When used to transfer data from the I/O V_L to the I/O V_{CC} ports, input signals referenced to the V_L supply are translated to output signals with a logic level matched to V_{CC}. In a similar manner, the I/O V_{CC} to I/O V_L translation shifts input signals with a logic level compatible to V_{CC} to an output signal matched to V_L.

The ET5014L translator consists of bi-directional channels that independently determine the direction of the data flow without requiring a directional pin. One-shot circuits are used to detect the rising or falling input signals. In addition, the one-shots decrease the rise and fall times of the output signal for high-to-low and low-to-high transitions.

Auto-sense translators such as the ET5014L have a wide bandwidth, but a relatively small DC output current rating. The high bandwidth of the bi-directional I/O circuit is used to quickly transform from an input to an output driver and vice versa. The I/O ports have a modest DC current output specification so that the output driver can be over driven when data is sent in the opposite direction. For proper operation, the input driver to the auto-sense translator should be capable of driving 2mA of peak output current. The bi-directional configuration of the translator results in both input stages being active for a very short time period. Although the peak current from the input signal circuit is relatively large, the average current is small and consistent with a standard CMOS input stage.

The ET5014L translator has an Enable pin (EN) that provides tri-state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CC} and I/O VL pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_L supply and has Over-Voltage Tolerant (OVT) protection.

The ET5014L translator can function as a non-inverting uni-directional translator. One advantage of using the translator as a uni-directional device is that each I/O pin can be configured as either an input or output. The configurable input or output feature is especially useful in applications such as SPI that use multiple uni-directional I/O lines to send data to and from a device. The flexible I/O port of the auto sense translator simplifies the trace connections on the PCB.

The values of the V_L and V_{CC} supplies can be set to anywhere between 1.08V and 5.0V. Design flexibility is maximized because V_L may be either greater than or less than the V_{CC} supply. In contrast, the majority of the competitive auto sense translators has a restriction that the value of the V_L supply must be equal to less than (V_{CC} - 0.4) V.

The sequencing of the power supplies will not damage the device during power-up operation. In addition, the I/O V_{CC} and I/O V_L pins are in the high impedance state if either supply voltage is equal to 0V. For optimal performance, 0.01uF to 0.1uF decoupling capacitors should be used on the V_L and V_{CC} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

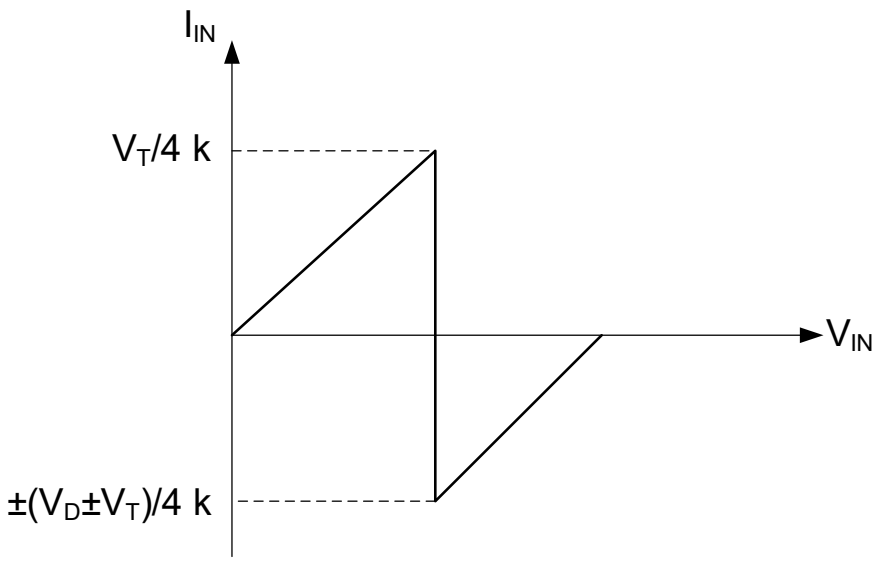
The ET5014L translators have a power down feature that provides design flexibility. The output ports are disabled when either power supply is off (V_L or V_{CC} = 0V). This feature causes all of the I/O pins to be in the power saving high impedance state.

About Pull-Up/Pull-Down Resistors

Do not use any pull-up or pull-down resistors. This device has bus-hold circuits: pull-up or pull-down resistors are not recommended because they interfere with the output state. The current through these resistors may exceed the hold drive's bus-hold current (see figure below), resulting in data transition and/or auto-direction sensing failures. The bus-hold feature eliminates the need for extra resistors.

Input Driver Requirements

For correct operation, the device driving the data I/Os of the ET5014L must have a minimum drive capability of ±2 mA (see figure below) for a plot of typical input current versus input voltage.



VT: Input threshold voltage of the ET5014L

VD: Supply voltage of the external driver

Figure 4. Typical IIN vs VIN Curve

Absolute Maximum Ratings

Symbol	Parameter	Condition	Value	Unit
V_{CC}	High-side DC Supply Voltage		-0.5 to +5.5	V
V_L	Low-side DC Supply Voltage		-0.5 to +5.5	V
I/O V_{CC}	V_{CC}-Referenced DC Input/Output Voltage		-0.5 to +5.5	V
I/O V_L	V_L-Referenced DC Input/Output Voltage		-0.5 to +5.5	V
V_I	Enable Control Pin DC Input Voltage		-0.5 to +5.5	V
I_{IK}	DC Input Diode Current	V_I < GND	-50	mA
I_{OK}	DC Output Diode Current	V_O < GND	-50	mA
I_{CC}	DC Supply Current Through V_{CC}		±100	mA
I_L	DC Supply Current Through V_L		±100	mA
I_{GND}	DC Ground Current Through Ground Pin		±100	mA
T_J	Max Junction Temperature		+150	°C
T_{STG}	Storage Temperature		-65 to +150	°C
ESD	Human Body Model, JEDEC JS-001		±4000	V
	Charged Device Model, JEDEC JS-002		±1000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	High-side Positive DC Supply Voltage		1.08	5.0	V
V_L	Low-side Positive DC Supply Voltage		1.08	5.0	V
V_I	Enable Control Pin Voltage		GND	5.0	V
V_{IO}	Bus Input/Output Voltage	I/O V_{CC}	GND	5.0	V
		I/O V_L	GND	5.0	
T_A	Operating Temperature Range		-40	+85	°C
△t/△V	Input Transition Rise or Rate V_I, V_{IO} from 30% to 70% of V_{CC}; V_{CC} = 3.3 V ± 0.3 V		0	10	ns

DC Electrical Characteristics

(***Note:*** V_S is the corresponding supply for IO, i.e. V_{CC} for IO_V_{CC} and V_L for IO_V_L)

Symbol	Parameter	Test Conditions[1]	V_{CC} [2]	V_L [3]	-40°C to +85°C			Unit
					Min	Typ [4]	Max	
V_{IH}	I/O Input HIGH Voltage		1.08~5.0	1.08~5.0	0.65* V_S	-	-	V
V_{IL}	I/O Input LOW Voltage		1.08~5.0	1.08~5.0	-	-	0.35* V_S	V
V_{IH-EN}	Control Pin Input HIGH Voltage	T_A=+25°C	1.08~5.0	1.08~5.0	0.65* V_S	-	-	V
V_{IL-EN}	Control Pin Input LOW Voltage	T_A=+25°C	1.08~5.0	1.08~5.0	-	-	0.35* V_S	V
V_{OH}	I/O Output HIGH Voltage	I/O Source Current = 20uA	1.08~5.0	1.08~5.0	V_S - 0.2	-	-	V
V_{OL}	I/O Output LOW Voltage	I/O Source Current = 20uA	1.08~5.0	1.08~5.0	-	-	0.2	V
I_Q	Static Supply Current	EN = V_L, I_O = 0 A, (I/O-in = 0 V or V_S, I/O-out = Float)	1.08~5.0	1.08~5.0	-	-	1	uA
I_{TS}	Tristate Output Mode Supply Current	EN = 0 V, (I/O-in = 0 V or V_S, I/O-out = Float)	1.08~5.0	1.08~5.0	-	-	1	uA
I_{OZ}	Tristate Output Mode I/O Leakage Current	EN = 0 V	1.08~5.0	1.08~5.0	-	-	±1	uA
I_I	Control Pin Input Current	T_A = +25°C	1.08~5.0	1.08~5.0	-	-	±1	uA
I_{OFF}	Power off Leakage Current	I/O V_{CC} = 0 to V_{CC}, I/O V_L = 0 to V_L	0	0	-	-	3.0	uA
			1.08~5.0	0	-	-	3.0	
			0	1.08~5.0	-	-	3.0	

Note1: Normal test conditions are V_I = 0 V, C_{IOVCC} ≤ 15 pF and C_{IOVL} ≤ 15 pF, unless otherwise specified.

Note2: V_{CC} is the supply voltage associated with the I/O V_{CC} port, and V_{CC} ranges from +1.08V to 5.0V under normal operating conditions.

Note3: V_L is the supply voltage associated with the I/O V_L port, and V_L ranges from +1.08V to 5.0V under normal operating conditions.

Note4: Typical values are for V_{CC} = +2.8V, V_L = +1.8V and T_A = +25°C. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Timing Characteristics

Symbol	Parameter		Test Conditions[5]	V_{CC} [6]	V_L [7]	-40°C to +85°C			Unit
						Min	Typ[8]	Max	
T_R	I/O Rise Time		C_{IO} = 15pF	1.08~5.0	1.08~5.0			9.5	ns
				1.8~5.0	1.8~5.0			7.5	
T_F	I/O Fall Time		C_{IO} = 15pF	1.08~5.0	1.08~5.0			9.5	ns
				1.8~5.0	1.8~5.0			7.5	
Z_{OVCC}	I/O V_{CC} One-Shot Output Impedance		[9]	1.8	1.08~5.0		20		Ω
				5.0			6.0		
Z_{OVL}	I/O V_L One-Shot Output Impedance		[9]	1.08~5.0	1.8		20		Ω
					5.0		6.0		
t_{PD}	Propagation Delay (Driving I/O V_{CC} or I/O V_L)		C_{IOVCC} = 15pF	1.08~5.0	1.08~5.0			35	ns
				1.8~5.0	1.8~5.0			13	
			C_{IOVCC} = 30pF	1.08~5.0	1.08~5.0			35	
				1.8~5.0	1.8~5.0			15	
			C_{IOVCC} = 50pF	1.08~5.0	1.08~5.0			37	
				1.8~5.0	1.8~5.0			15	
t_{SK}	Channel-to -Channel Skew		C_{IOVCC} = C_{IOVL} =5pF[9]	1.08~5.0	1.08~5.0			3	ns
I_{IN_PEAK}	Input Driver Maximum Peak Current		I/O_V_{CC} = 1MHz Square Wave, Amplitude = V_{CC}, or I/O_V_L = 1 MHz Square Wave, Amplitude = V_L EN = V_L[9]	1.08~5.0	1.08~5.0			2	mA
t_{EN}	I/O Output Enable Time	t_{PZH}	C_{IO} = 15 pF, I/O_V_L = V_L	1.08~5.0	1.08~5.0			170	ns
		t_{PZL}	C_{IO} = 15pF, I/O_V_L = 0V	1.08~5.0	1.08~5.0			170	
t_{DIS}	I/O Output Disable Time	t_{PHZ}	C_{IO} = 15 pF, I/O_V_L= V_L	1.08~5.0	1.08~5.0			180	ns
		t_{PLZ}	C_{IO} = 15pF, I/O_V_L = 0V	1.08~5.0	1.08~5.0			175	

Timing Characteristics (Continued)

Symbol	Parameter	Test Conditions[5]	V_{CC} [6]	V_L [7]	-40°C to +85°C			Unit
					Min	Typ[8]	Max	
MDR[10]	Maximum Data Rate	C_{IO} = 15pF	1.08~5.0	1.08~5.0	40			Mbps
			1.5~5.0	1.5~5.0	80			
			1.8~5.0	1.8~5.0	100			
			2.3~5.0	2.3~5.0	160			
		C_{IO} = 30pF	1.08~5.0	1.08~5.0	40			
			1.5~5.0	1.5~5.0	72			
			1.8~5.0	1.8~5.0	94			
			2.3~5.0	2.3~5.0	140			
		C_{IO} = 50pF	1.08~5.0	1.08~5.0	35			
			1.5~5.0	1.5~5.0	63			
			1.8~5.0	1.8~5.0	87			
			2.3~5.0	2.3~5.0	120			

Note5: Normal test conditions are V_I = 0V, C_{IOVCC} ≤ 15pF and C_{IOVL} ≤ 15pF, unless otherwise specified.

Note6: V_{CC} is the supply voltage associated with the I/O V_{CC} port, and V_{CC} ranges from +1.08V to 5.0V under normal operating conditions.

Note7: V_L is the supply voltage associated with the I/O V_L port, and V_L ranges from +1.08V to 5.0V under normal operating conditions.

Note8: Typical values are for V_{CC} = 2.8V, V_L = 1.8V and T_A = 25°C. All units are production tested at T_A = 25°C. Limits over the operating temperature range are guaranteed by design.

Note9: Guaranteed by design.

Note10: MDR Test Pass Standard: V_{OH} ≥ 70% × V_S, V_{OL} ≤ 30% × V_S.

Test Circuit and Timing

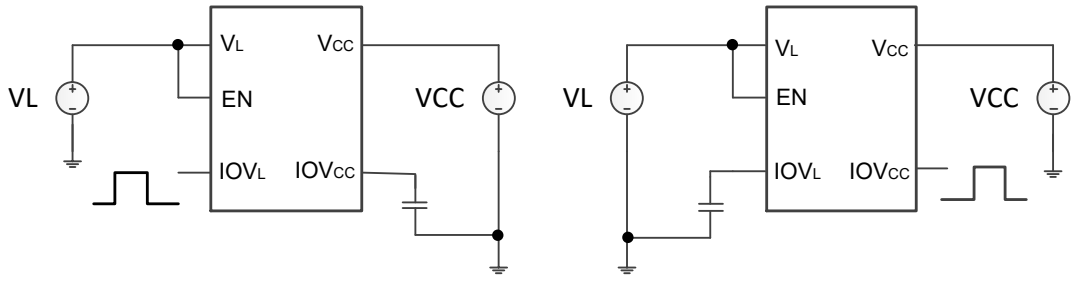


Figure 5. Driving I/O Tr / Tf / Tpd Test Circuit

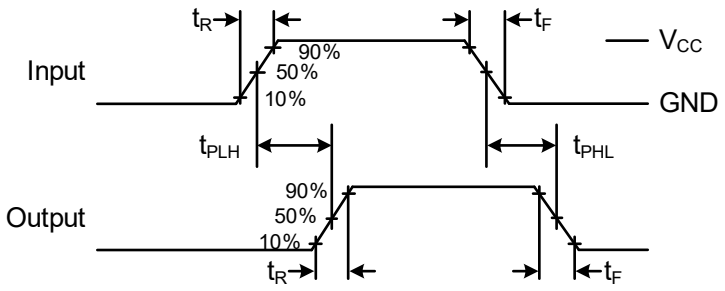
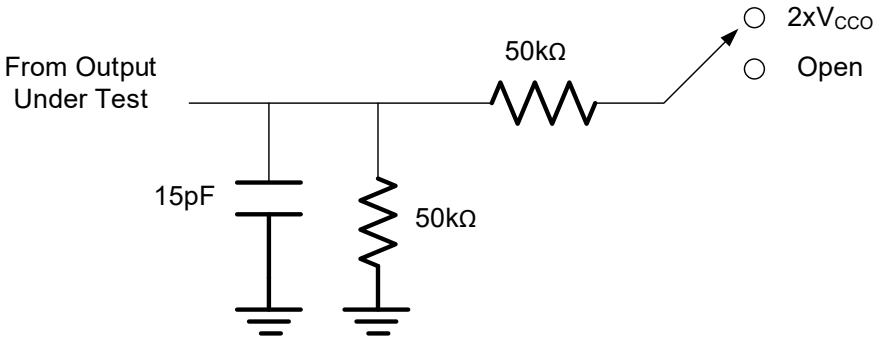


Figure 6. Driving I/O T_R / T_F / Tpd Test Timing



Test	Switch
t_{PZH}, t_{PHZ}	open
t_{PZL}, t_{PLZ}	2 × V_{CCO}

Figure 7. Enable / Disable Test Circuit

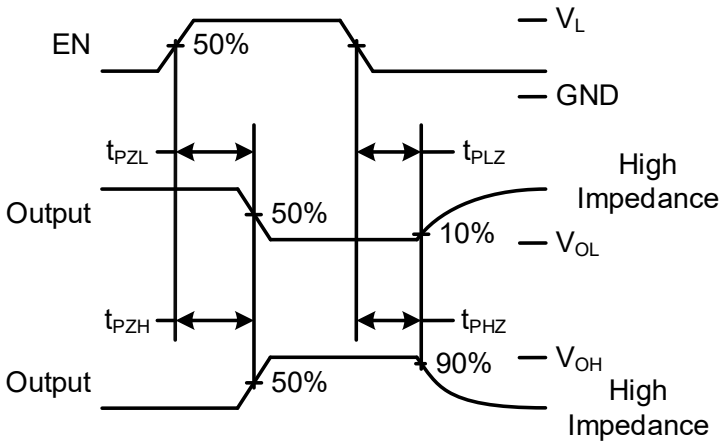


Figure 8. Enable / Disable Test Timing

Typical Application Circuits[11]

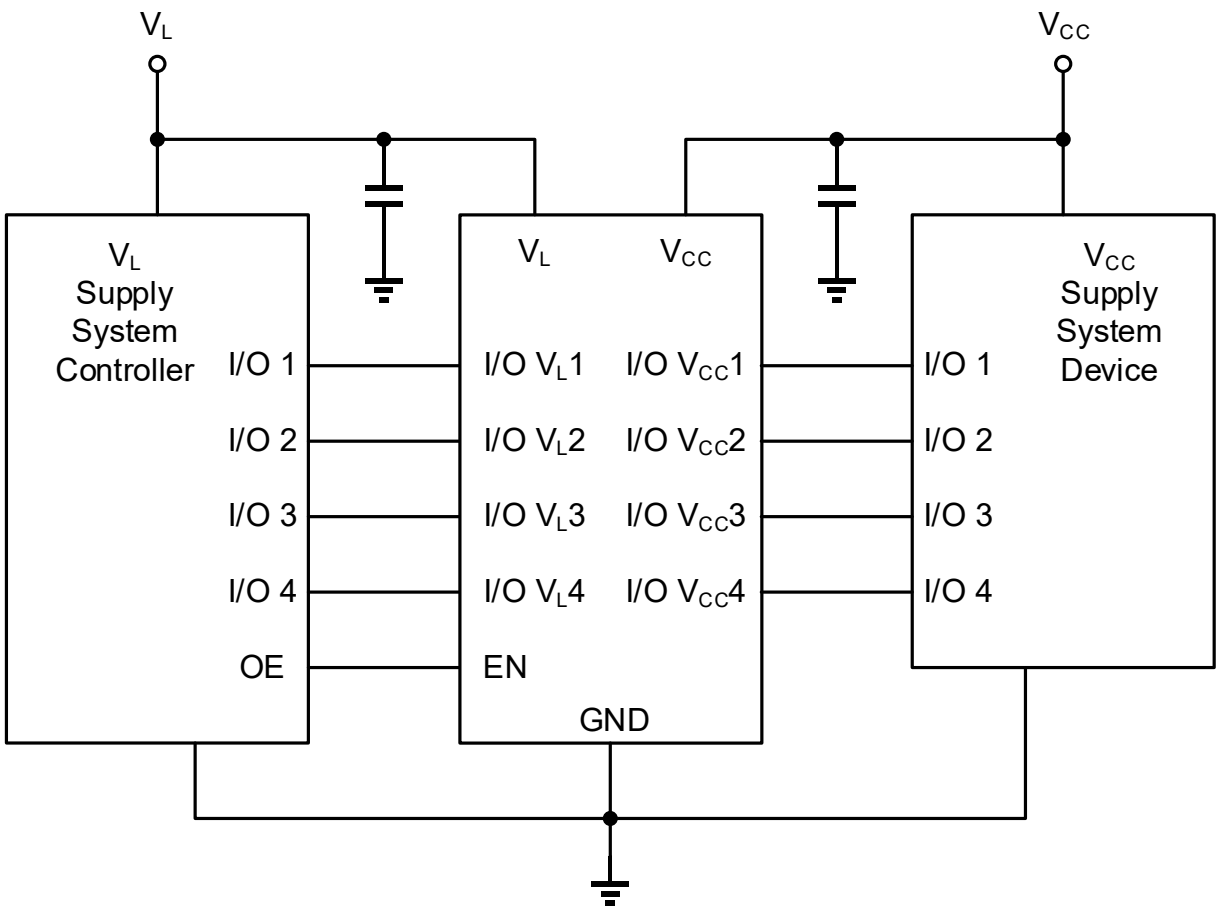
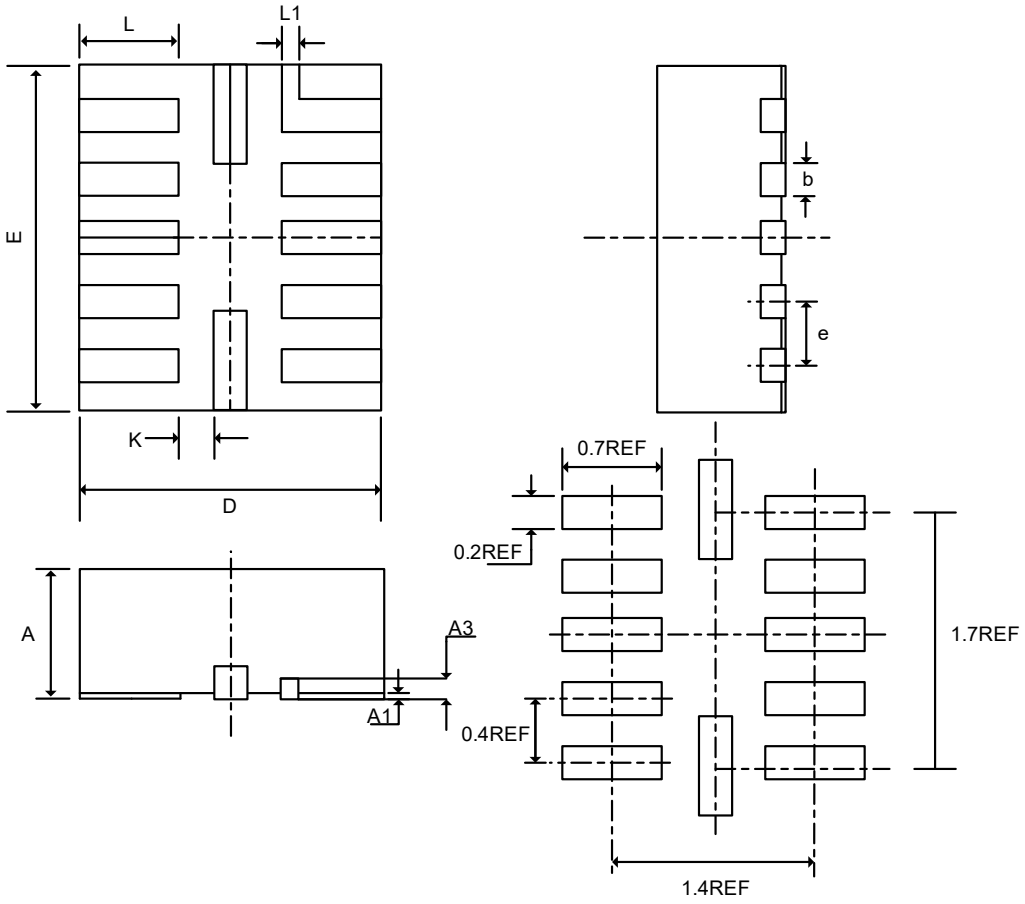


Figure 9. Typical Application Circuit

Note11: This electric circuit only supplies for reference.

Package Dimension

QFN12



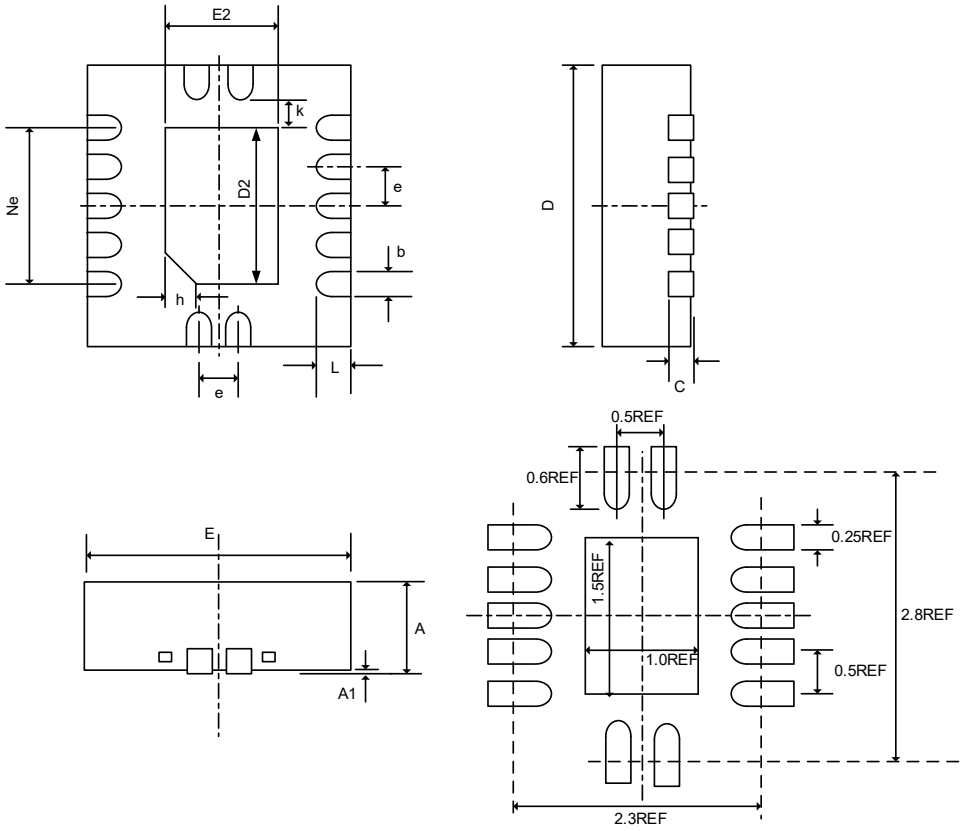
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	MAX
A	0.450	0.550
A1	0.000	0.050
A3	0.152 REF.	
b	0.150	0.250
D	1.600	1.800
E	1.900	2.100
e	0.400 TYP.	
L	0.450	0.550
L1	0.150 REF.	
K	0.200 MIN.	

Figure 10. QFN12 Package Dimension

QFN14



COMMON DIMENSIONS

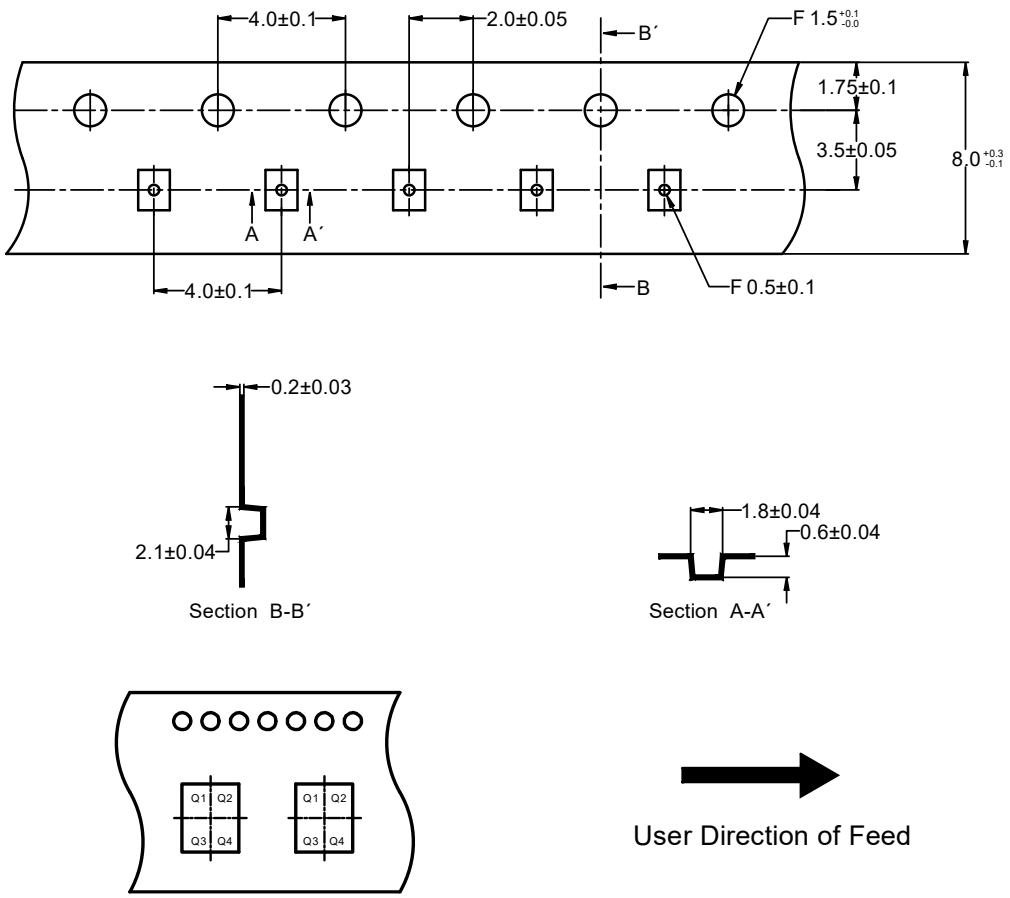
(Unit: mm)

Symbol	Min	Typ	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.2	0.25	0.3
c		0.20 REF	
D	2.90	3.00	3.10
D2	1.40	1.50	1.60
Ne		2.00 BSC	
e		0.50 BSC	
E	2.40	2.50	2.60
E2	0.90	1.00	1.10
L	0.3	0.4	0.5
K	0.20	-	-
h		0.25 REF	

Figure 11. QFN14 Package Dimension

Tape Information

QFN12



Pin1 Quadrant: Q1

Unit: mm

Figure 12. Tape Information

Marking

QFN12
5014 - Part Number
XXXX - Tracking Number

QFN14
14LY - Part Number
XXXX - Tracking Number

Figure 13. Marking

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2022-1-14	Initial Version	Ma Yong Jian	Ma Yong Jian	Zhu Jun Li
1.1	2022-6-18	Updated form	Shi Bo	Shi Liang Jun	Zhu Jun Li
1.2	2023-3-6	I_{OFF} up to 1.2uA	Shi Bo	Shi Liang Jun	Zhu Jun Li
1.3	2023-6-1	Update VCC/VL Operating Range	Wang Peng	Zhang Zhi Wei	Zhu Jun Li
1.4	2023-10-23	Updated EC Table, Add note10	Wang Peng	Zhang Zhi Wei	Zhu Jun Li
1.5	2025-10-10	Updated Package Dimension	Zhang Wang	Zhang Zhi Wei	Zhu Jun Li