

400mA Ultra-Low Noise, High PSRR LDO for RF and Analog Circuits

General Description

The ET538XXYB of low-dropout (LDO), low-power linear regulators offer up to 400mA with PMOS pass transistor. The device offers low noise, high PSRR, low quiescent current and very good line/load transients, suitable for RF applications and analog circuits.

The ET538XXYB is stable with a 1 μ F input and 1 μ F ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve accuracy of 1.5%.

It is in a small DFN4(1x1) package, which is ideal for small form factor portable equipment such as wireless handsets and PDAs.

Features

- Wide Input Voltage Range from 2.2V~5.5V
- Output Voltage Range from 1.2V to 4.3V
- Output Voltage Accuracy are $\pm 1.5\%$
- Output Current are up to 400mA
- Very Low IQ of 20 μ A Typical
- Shutdown Current of 0.1 μ A Typical
- Low Dropout are Typical 180mV at 400mA, 2.8V Output
- Ultra Low Noise are Typical 8 μ V_{RMS} (Load=200mA)
- Very High PSRR are 100dB at 1KHz, 45dB at 1MHz, 30mA
- Excellent Line/Load Transient Response
- Built-in I_{LIMIT} Protection and Thermal Shutdown Circuit
- Built-in Auto Discharge Function
- Package Information:

Part No.	Package	MSL
ET538XXYB	DFN4 (1 x 1)	Level 1

Applications

- Smart Phones and Cellular Phones
- PDAs
- MP3/MP4 Player
- Digital Still Cameras
- Portable instrument

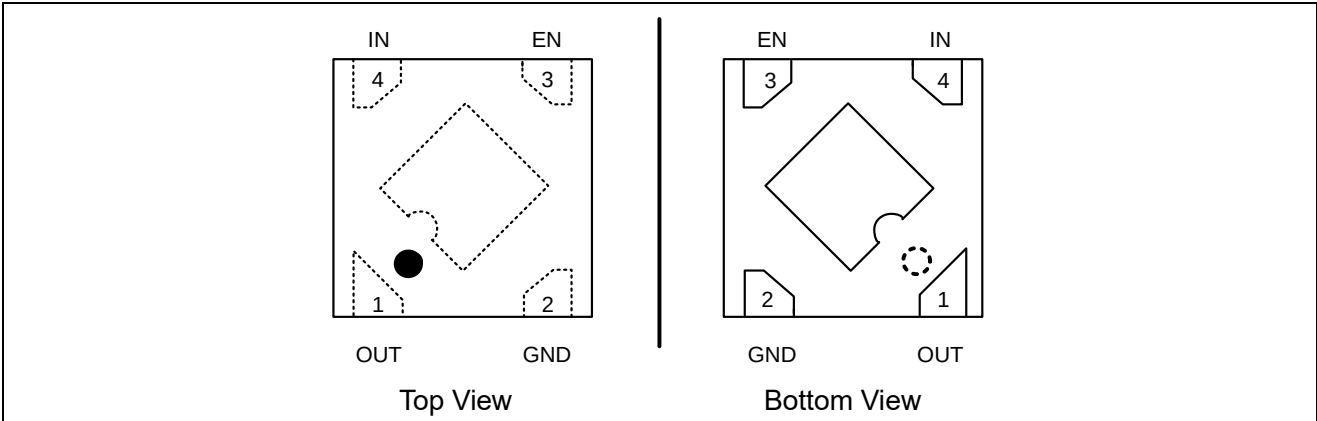
ET538XXYB

Device information

ET 538 XX Y B

<u>XX</u> Output Voltage		<u>Y</u> Package		<u>B</u> Auto-discharge Function	
XX	Fixed Output Voltage	Y	DFN4 -1.0×1.0	B	Available

Pin Configuration

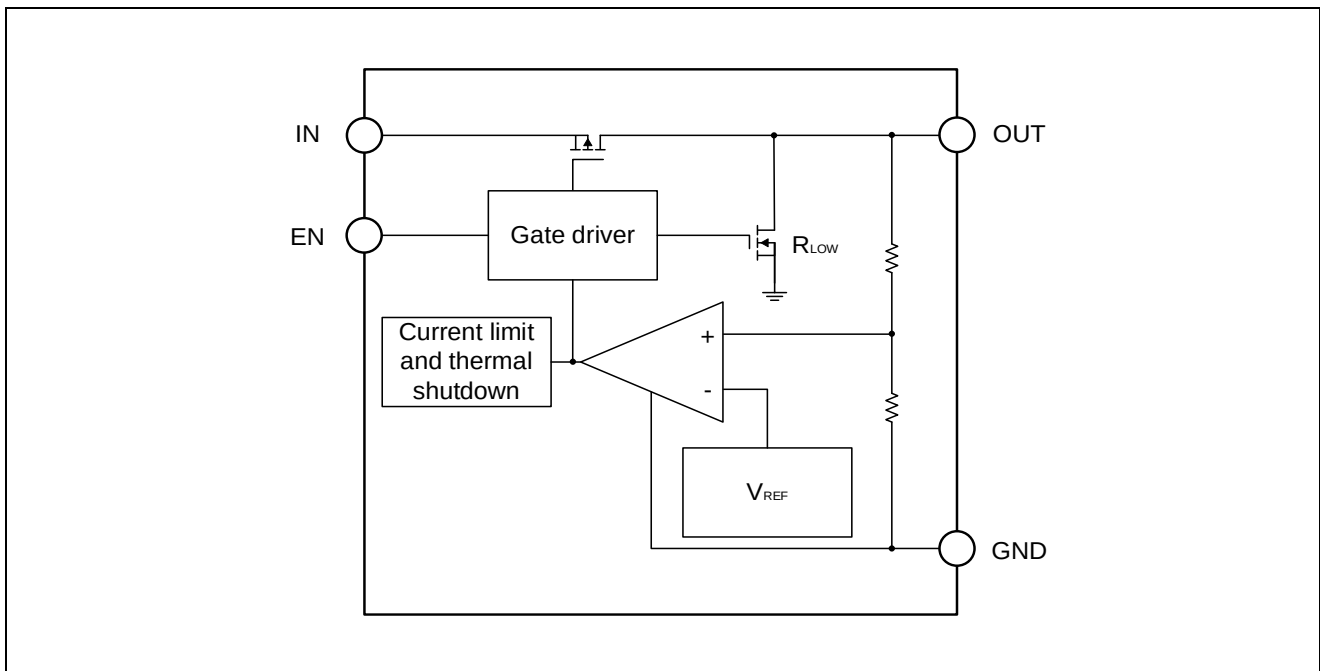


Pin Function

Pin No.	Pin Name	Pin Function
1	OUT	Output pin. A 1μF low-ESR capacitor should be connected to this pin to ground.
2	GND	Ground.
3	EN	Enable control input, active high. Do not leave EN floating.
4	IN	Supply input pin. Must be closely decoupled to GND with a 1μF ceramic capacitor.
-	Thermal Pad	Thermal pad , connect to GND plane for better power dissipation.

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Block Diagram



Functional Description

Input Capacitor

A 1 μ F ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 μ F to 10 μ F, Equivalent Series Resistance (ESR) is from 5m Ω to 100m Ω , and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins. With a reasonable PCB layout, the single 1 μ F ceramic output capacitor can be placed up to 10cm away from the ET538XXYB device.

Remote Output Capacitor Placement

The ET538XXYB requires at least a 1 μ F capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10cm away from the LDO.

ON/OFF Input Operation

The ET538XXYB is turned on by setting the EN pin higher than V_{IH} threshold, and is turned off by pulling it lower than V_{IL} threshold. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time.

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Low Quiescent Current

The ET538XXYB, consuming only 20 μ A quiescent current, provides great power saving in portable and low power applications.

High PSRR and Low Noise

The ET538XXYB, with PSRR of 100dB at 1KHz,30mA is suitable for most of these applications that require high PSRR and low noise.

Fast Transient Response

The ET538XXYB's fast transient response from 0 to 400mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

Dropout Voltage

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage. The ET538XXYB internal circuitry is not fully functional until V_{IN} is at least 2.2V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2V or ($V_{OUT} + V_{DROP}$).

Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuiting to GND, the current limit protection will be triggered and clamp the output current to approximately 650mA to prevent over-current and to protect the regulator from damage due to overheating.

Output Automatic Discharge

The ET538XXYB output employs an internal 350 Ω (Typical) pull-down resistance to discharge the output when the EN pin is low, and the device is disabled.

Thermal Overload Protection

Thermal shutdown disables the output when the junction temperature rises to approximately 150°C which allows the device to cool. When the junction temperature cools to approximately 120°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the ET538XXYB has been designed to protect against temporary thermal overload conditions. The TSD circuitry was not intended to replace proper heat-sinking. Continuously running the ET538XXYB device into thermal shutdown may degrade device reliability

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Absolute Maximum Ratings

Symbol	Parameters (Items)	Value	Unit
V_{IN}	Input Voltage(IN Pin)	-0.3 to 6.0	V
V_{EN}	Input Voltage (EN Pin)	-0.3 to 6.0	V
V_{OUT}	Output Voltage(OUT Pin)	-0.3 to $V_{IN}+0.3$	V
P_{D_MAX} ⁽¹⁾	Maximum Power Consumption	500	mW
I_{MAX}	Maximum Load Current	400	mA
T_J	Operating Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SLOD}	Lead Temperature (Soldering, 10 sec)	260	°C
V_{ESD}	HBM (ESDA/JEDEC JS-001-2017)	±4000	V
	CDM (ESDA/JEDEC JS-002-2014)	±1500	V
I_{LU}	Latch up Current Maximum Rating (JESD78E)	±200	mA

Note (1): Rating at mounting on a board (PCB board dimension: 40mm x 40mm (4layer), copper: 1OZ).

Recommended Operating Conditions

Symbol	Parameters	Rating	Unit
V_{IN} ⁽²⁾	Input Voltage	2.2 to 5.5	V
V_{OUT}	Output Voltage	1.2 to 4.3	V
I_{OUT}	Output Current	0 to 400	mA
T_A	Operating Ambient Temperature	-40 to 85	°C
C_{IN}	Effective Input Ceramic Capacitor Value	0.68 to 10	μF
C_{OUT}	Effective Output Ceramic Capacitor Value	0.68 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

Note (2): In order to achieve high performance of PSRR, it is recommended that the V_{IN} needs to be no smaller than ($V_{OUT}+0.5V$).

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Electrical Characteristics

($V_{IN} = V_{OUT} + 1V$, $V_{EN} = 1.2V$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$. Typical values are at $T_A = 25^\circ C$, unless otherwise stated)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{IN}^{(3)}$	Input Voltage Range		2.2		5.5	V
V_{UVLO}	Under Voltage Lockout	V_{IN} Rising	1.8	2.0	2.2	V
		V_{IN} Falling	1.7	1.9	2.1	V
$V_{DROP}^{(4)}$	Dropout Voltage	$V_{OUT} = 1.8V$, $I_{OUT} = 400mA$			400	mV
		$V_{OUT} = 2.2V$, $I_{OUT} = 400mA$		200	280	mV
		$V_{OUT} = 2.8V$, $I_{OUT} = 400mA$		180	260	mV
I_{Q_ON}	Input Quiescent Current	$I_{OUT} = 0mA$		20	40	μA
I_{Q_OFF}	Input Shutdown Quiescent Current	$V_{EN} = 0V$		0.1	1	μA
V_{OUT}	Output Voltage Accuracy	$V_{IN} = V_{OUT(NOM)} + 1V$, $I_{OUT} = 1mA$, $T_A = -40^\circ C < T_A < 85^\circ C$	-1.5		1.5	%
Reg_{LINE}	Line Regulation	$V_{IN} = V_{OUT} + 1V$ to $5.5V$, $I_{OUT} = 1mA$		0.01	0.1	%/V
Reg_{LOAD}	Load Regulation	$I_{OUT} = 1mA$ to $400mA$		20	40	mV
I_{OUT}	Output Current		400			mA
I_{LIMIT}	Current Limit	$T_A = 25^\circ C$	450	650	850	mA
I_{SHORT}	Short Current Limit	$V_{OUT} = 0V$, $T_A = 25^\circ C$	50	140	260	mA
$PSRR^{(5)}$	Power Supply Rejection Ratio	$f = 100\text{ Hz}$, $I_{OUT} = 30mA$		90		dB
		$f = 1\text{ kHz}$, $I_{OUT} = 30mA$		100		dB
		$f = 100\text{ kHz}$, $I_{OUT} = 30mA$		65		dB
		$f = 1\text{ MHz}$, $I_{OUT} = 30mA$		45		dB
$e_N^{(5)}$	Output Noise Voltage	$BW = 10\text{ Hz to }100\text{ kHz}$, $I_{OUT} = 10mA$		9		μV_{RMS}
		$BW = 10\text{ Hz to }100\text{ kHz}$, $I_{OUT} = 200mA$		8		μV_{RMS}
V_{IH}	EN Low Threshold	$V_{IN} = 2.2$ to $5.5V$	0.84			V
V_{IL}	EN High Threshold	$V_{IN} = 2.2$ to $5.5V$			0.40	V
I_{EN}	EN Input current	$V_{EN} = 0$ to $5.5V$		0.5	1	μA
$V_{TRLN}^{(5)}$	Line Transient	$V_{IN} = (V_{OUT} + 1V)$ to $(V_{OUT} + 2V)$ in $10\mu s$		5	20	mV
		$V_{IN} = (V_{OUT} + 2V)$ to $(V_{OUT} + 1V)$ in $10\mu s$		5	20	mV
$V_{TRLD}^{(5)}$	Load Transient	$I_{OUT} = 1mA$ to $400mA$ in $10\mu s$		25	60	mV
		$I_{OUT} = 400mA$ to $1mA$ in $10\mu s$		20	45	mV
R_{LOW}	Output Discharge FET R_{dson}	$V_{EN} = 0V$, $V_{IN} = 5V$, $I_{OUT} = 10mA$	200	350	500	Ω
t_{ON}	Output Turn-on Time	From $V_{EN} > V_{ENH}$ to $V_{OUT} = 95\%$ of $V_{OUT(NOM)}$		500		μs
$T_{TSD}^{(5)}$	Thermal Shutdown Threshold	T_J Rising		150		$^\circ C$
$T_{HYS}^{(5)}$	Thermal Shutdown Hysteresis	T_J Falling from Shutdown		30		$^\circ C$

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Note(3): The maximum input voltage should take into account the maximum power consumption (P_{D_MAX}). The calculation formula is as follows:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT}$$

The maximum power consumption of the circuit is 500mW.

$$V_{IN(MAX)} = 500mW / I_{OUT} + V_{OUT}$$

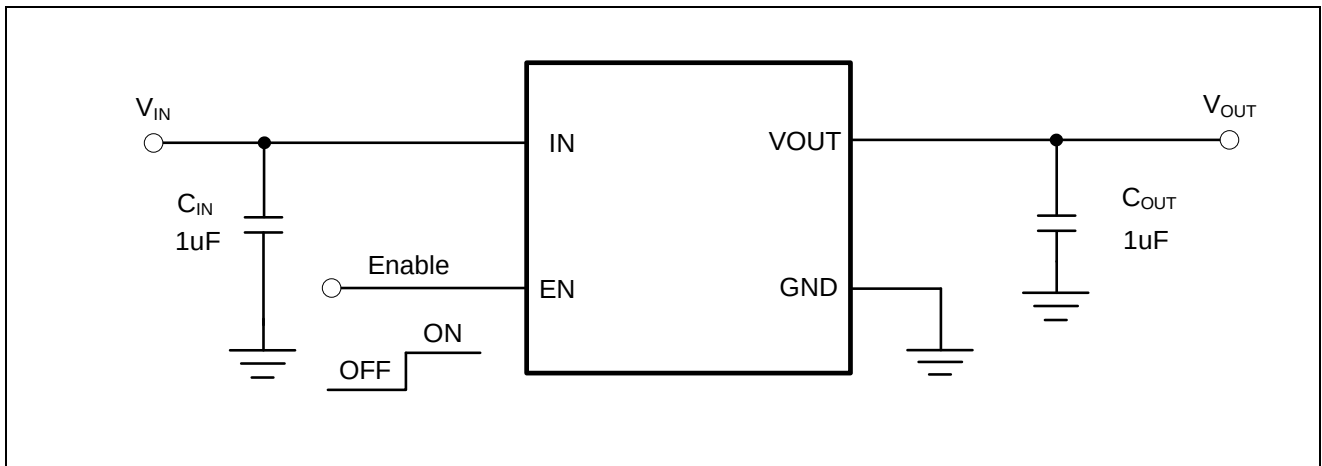
For example:

If $V_{OUT} = 1.2V$, $I_{OUT} = 400mA$, the maximum input voltage is $V_{IN(MAX)} = 500mW / 400mA + 1.2 = 2.45V$

Note(4): V_{DROP} FT test method: test the V_{OUT} voltage at $V_{SET} + V_{DROPMAX}$ with output current.

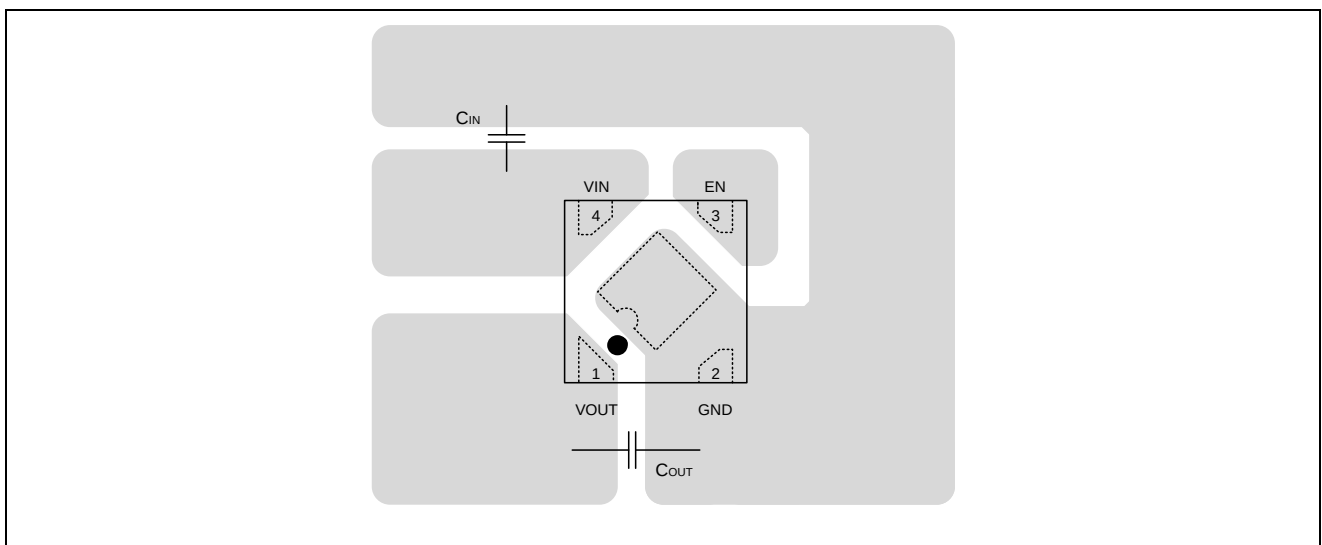
Note(5): Guaranteed by design and characterization. Not a FT item.

Application Circuits



PCB Layout Guide

DFN4

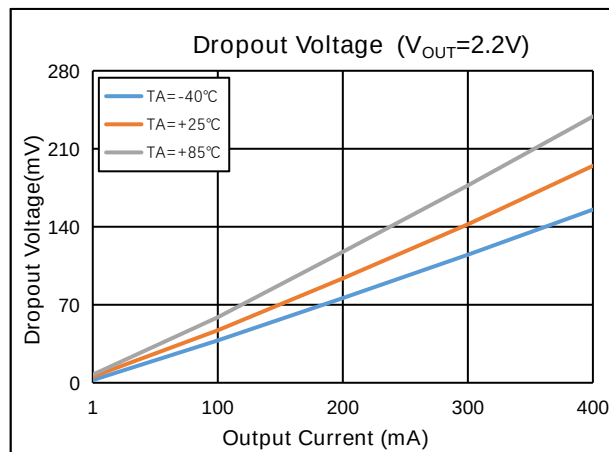
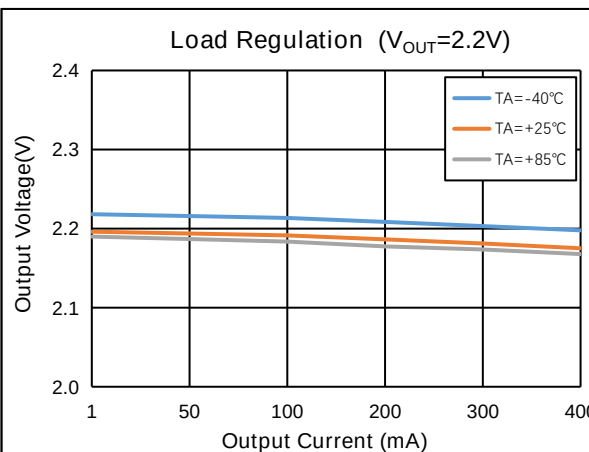
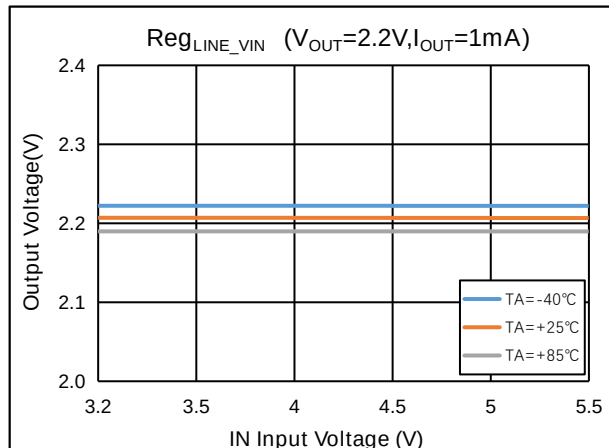
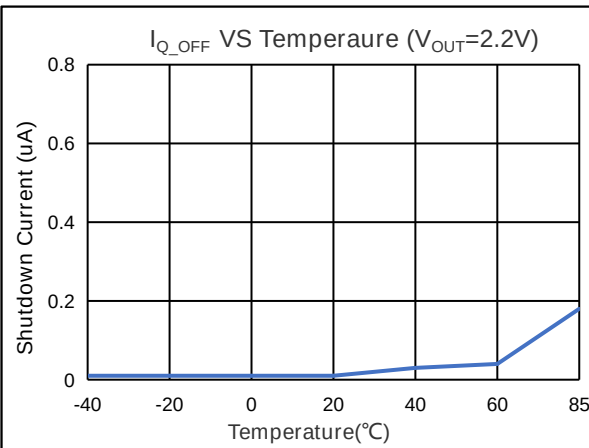
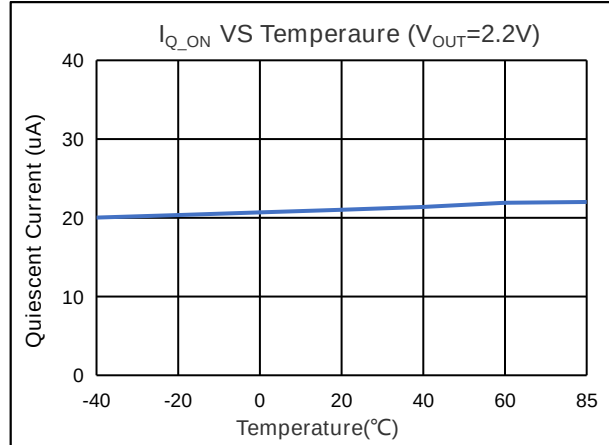
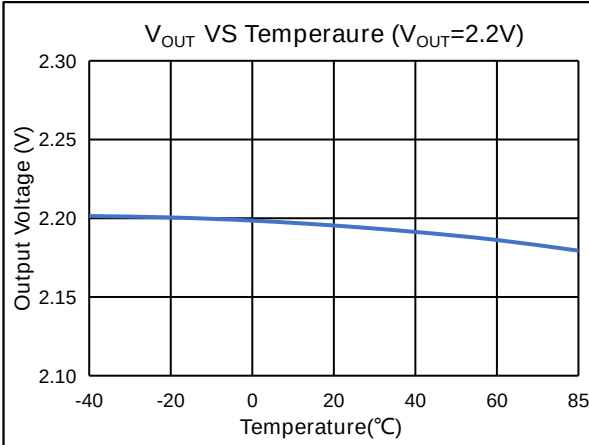


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Typical Characteristics

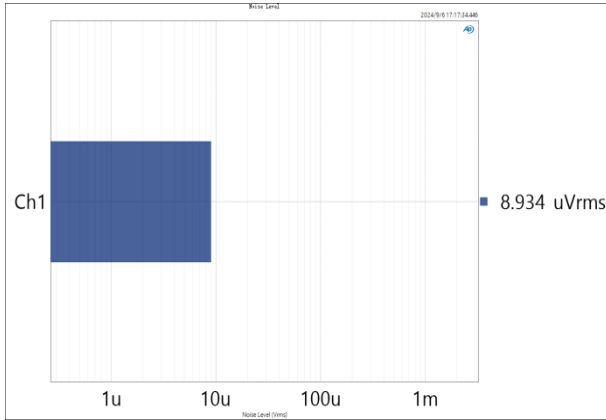
(1) VOLTAGE VERSION 2.2 V

($V_{IN}=3.2V$; $C_{IN}=C_{OUT}=1.0\mu F$, unless otherwise noted. Typical values are at $T_A=25^\circ C$.)

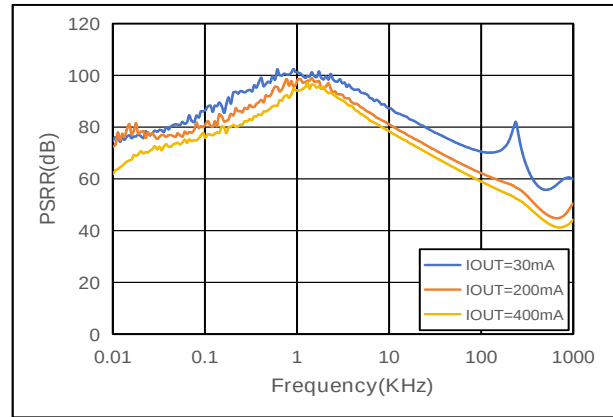


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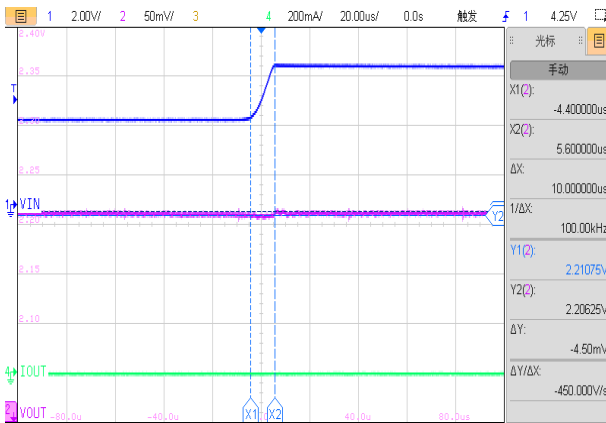
($V_{IN}=3.2V$; $C_{IN}=C_{OUT}=1.0\mu F$, unless otherwise noted. Typical values are at $T_A=25^{\circ}C$.)



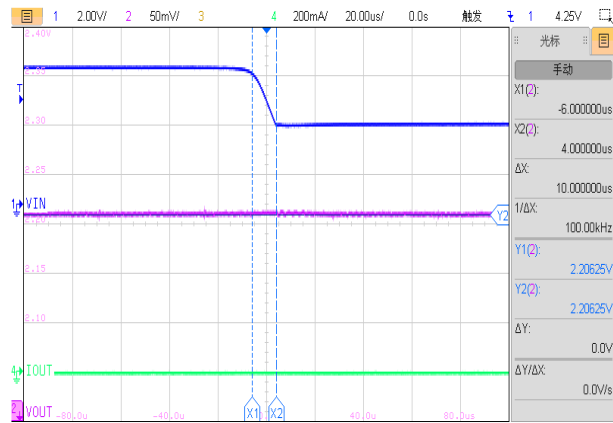
Noise ($I_{OUT}=200mA$)



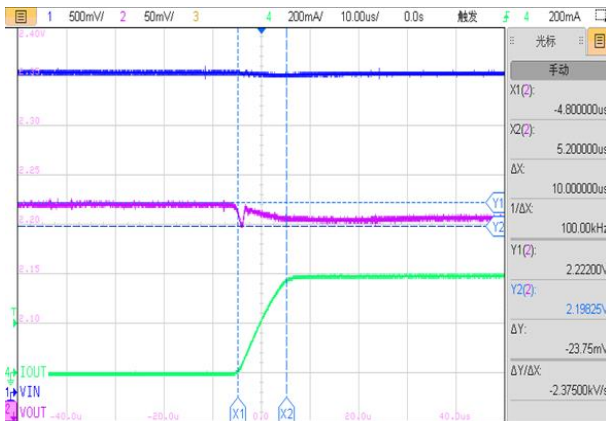
PSRR ($I_{OUT}=200mA$)



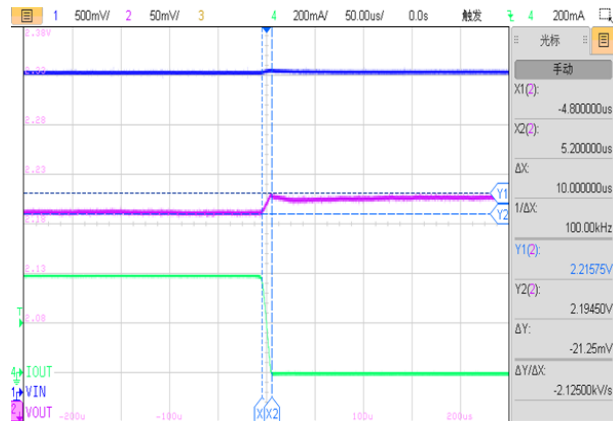
Line Transient ($V_{IN}=3.2\sim 5.5V$ $I_{OUT}=1mA$)



Line Transient ($V_{IN}=5.5\sim 3.2V$ $I_{OUT}=1mA$)



Load Transient ($V_{IN}=3.2V$ $I_{OUT}=1\sim 400mA$)

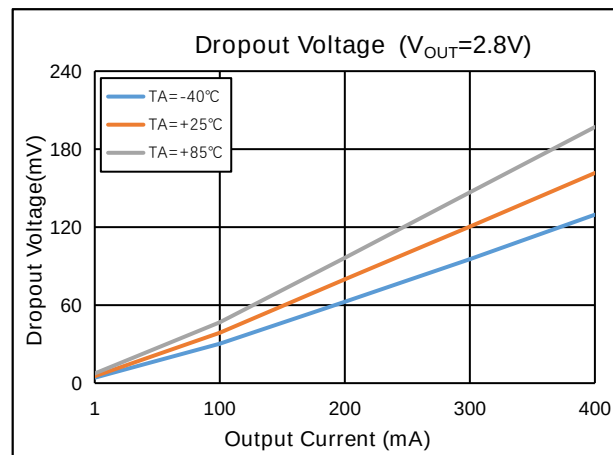
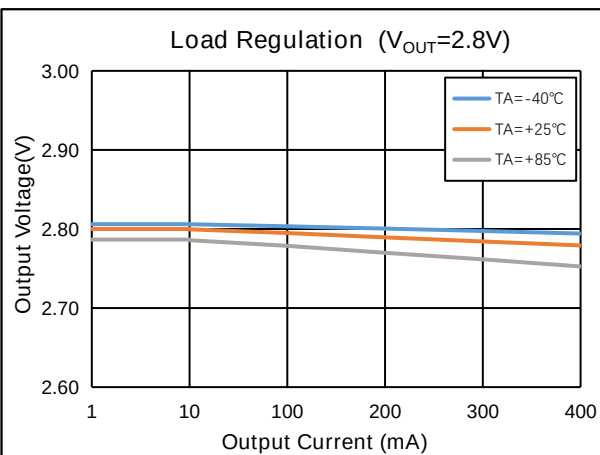
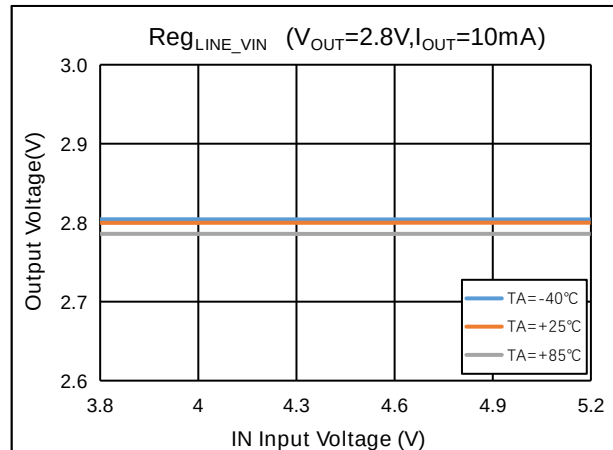
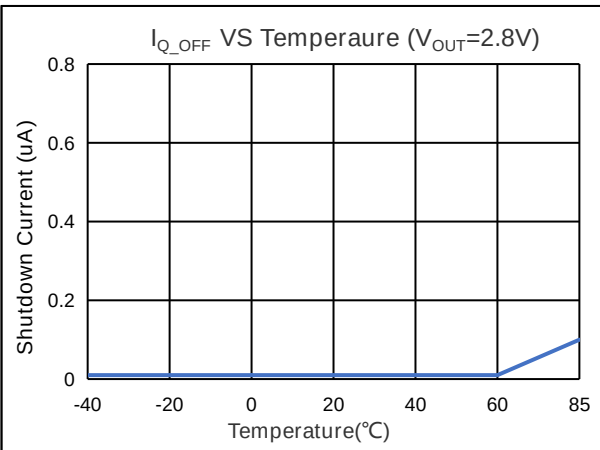
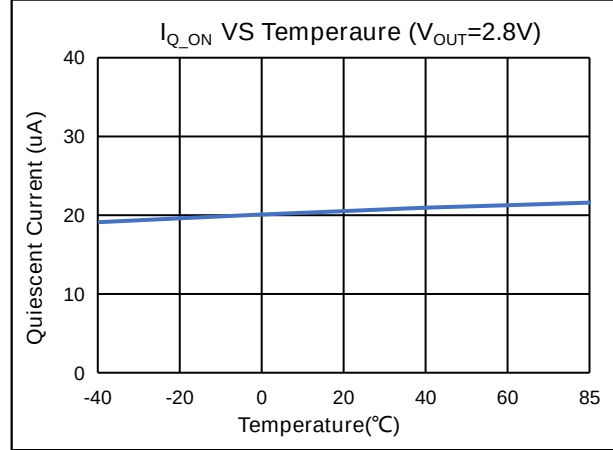
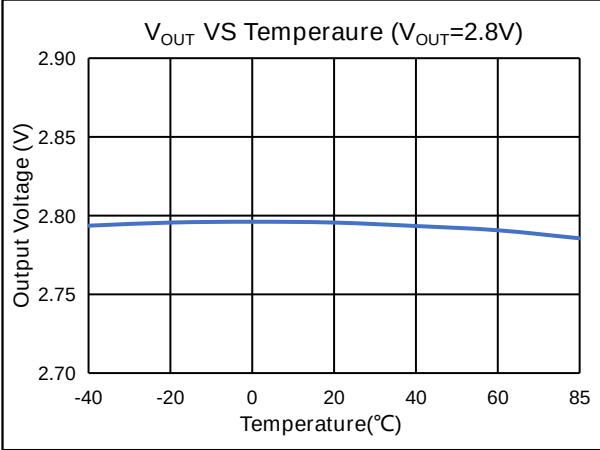


Load Transient ($V_{IN}=3.2V$ $I_{OUT}=400\sim 1mA$)

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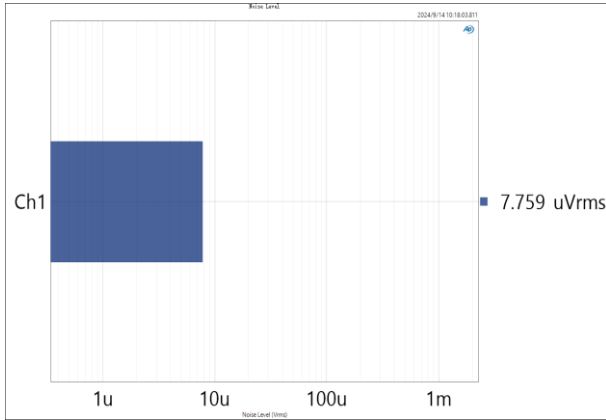
(2) VOLTAGE VERSION 2.8 V

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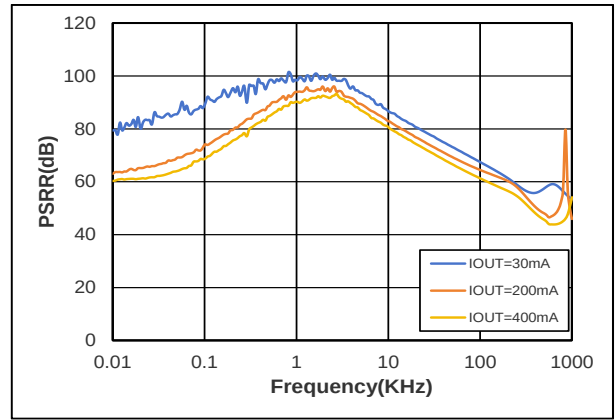


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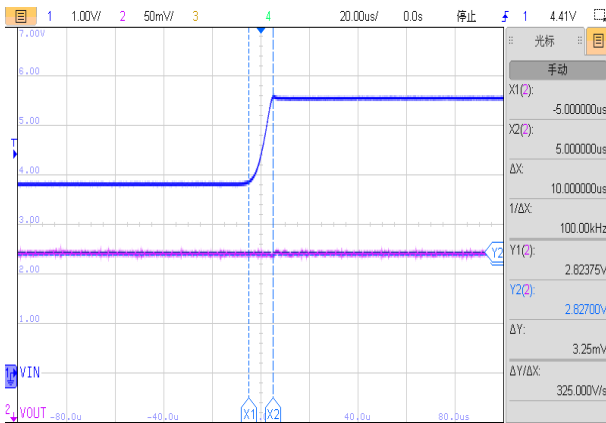
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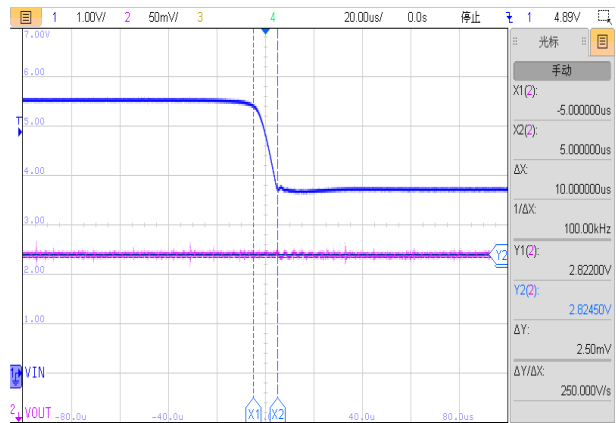
Noise ($I_{OUT}=200mA$)



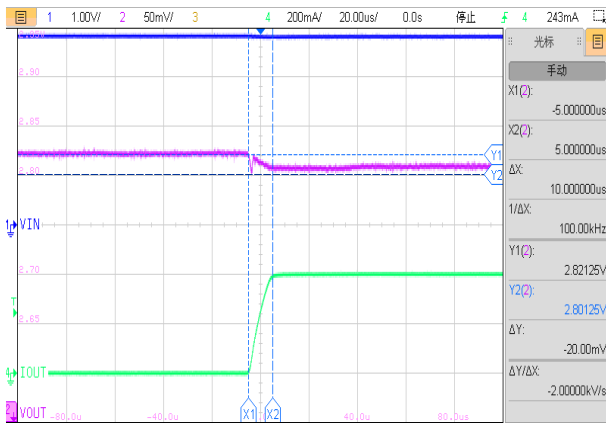
PSRR ($I_{OUT}=200mA$)



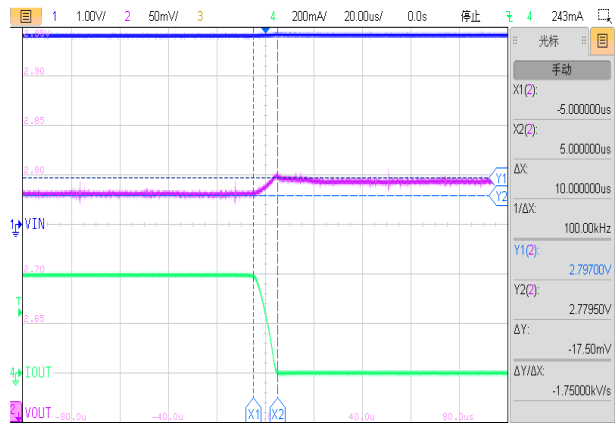
Line Transient ($V_{IN}=3.8\sim 5.5V$ $I_{OUT}=1mA$)



Line Transient ($V_{IN}=5.5\sim 3.8V$ $I_{OUT}=1mA$)



Load Transient ($V_{IN}=3.8V$ $I_{OUT}=1\sim 400mA$)

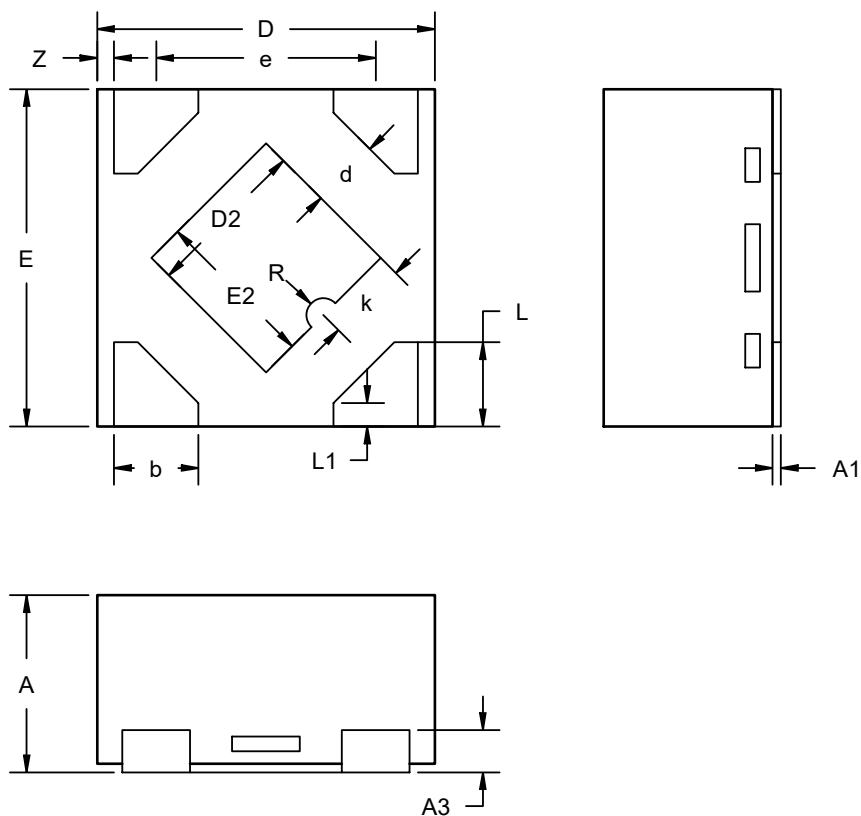


Load Transient ($V_{IN}=3.8V$ $I_{OUT}=400\sim 1mA$)

ET538XXYB

Package Dimension

DFN4(1mm × 1mm)



Dimensions Table (Units: mm)

Symbol	Min	Nom	Max
A	0.35	0.38	0.40
A1	0.00	0.03	0.05
A3	0.127 REF		
D	0.95	1.00	1.05
E	0.95	1.00	1.05
b	0.20	0.25	0.30
L	0.20	0.25	0.30
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
e	0.65 BSC		
k	0.19	0.24	0.29
L1	0.02	0.07	0.12
R	0.02	0.05	0.08
z	0.05 REF		
d	0.205 REF		

