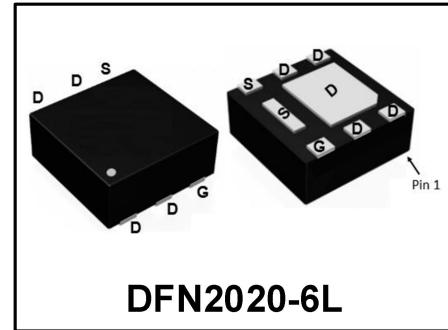


30V N-Channel Enhancement Mode Power MOSFET

Description

EMR13N03M uses advanced power trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

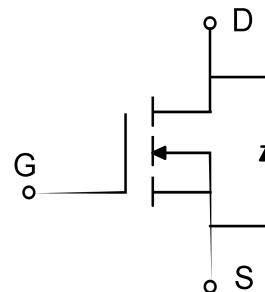


Features

- $V_{DS} = 30V$, $I_D = 12.5A$
 $R_{DS(on)} < 11m\Omega$ @ $V_{GS} = 10V$
 $R_{DS(on)} < 13.5m\Omega$ @ $V_{GS} = 4.5V$
- Green Device Available
- High Power and Current Handling Capability
- MSL1

Applications

- Battery Protection
- Power Management
- Load Switch



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ¹	I_D	12.5	A
$T_A = 100^\circ C$		7.5	
Pulsed Drain Current ²	I_{DM}	38	A
Single Pulse Avalanche Energy ³	EAS	31.2	mJ
Avalanche Current	I_{AS}	25	A
Total Power Dissipation ⁴	P_D	1.71	W
Operating Junction and Storage Temperature Range	T_J , T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ¹	$R_{\theta JA}$	73	°C/W

Electrical Characteristics $T_c = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	30	-	-	V
Gate-body Leakage current	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 12\text{V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 0\text{V}$	-	-	1	μA
Gate-Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	0.4	0.75	1	V
Drain-Source on-Resistance ²	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 8\text{A}$	-	8.5	11	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 6\text{A}$	-	9.0	13.5	
		$V_{\text{GS}} = 2.5\text{V}, I_D = 4\text{A}$	-	10.3	16	
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{\text{DS}} = 15\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$	-	1430	-	pF
Output Capacitance	C_{oss}		-	150	-	
Reverse Transfer Capacitance	C_{rss}		-	124	-	
Switching Characteristics						
Gate Resistance	R_G	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$	-	2.5	-	Ω
Total Gate Charge	Q_g	$V_{\text{GS}} = 4.5\text{V}, V_{\text{DS}} = 15\text{V}, I_D = 10\text{A}$	-	10	-	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	
Gate-Drain Charge	Q_{gd}		-	2.2	-	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{GS}} = 4.5\text{V}, V_{\text{DS}} = 15\text{V}, I_D = 10\text{A}, R_G = 3\Omega$	-	8	-	nS
Rise Time	t_r		-	28	-	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		-	15	-	
Fall Time	t_f		-	7	-	
Drain-Source Body Diode Characteristics						
Diode Forward Voltage ²	V_{SD}	$I_S = 1\text{A}, V_{\text{GS}} = 0\text{V}$	-	-	1	V
Continuous Source Current ^{1,5}	I_S	$V_G = V_D = 0\text{V}$, Force Current	-	-	12.5	A

Notes:

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{\text{DD}}= 25\text{V}, V_{\text{GS}}= 10\text{V}, L= 0.1\text{mH}, I_{\text{AS}}= 25\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation

Typical Characteristics

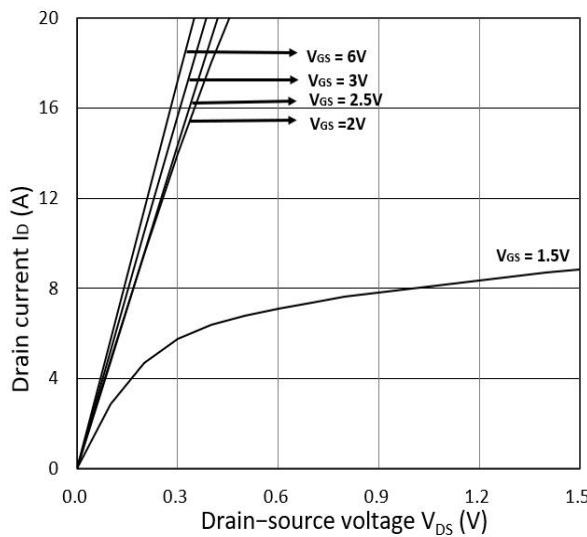


Figure 1. Output Characteristics

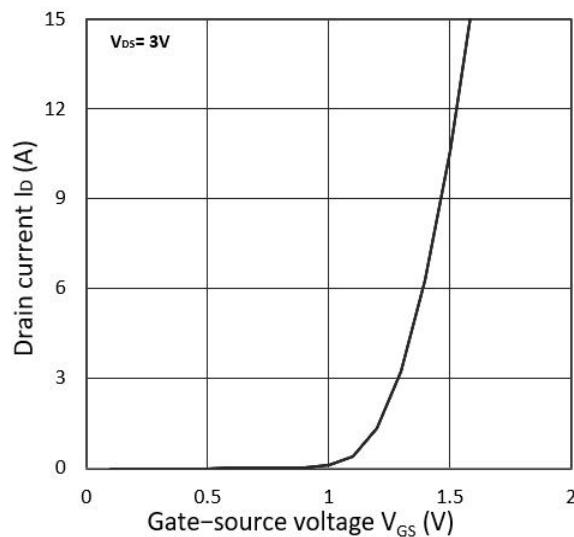


Figure 2. Transfer Characteristic

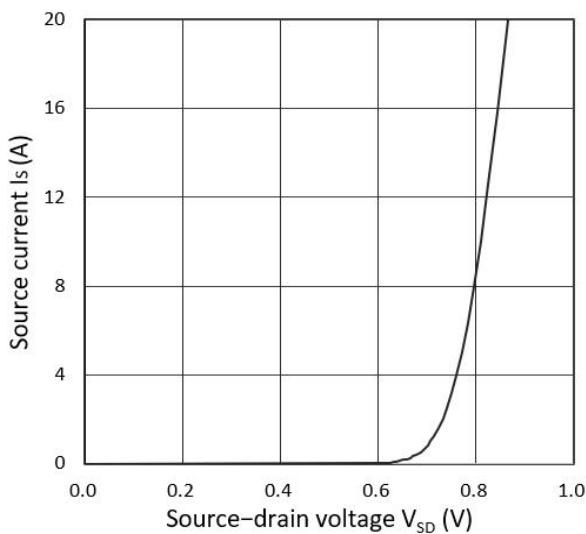


Figure 3. Forward Characteristics of Reverse

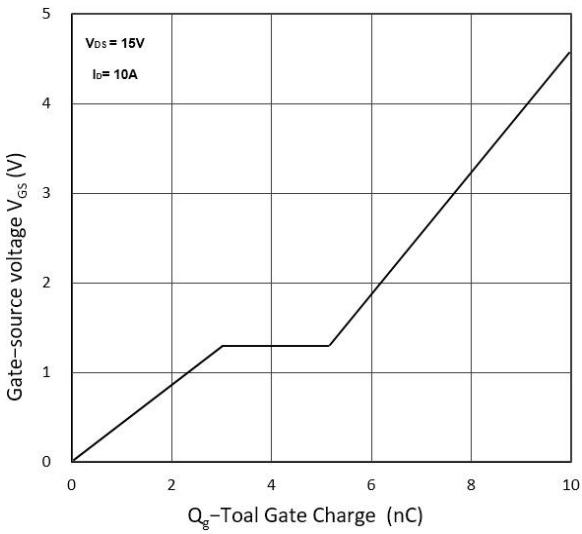
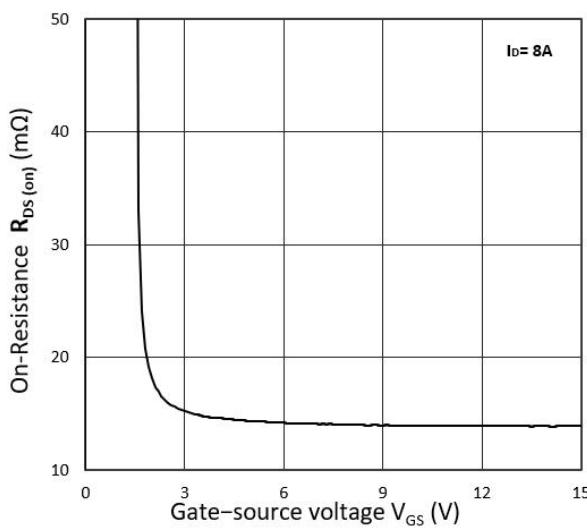
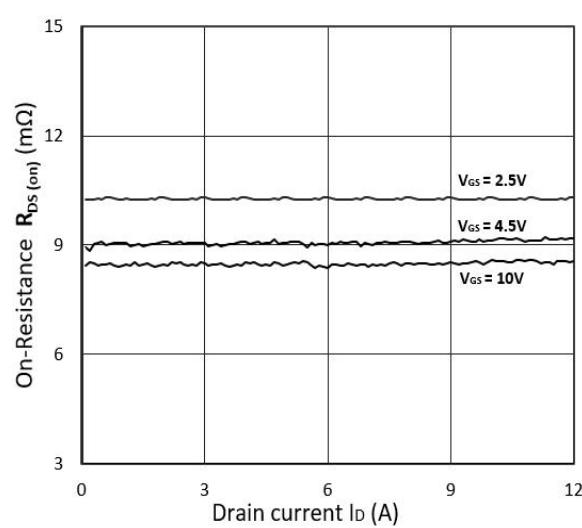


Figure 4. Gate Charge Characteristics

Figure 5. $R_{DS(on)}$ vs. V_{GS} Figure 6. $R_{DS(on)}$ vs. I_D

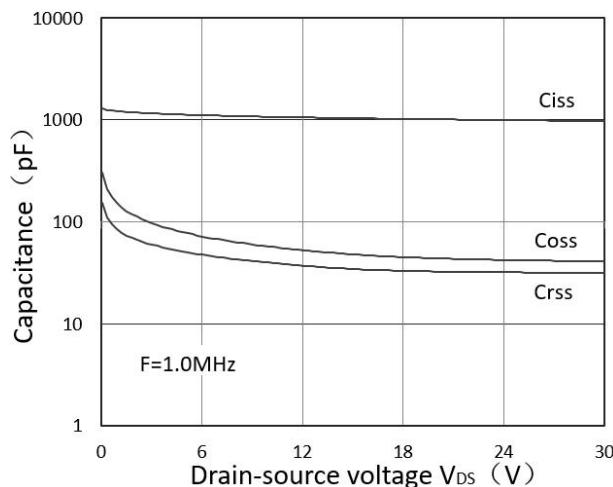


Figure 7. Capacitance Characteristics

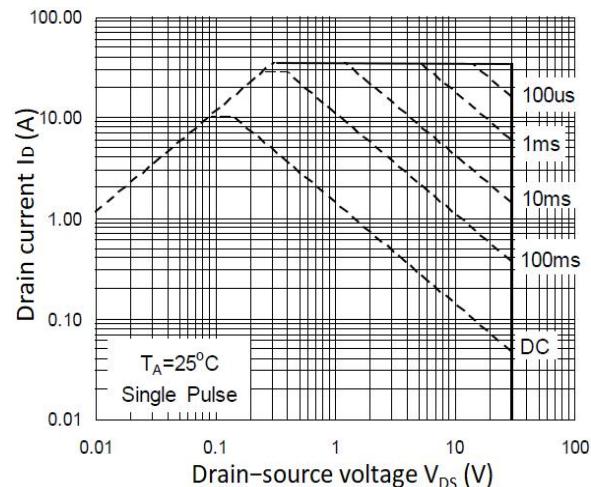


Figure 8. Safe Operating Area

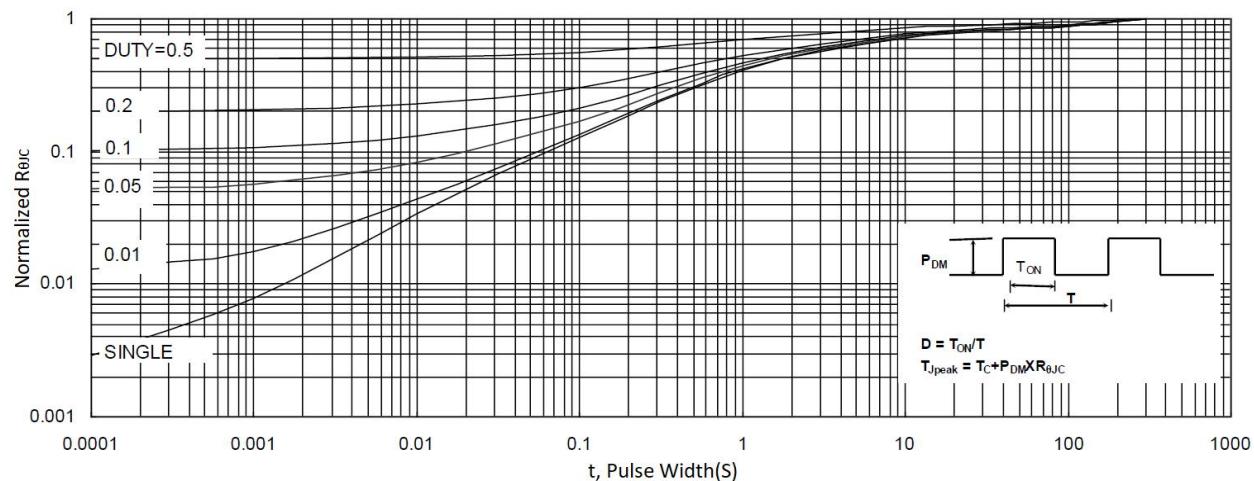


Figure 9. Normalized Maximum Transient Thermal Impedance

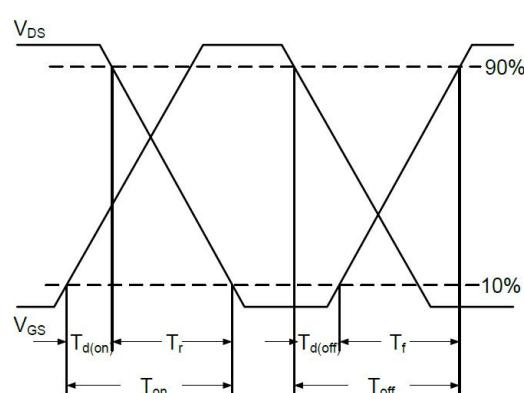


Figure 10. Switching Time Waveform

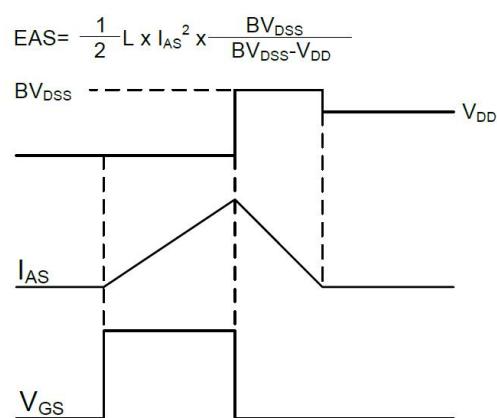


Figure 11. Unclamped Inductive Switching Waveform

Outline Drawing – DFN2020-6L

SYMBOL	MM	
	MIN	MAX
A	0.5	0.6
A1	0	0.05
A2	0.152REF	
b	0.25	0.35
D	1.95	2.05
D1	0.8	1
E	1.95	2.05
E1	0.8	1
L1	0.46	0.66
D2	0.25	0.35
e	0.65BSC	
L	0.25	0.35

Package Outline

The drawing shows the physical dimensions of the package. The top view indicates a square package with side length D and height E. The side view shows the thickness A and lead spacing A1. The cross-sectional view provides internal dimensions: lead width b, lead pitch L, lead height L1, and lead thickness e. The top view also includes a central marking '+'.

Ordering Information

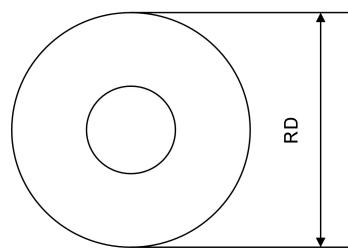
Part	Package	Marking	Packing method
EMR13N03M	DFN2020-6L	R13N03	Tape and Reel

Marking Information

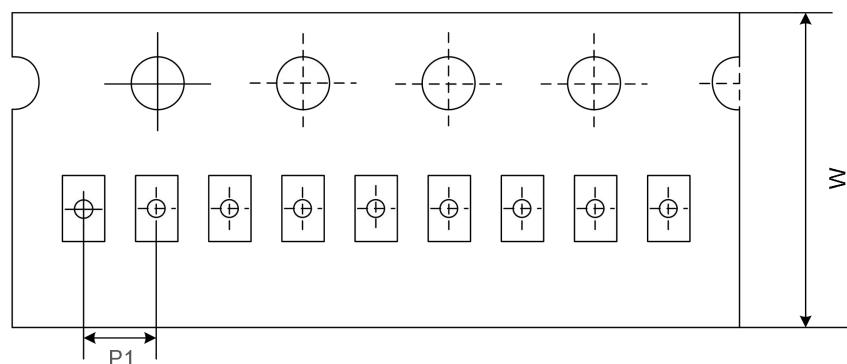
Part Number	Marking
EMR13N03M	<p>R13N03 WWXXXXXX</p> <p>R13N03= Device code WWXXXXXX= Tracking Number</p>

Tape Information

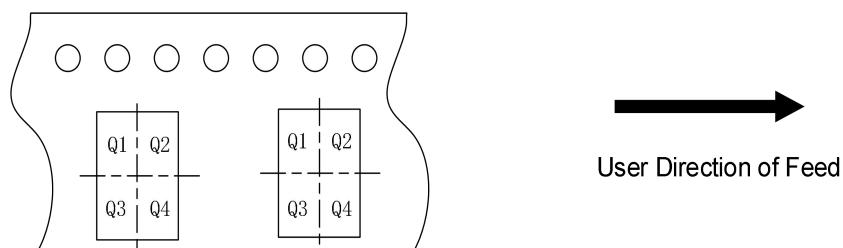
Reel Dimensions



Tape Dimensions

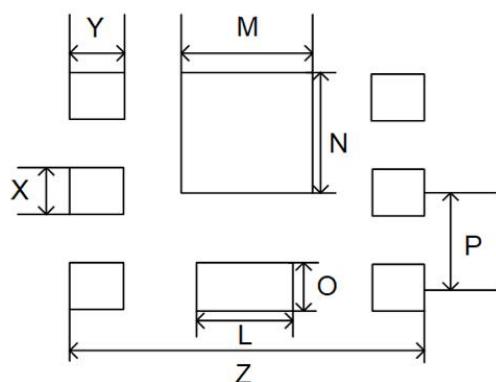


Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimensions	7 inch
W	Overall width of the carrier tape	8 mm
P1	Pitch between successive cavity centers	4 mm
Pin1	Pin1 Quadrant	Q2

DFN2020-6L RECOMMENDED LAND PATTERN



DIMENSIONS	
SYMBOL	MM
X	0.40
Y	0.425
M	1.15
N	0.95
L	0.80
O	0.48
P	0.65
Z	2.30

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.050\text{mm}$.
3. The pad layout is for reference purposes only.

Revision History

No.	Version	Date	Revision Item	Request	Function and characteristic checking	Package dimension checking	Typos checking
1	1.0	2020-09-22	Released Version	Qi Shu Kun	Qi Shu Kun	Liu Jia Ying	Liu Jia Ying
2	1.1	2020-11-4	Add Tape information and recommended land pattern	Qi Shu Kun	Qi Shu Kun	Liu Jia Ying	Liu Jia Ying
3	1.2	2021-3-19	Update Package size, marking and Qg graph	Qi Shu Kun	Qi Shu Kun	Liu Jia Ying	Liu Jia Ying
4	1.3	2021-6-23	Update recommended land pattern	Qi Shu Kun	Qi Shu Kun	Liu Jia Ying	Liu Jia Ying
5	1.4	2021-8-19	Update PIN1 Direction	Qi Shu Kun	Qi Shu Kun	Liu Jia Ying	Liu Jia Ying