

30V N-Channel Enhancement Mode Power MOSFET

Description

EMR12N03T1 uses advanced power trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

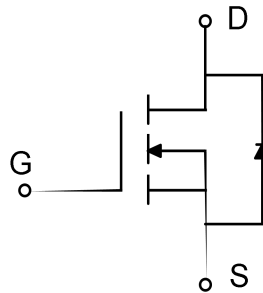
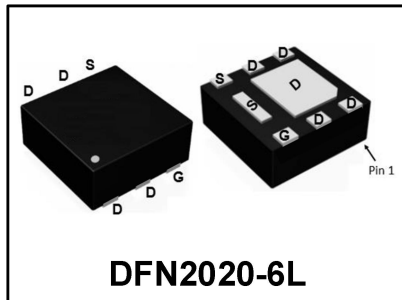
Features

- $V_{DS} = 30V$, $I_D = 12A$
 $R_{DS(on)} < 9m\Omega @ V_{GS} = 10V$
 $R_{DS(on)} < 12.5m\Omega @ V_{GS} = 4.5V$
- Green Device Available
- High Power and Current Handling Capability

Applications

- Battery Protection
- Power Management
- Load Switch

Schematic



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A = 25^\circ C$	I_D	12	A
	$T_A = 100^\circ C$		7	
Pulsed Drain Current ⁴		I_{DM}	48	A
Single Pulse Avalanche Energy ³		E_{AS}	20	mJ
Total Power Dissipation	$T_A = 25^\circ C$	P_D	2.1	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ¹	$R_{\theta JA}$	60	°C/W

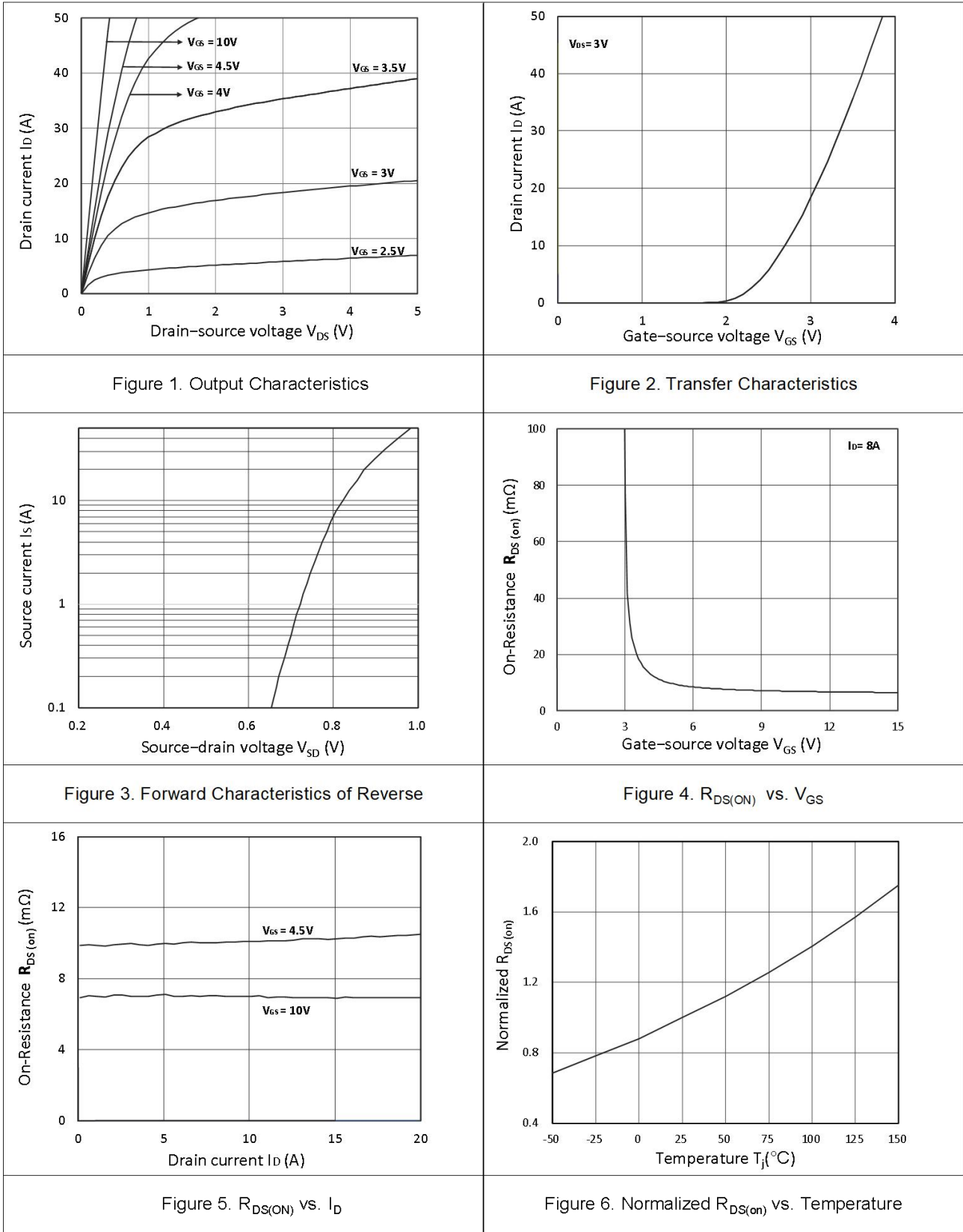
Electrical Characteristics T_c = 25°C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30	-	-	V
Gate-body Leakage current	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V	-	-	1	μA
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.6	2.5	V
Drain-Source on-Resistance ²	R _{DS(on)}	V _{GS} = 10V, I _D = 8A	-	6.8	9	mΩ
		V _{GS} = 4.5V, I _D = 6A	-	10	12.5	
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} = 15V, V _{GS} =0V, f=1.0 MHz	-	1250	-	pF
Output Capacitance	C _{oss}		-	174	-	
Reverse Transfer Capacitance	C _{rss}		-	142	-	
Switching Characteristics						
Gate Resistance	R _G	V _{DS} = 0V, V _{GS} =0V, f=1MHz	-	2.8	-	Ω
Total Gate Charge	Q _g	V _{GS} = 4.5V, V _{DS} = 15V, I _D =12A	-	10	-	nC
Gate-Source Charge	Q _{gs}		-	3.5	-	
Gate-Drain Charge	Q _{gd}		-	2.2	-	
Turn-on Delay Time	t _{d(on)}	V _{GS} =4.5V, V _{DS} =15V, I _D = 10A, R _G =3Ω	-	8	-	ns
Rise Time	t _r		-	28	-	
Turn-off Delay Time	t _{d(off)}		-	15	-	
Fall Time	t _f		-	7	-	
Drain-Source Body Diode Characteristics						
Diode Forward Voltage ²	V _{SD}	I _S = 1A, V _{GS} = 0V	-	-	1.2	V
Continuous Source Current ^{1,5}	I _S	V _G =V _D =0V , Force Current	-	-	12	A

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.1mH, I_{AS} = 20A$
4. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ C$.
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation

Typical Characteristics



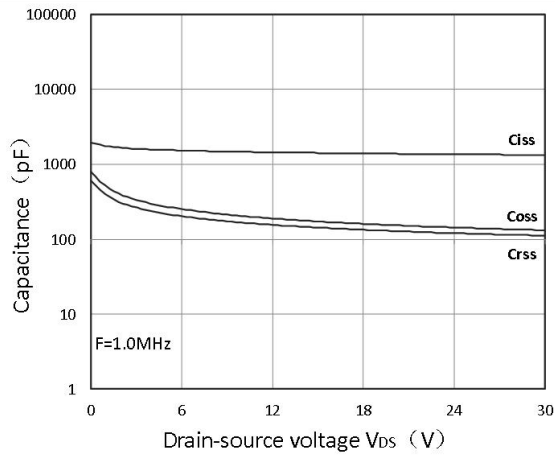


Figure 7. Capacitance Characteristics

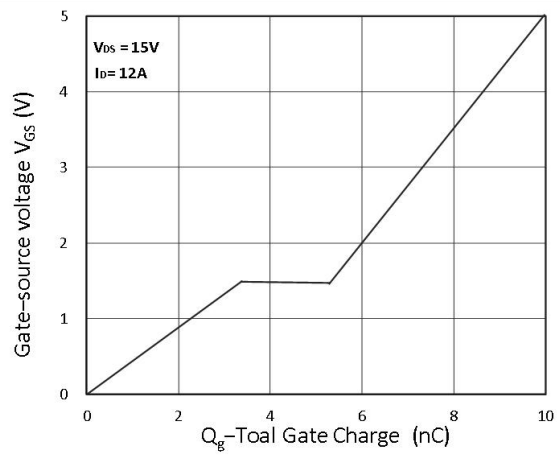


Figure 8. Gate Charge Characteristics

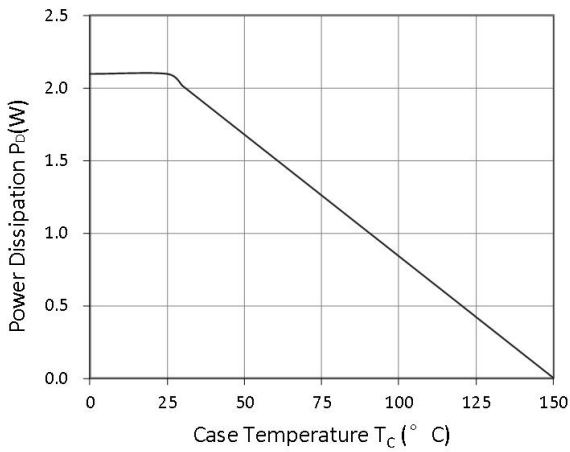


Figure 9. Power Dissipation

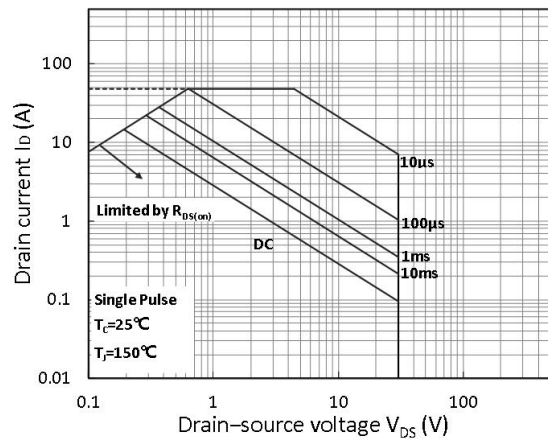


Figure 10. Safe Operating Area

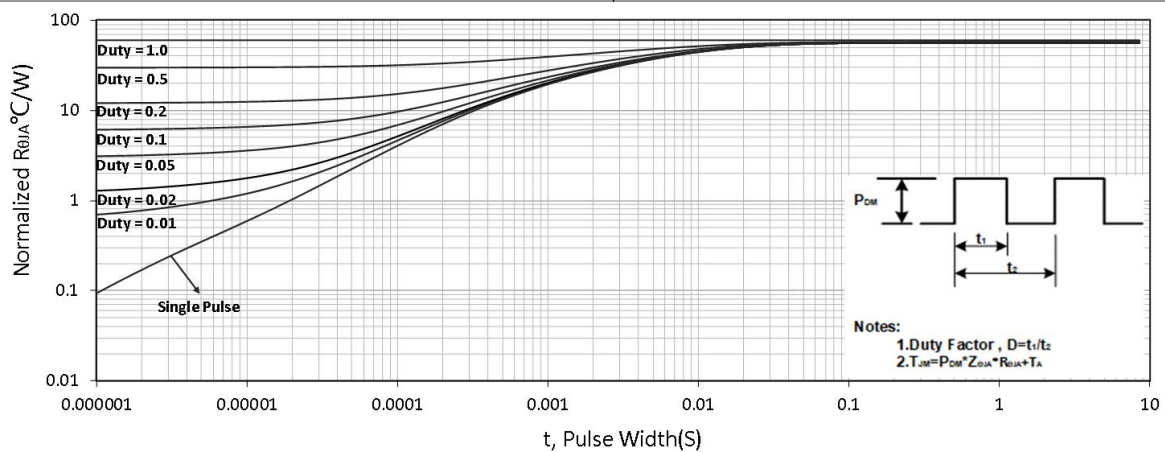


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

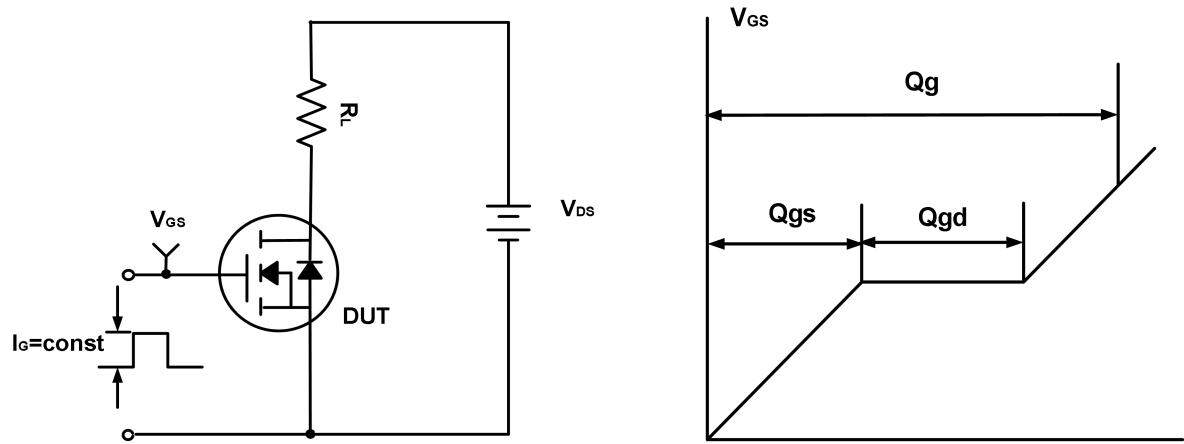


Figure A. Gate Charge Test Circuit & Waveforms

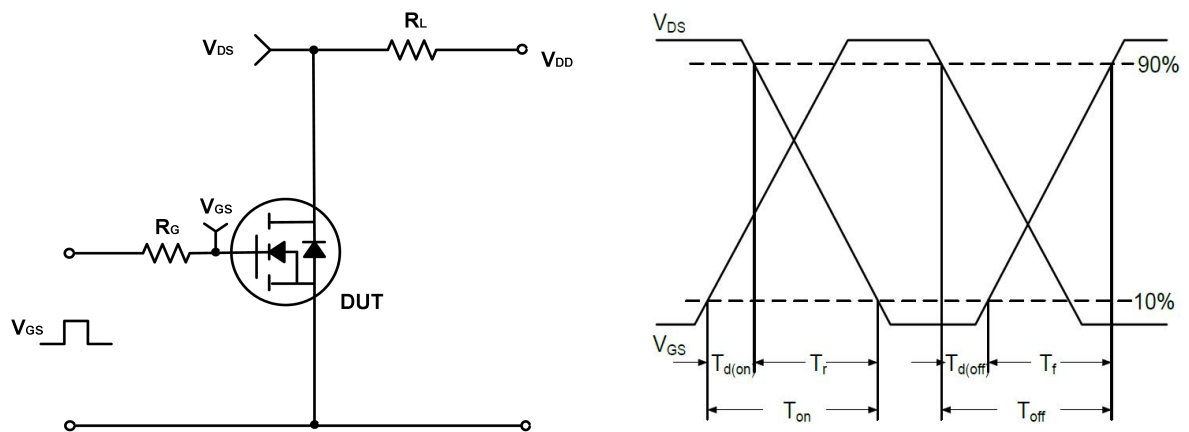


Figure B. Switching Test Circuit & Waveforms

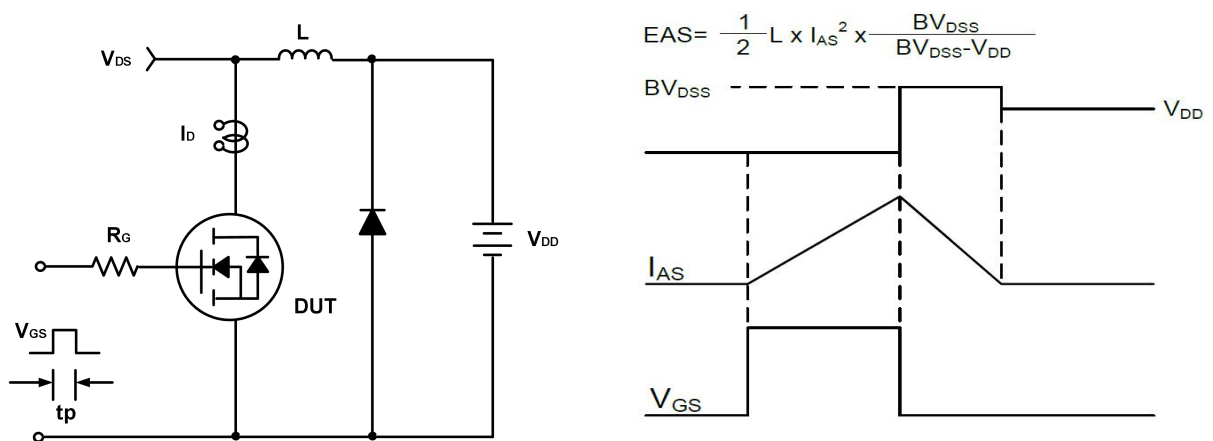
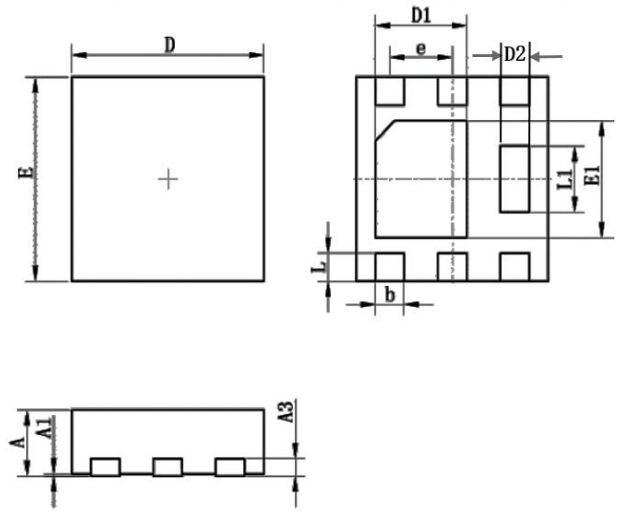
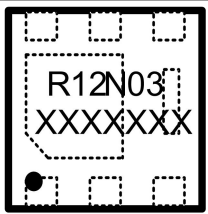


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Mechanical Dimensions for DFN2020-6L

PACKAGE OUTLINE	SYMBOL	MM	
		MIN	MAX
	A	0.50	0.60
	A1	0.00	0.05
	A3	0.152REF	
	b	0.25	0.35
	D	1.90	2.10
	D1	0.80	1.00
	E	1.90	2.10
	E1	0.80	1.00
	L1	0.46	0.66
	D2	0.25	0.35
	e	0.65BSC	
	L	0.25	0.35

Marking Information

Part No.	Marking	
EMR12N03T1		R12N03= Device code XXXXXXXX= Date code

Revision History

No.	Version	Date	Revision Item	Request	Function and characteristic checking	Package dimension checking	Typos checking
1	1.0	2020-05-08	Released Version	Qi Shu Kun	Qi Shu Kun	Liu Jia Ying	Liu Jia Ying