

30V N-Channel Enhancement Mode Power MOSFET

Description

EMR12N03TC uses advanced power trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

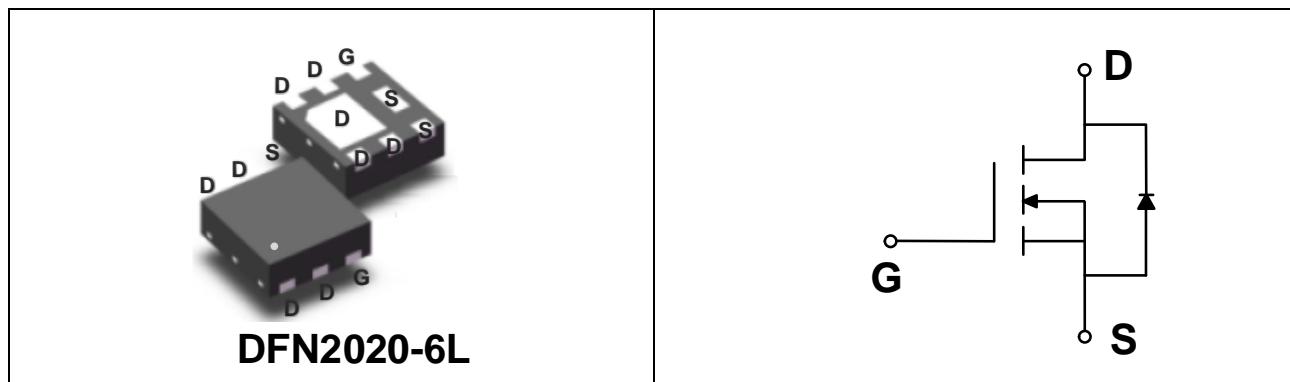
Features

- $V_{DS} = 30V$, $I_D = 12A$
- $R_{DS(on)} < 8.5m\Omega$ @ $V_{GS} = 10V$
- $R_{DS(on)} < 12.5m\Omega$ @ $V_{GS} = 4.5V$
- Green Device Available
- High Power and Current Handing Capability

Applications

- Battery Protection
- Power Management
- Load Switch

Schematic & PIN Configuration



EMR12N03TC

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current <small>$T_A=25^\circ\text{C}$</small>	I_D	12	A
		7.6	
Pulsed Drain Current ⁽¹⁾	I_{DM}	48	A
Single Pulse Avalanche Energy ⁽²⁾	EAS	45	mJ
Total Power Dissipation	P_D	2.2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction to Ambient ⁽³⁾	$R_{\theta JA}$	56.8	$^\circ\text{C}/\text{W}$

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Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	30	-	-	V
Gate-body Leakage Current	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 20\text{V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current $T_J=25^\circ\text{C}$ $T_J=100^\circ\text{C}$	I_{DSS}	$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 0\text{V}$	-	-	1	μA
			-	-	100	
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	1.0	1.5	2.0	V
Drain-Source on-state Resistance ⁽⁴⁾	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 8\text{A}$	-	6.5	8.5	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 6\text{A}$	-	9	12.5	
Dynamic Characteristics ⁽⁵⁾						
Input Capacitance	C_{iss}	$V_{\text{DS}} = 15\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$	-	1285	-	pF
Output Capacitance	C_{oss}		-	170	-	
Reverse Transfer Capacitance	C_{rss}		-	133	-	
Gate Resistance	R_g	$f = 1\text{MHz}$	-	2	-	Ω
Switching Characteristics ⁽⁵⁾						
Total Gate Charge	Q_g	$V_{\text{GS}} = 10\text{V}, V_{\text{DS}} = 15\text{V}, I_D = 8\text{A}$	-	23.5	-	nC
Gate-Source Charge	Q_{gs}		-	4.3	-	
Gate-Drain Charge	Q_{gd}		-	3.4	-	
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, V_{\text{DD}} = 15\text{V}, R_G = 3\Omega, I_D = 8\text{A}$	-	6.9	-	ns
Rise Time	t_r		-	2	-	
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	22.3	-	
Fall Time	t_f		-	5.2	-	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 8\text{A}, dI/dt = 100\text{A}/\mu\text{s}$	-	17	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	2.7	-	nC
Drain-Source Body Diode Characteristics						
Diode Forward Voltage ⁽⁴⁾	V_{SD}	$I_S = 1\text{A}, V_{\text{GS}} = 0\text{V}$	-	-	1.2	V
Continuous Source	$T_A = 25^\circ\text{C}$	I_S	-	-	12	A

Note1: Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$

Note2: The test condition is $V_{\text{DD}}=20\text{V}, V_{\text{GS}}=10\text{V}, L=0.4\text{mH}, I_{\text{AS}}=15\text{A}$.

Note3: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.

Note4: The data tested by pulsed , pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$.

Note5: This value is guaranteed by design hence it is not included in the production test.

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Typical Characteristics

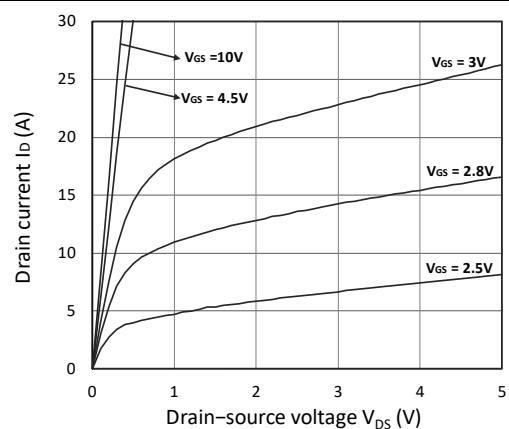


Figure 1. Output Characteristics

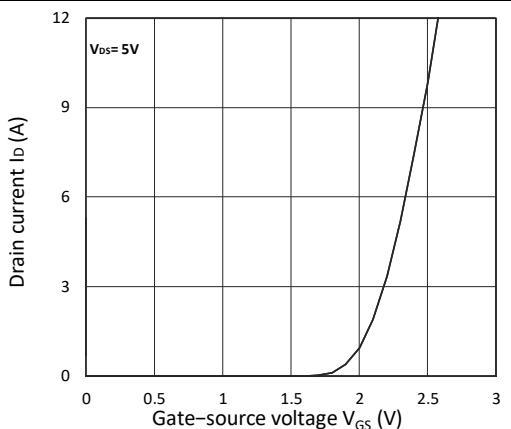


Figure 2. Transfer Characteristics

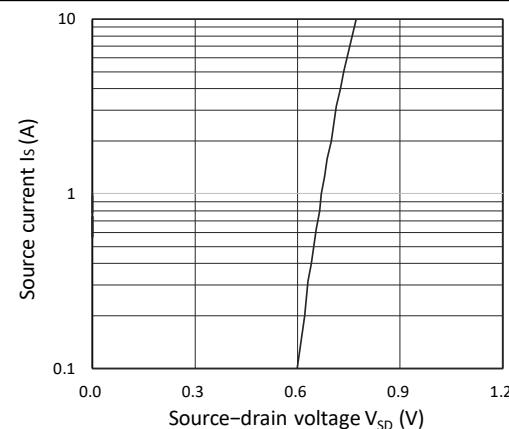


Figure 3. Forward Characteristics of Reverse

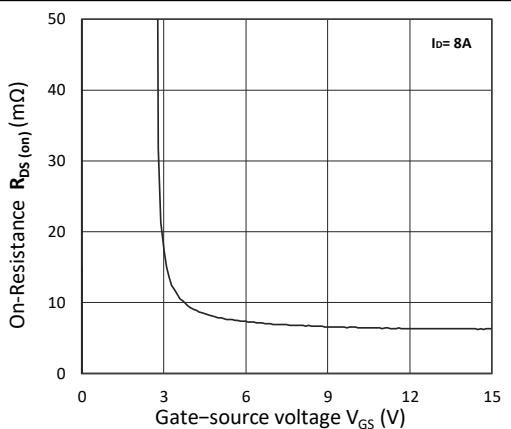


Figure 4. $R_{DS(on)}$ vs. V_{GS}

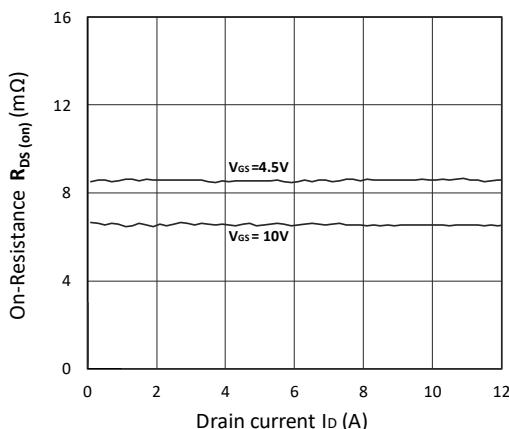


Figure 5. $R_{DS(on)}$ vs. I_D

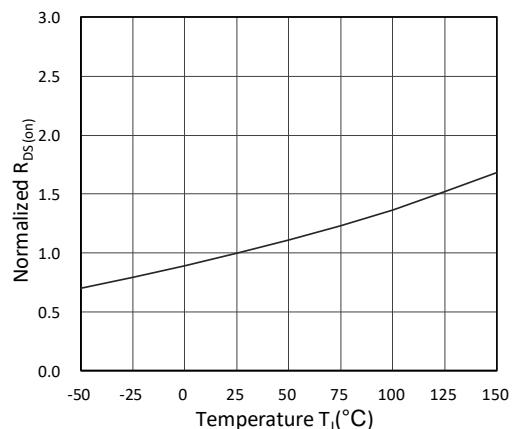
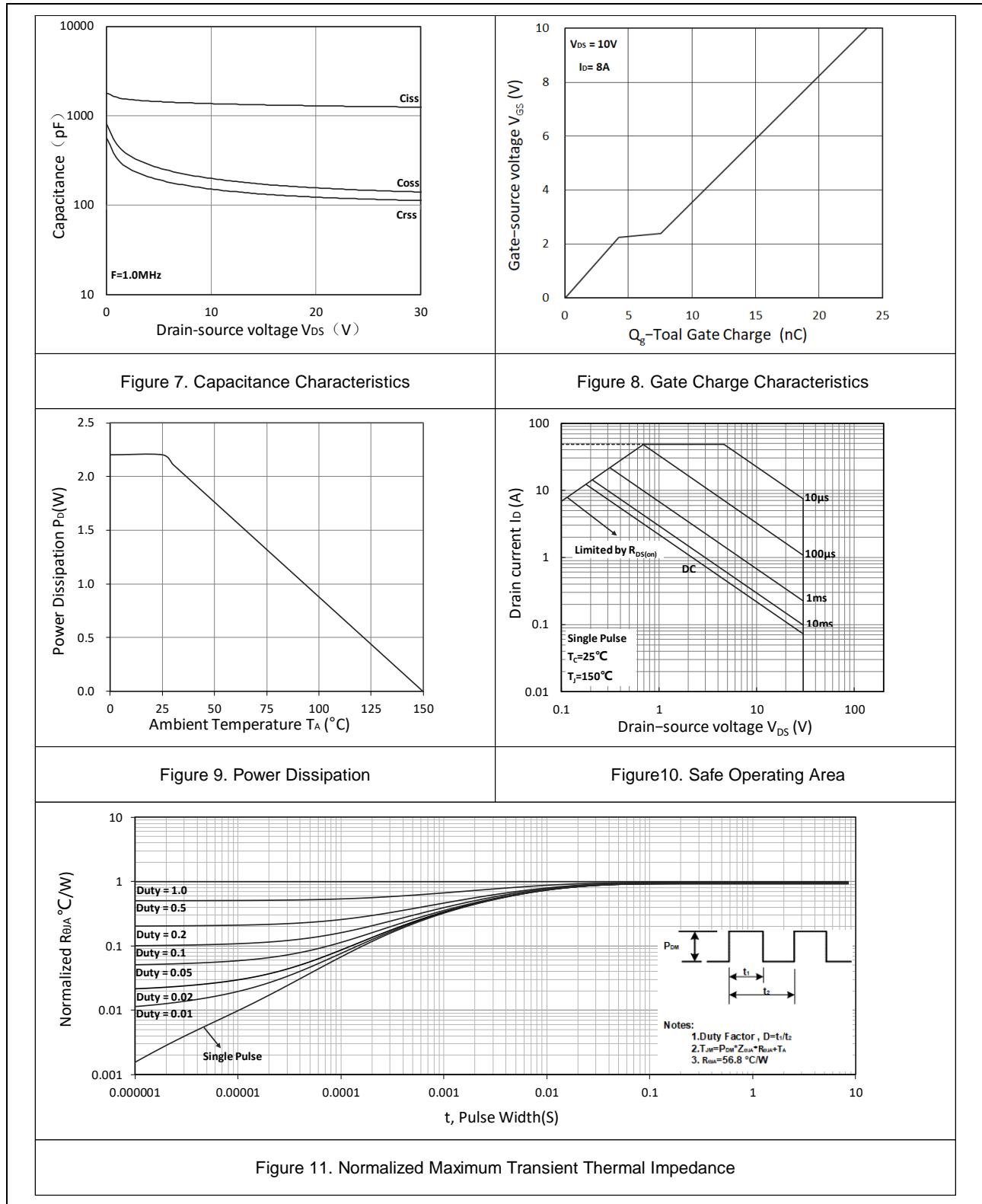


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

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Typical Characteristics(Continued)



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Test Circuit

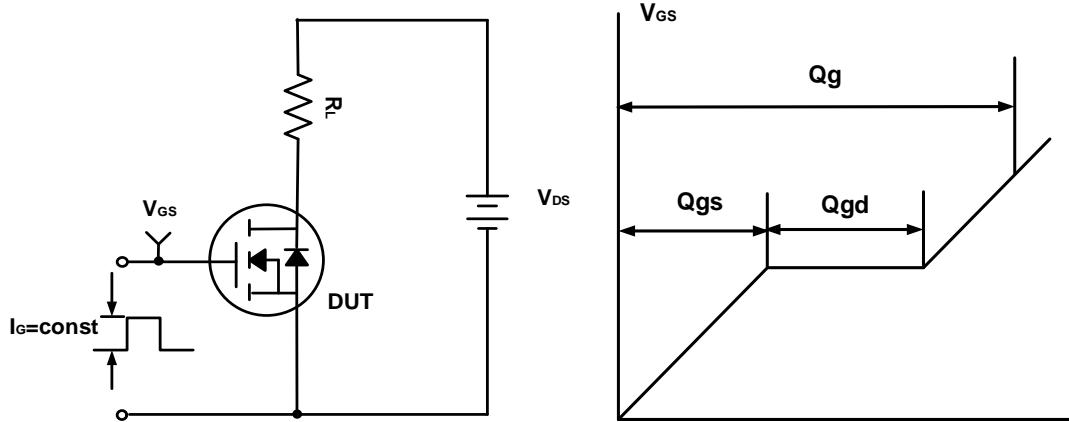


Figure A. Gate Charge Test Circuit & Waveforms

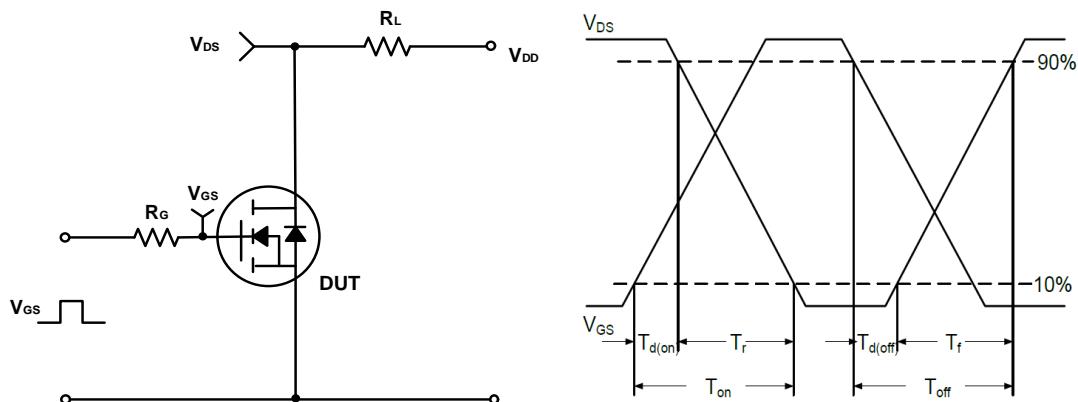


Figure B. Switching Test Circuit & Waveforms

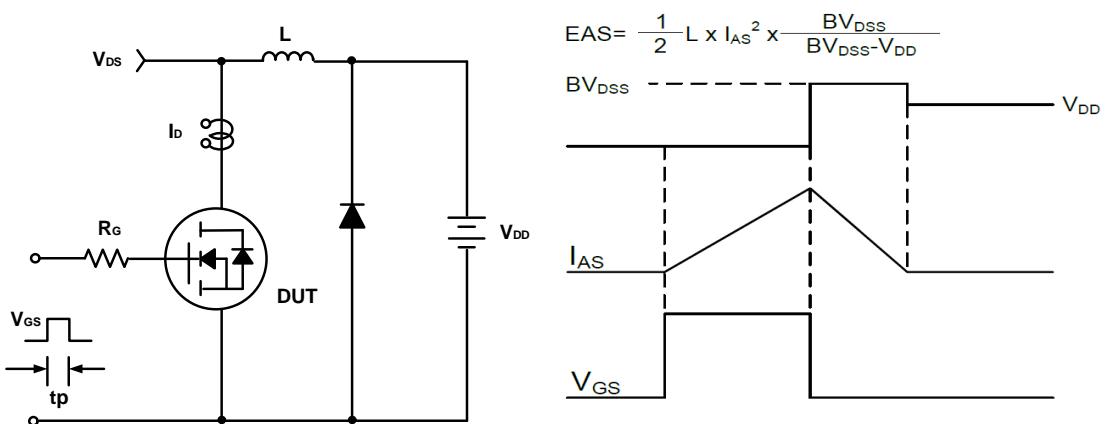


Figure C. Unclamped Inductive Switching Circuit & Waveforms

EMR12N03TC

Package Dimension

DFN2020-6L

SYMBOL	MILLIMETER	
	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
A3	0.152REF	
b	0.25	0.35
D	1.90	2.10
D1	0.80	1.00
E	1.90	2.10
E1	0.80	1.00
L1	0.46	0.66
e	0.65BSC	
D2	0.25	0.35
L	0.25	0.35

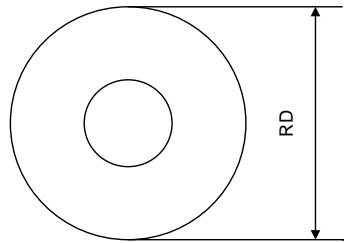
Ordering Information

Part	Package	Marking	Packing method	MPQ
EMR12N03TC	DFN2020-6L	R12N03C	Tape and Reel	3K/Reel

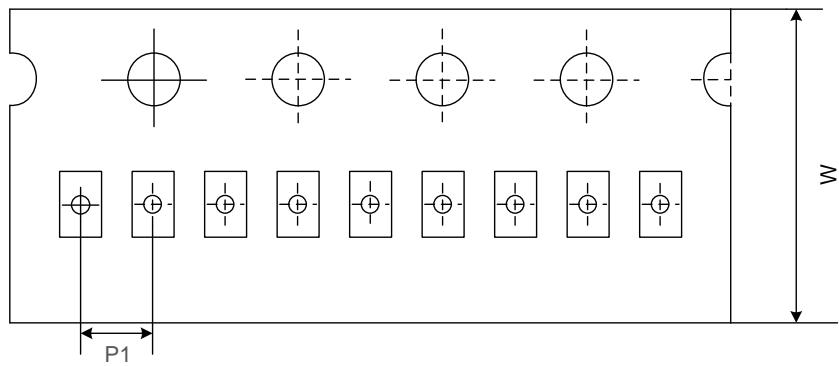
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Tape and Reel

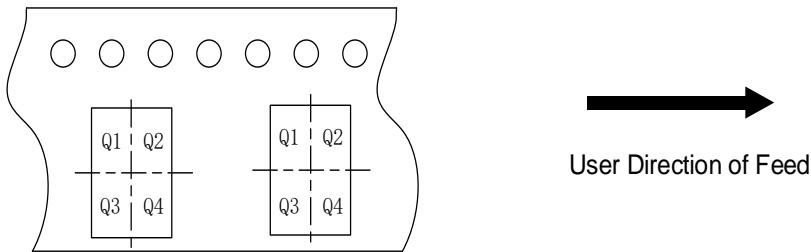
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimensions	7 inch
W	Overall width of the carrier tape	8 mm
P1	Pitch between successive cavity centers	4mm
Pin1	Pin1 Quadrant	Q1

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Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2023-08-16	Released Version	Chen Zu Xiong	Qi Shu Kun	Liu Jia Ying