



Features

- Solid-state silicon-avalanche technology
- Low operating and clamping voltage
- Up to two I/O Lines of Protection
- Ultra low capacitance
- Low operating voltage:5V
- Low Leakage Current

IEC COMPATIBILITY (EN61000-4)

- IEC 61000-4-2 (ESD) $\pm 20\text{kV}$ (air), $\pm 15\text{kV}$ (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning)4A (8/20 μs)

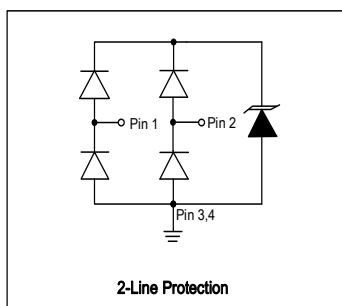
Mechanical Characteristics

- DFN1610-6L package
- Marking : Marking Code
- Packaging : Tape and Reel per EIA 481
- RoHS Compliant

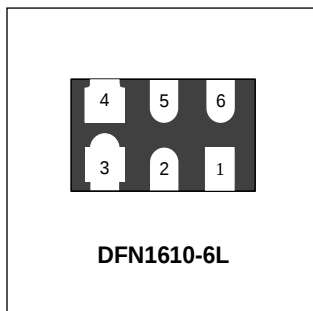
Applications

- Digital Visual Interface(DVI)
- MDDI Ports
- Display Port TM Interface
- PCI Express
- High Definition Multi-Media Interface(HDMI)
- HDMI Interfaces

Circuit Diagram



Schematic & PIN Configuration



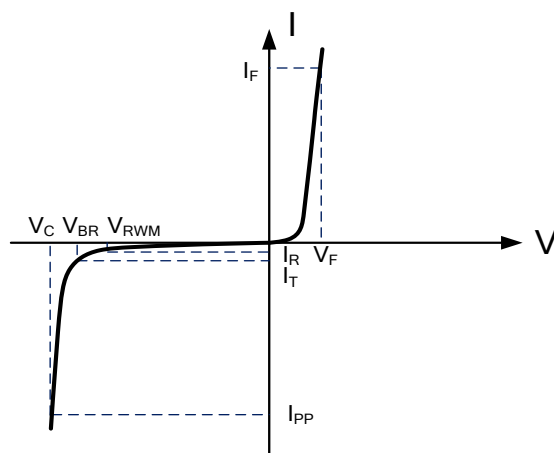
Pin	Identificaion
1,2	Input line
5,6	Output Lines (No Internal Connection)
3,4	Ground

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{PP}	48	Watts
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{PP}	4	A
Operating Temperature	T_J	-55 to + 125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Parameters (T=25°C)

Symbol	Parameter
I_{PP}	Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Reverse Stand-Off Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F



Electrical Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	$I_T=1mA$	6		9	V
Reverse Leakage Current	I_R	$V_{RWM}=5V$, $T=25^{\circ}C$			500	nA
Forward Voltage	V_F	$I_F=10mA$	0.6		1.2	V
Clamping Voltage	V_C	$I_{PP}=4A$, $t_p=8/20\mu s$		10.5	12	V
Dynamic Resistance ^{1,2}	R_{DYN}	TLP=0.2/100ns		0.34		Ω
ESD Clamping Voltage ¹	V_C	$I_{PP} = 4A$, $t_p = 0.2/100ns$ (TLP)		9.13		V
ESD Clamping Voltage ¹	V_C	$I_{PP} = 16A$, $t_p = 0.2/100ns$ (TLP)		13.2		V
Junction Capacitance	C_j	$V_R = 0V$, $f = 1MHz$ I/O pin to GND		0.5	0.7	pF
		$V_R = 0V$, $f = 1MHz$ Between I/O pins		0.25	0.35	pF

Notes : 1、 TLP Setting : $t_p=100ns$, $t_r=0.2ns$, I_{TLP} and V_{TLP} sample window: $t_1=70ns$ to $t_2=90ns$.

2、 Dynamic resistance calculated from $I_{PP}=4A$ to $I_{PP}=16A$ using “Best Fit”.

Typical Characteristics

Figure 1: Peak Pulse Power vs. Pulse Time

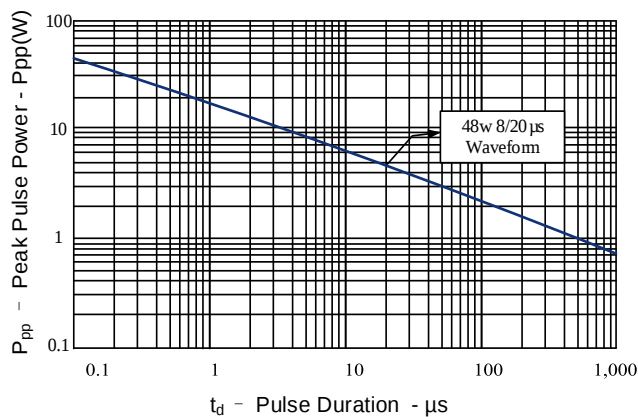


Figure 2: Power Derating Curve

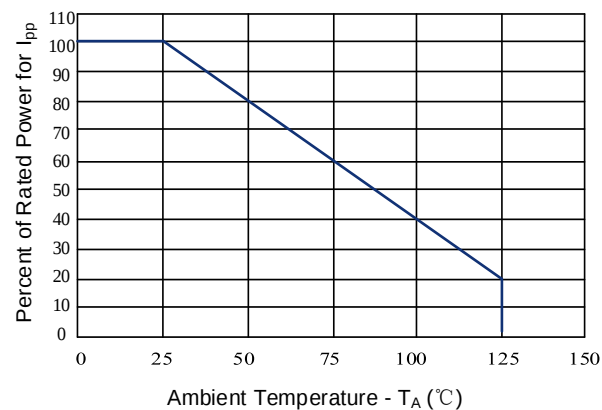


Figure 3: Clamping Voltage vs. Peak Pulse Current

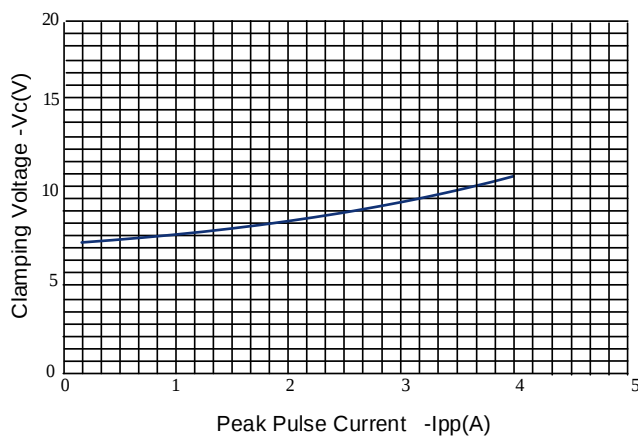


Figure 4: Normalized Junction Capacitance vs. Reverse Voltage

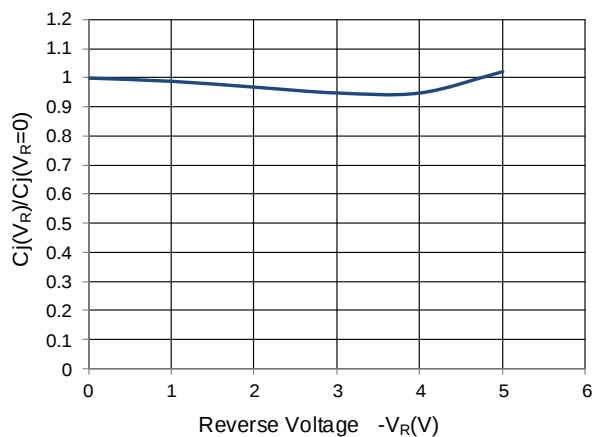


Figure 5: 8/20μs Pulse Waveform

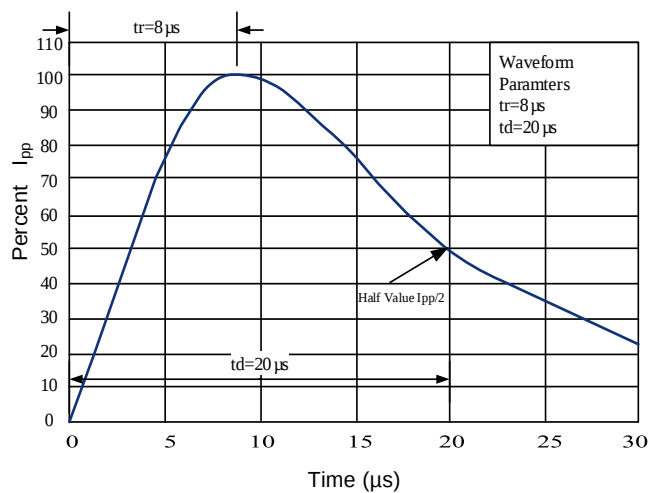
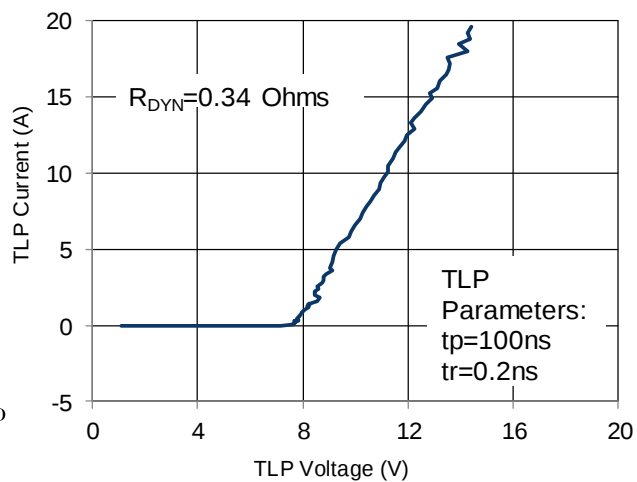


Figure 6: TLP I-V Curve



Outline Drawing – DFN1610-6L

DIMENSIONS				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D	1.55	1.65	0.061	0.065
E	0.95	1.05	0.037	0.041
L	0.33	0.43	0.013	0.017
b	0.15	0.25	0.006	0.010
b1	0.35	0.45	0.014	0.018
b2	0.25	0.35	0.010	0.014
e	0.50BSC		0.020BSC	
e1	1.00BSC		0.039BSC	
A	0.45	0.55	0.018	0.022
A1	0.15REF		0.006REF	
A2	0.00	0.05	0.000	0.002

DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	0.024	0.60
G	0.004	0.10
P	0.020	0.50
P1	0.039	1.00
X	0.012	0.30
Y	0.020	0.50
Y1	0.043	1.10

Notes:
Controlling Dimension: Millimeter.

Marking Codes

Part Number	Marking Code
ES052R2PL	2R2P

Package Information

Qty: 10k/Reel

Revision History

No.	Version	Date	Revision Item	Request	Function and characteristic checking	Package dimension checking	Typos checking
1	1.0	2019-10-15	Released Version	Qi Shu Kun	Qi Shu Kun	Liu Jia Ying	Liu Jia Ying