1.5A Inductorless Flash LED Driver with I²C Control

General Description

ET93011 is a inductorless LED flash driver that provides a high level of adjust-ability within a ultra-small size. It can produce up to 1.5A of LED flash current. The 128 levels current source provides the flexibility to adjust the current ratios in Flash/Torch/IR modes. An adaptive regulation method ensures the current source remain in regulation and maximizes efficiency. It also provides IVFM protection mode to prevent system reset or shutdown under low battery condition.

ET93011 are controlled via an I²C compatible interface. These features include: flash/torch current, flash timeout duration, IVFM, under-voltage Protection. The device offers programmable currents in a Flash or Movie Mode (Torch) condition, and also provides hardware flash pin (STROBE) to control Flash events.

ET93011 is available in WLCSP8 package and operates ambient temperature range of -40℃ to +85℃.

Features

- Accurate and programmable LED currents
  - Flash current range from 11mA to 1.5A
  - Torch current range from 2.4mA to 375mA
- Flash timeout values up to 1.6 seconds
- Optimized flash LED current during low battery conditions
- Grounded cathode LED operation for improved thermal management
- Hardware strobe enable
- Synchronization Input for RF Power Amplifier Pulse Events(TX)
- 400KHz I²C compatible interface
- Under-voltage protection
- LED/VOUT short circuit protection
- Less than 1uA shutdown current
- Package: WLCSP(1.49mm × 0.8mm)

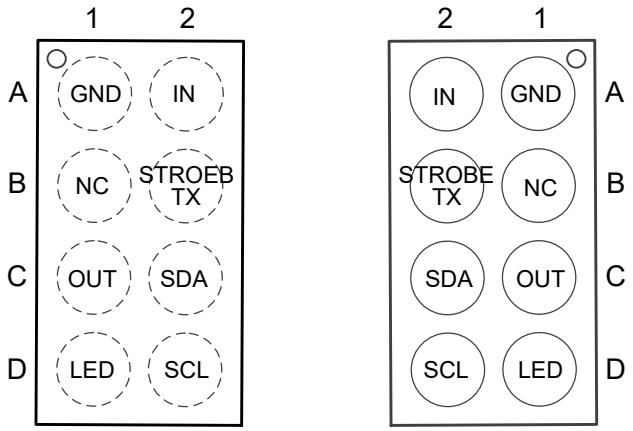
Application

- Flash/torch/video light for smart phones, feature-phones, tablets, DSCs, DVCs
- IR LED Driver
- Video Surveillance:
- IP Camera
- Barcode Scanner
- Portable Data Terminal

Device Information

Part No.	Package	Size	MSL
ET93011	WLCSP	1.49mm × 0.8mm	Level 1

Pin Assignments



Top View Bottom View

Figure 1. Pin Assignments

Pin Function

Pin No.	Name	I/O	Function
A1	GND	Ground	Ground
A2	IN	Power	Input voltage connection. Connect IN to the input supply and bypass to GND with a 10μF or larger ceramic capacitor.
B1	NC	-	-
B2	STROBE/TX	I	Active high hardware flash enable for drive STROBE high to turn on flash pulse or Configurable dual polarity power amplifier synchronization input. An internal pull-down resistor of 300 kΩ between STROBE/TX and GND
C1	OUT	Power	Step-up DC-DC converter output. Connect a 10-μF ceramic capacitor between this pin and GND.
C2	SDA	I/O	I^2C serial data input/output.
D1	LED	Power	High-side current source output for flash LED.
D2	SCL	I	I^2C serial clock input.

Block Diagram

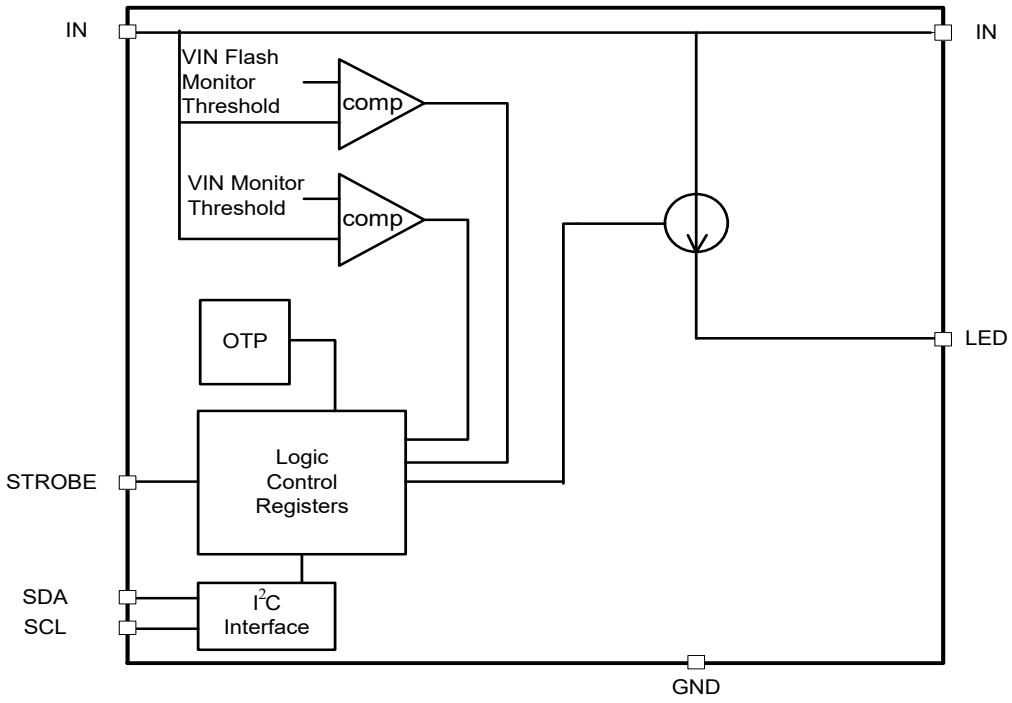


Figure 2. Block Diagram

Functions Description

ET93011 is a high-power white LED flash driver capable of delivering up to 1.5A to the LED current over the 2.5V to 5.5V input voltage range.It has one logic input for a hardware Flash Enable (STROBE pin). This logic input has internal 300kΩ (typical) pull-down resistors to GND.

Control is done via an I^2C compatible interface. This includes adjustment of the Flash and Torch current levels, changing the Flash Timeout Duration. Additionally, there are flags and status bits that indicate flash current timeout, LED over-temperature condition, LED failure (open and short), device thermal shutdown, thermal current scale-back, VIN under-voltage condition.

Flash Mode

In Flash Mode, the LED current source provides 128 target current levels from 11mA to 1.5A. The Flash currents are adjusted via the LED Flash Brightness Register. Flash mode is activated by the Enable Register (setting M1, M0 to '11'), or by pulling the STROBE pin HIGH when the pin is enabled (Enable Register). Once the Flash sequence is activated, the LED current source ramps up to the programmed Flash current by stepping through all current steps until the programmed current is reached. The headroom on the current source is regulated to provide 11mA to 1.5A.

When the device is enabled in Flash Mode through the Enable Register, the mode bits in the Enable Register are cleared after a flash timeout event.

Torch Mode

In Torch mode, the LED current source provide 128 target current levels from 2.4mA to 375mA on ET93011. The Torch currents are adjusted via the LED Torch Brightness Register. Torch mode is activated by the Enable Register (setting M1, M0 to '10'). Once the TORCH sequence is activated, the LED current source ramps up to the programmed Torch current by stepping through all current steps until the programmed current is reached. The rate of the current ramps is determined by the value chosen in the Torch Ramp bit [0] in Timing Register(0x02).

Torch Mode is not affected by Flash Timeout.

IR Mode

In IR Mode, the target LED current is equal to the value stored in the LED Flash Brightness Register. When IR mode is enabled (setting M1, M0 to '01'), at this point, toggling the STROBE pin enables and disables the LED current source. The strobe pin can only be set to be Level sensitive, meaning all timing of the IR pulse is externally controlled. In IR Mode, the current source do not control the ramp rate of the LED output.

The current transitions immediately from off to on and then on to off.

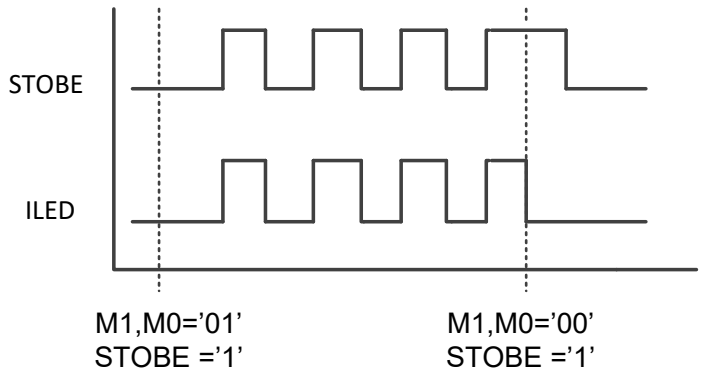


Figure 3. IR Mode

When the flash timer elapses, the device goes into stand-by regardless of strobe state, see in Figure 4.

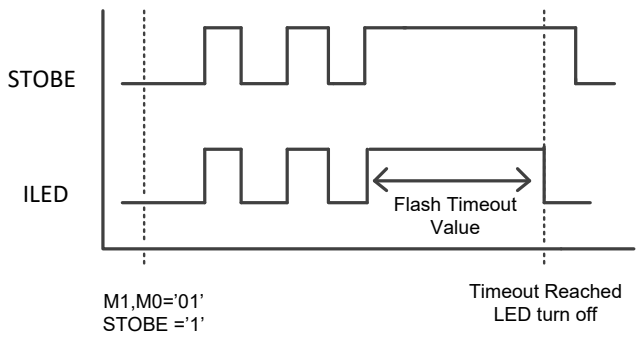


Figure 4. IR Mode Timeout

Soft Start-up

Turn on of the ET93011 Torch and Flash modes can be done through the Enable Register. At turn-on the current source steps through each FLASH or TORCH level until the target LED current is reached. This gives the device a controlled turn-on and limits inrush current from the VIN supply. The target LED flash and the target LED torch currents are set by the LED Flash Brightness Register (0x03 bits [6:0]) and LED Torch Brightness Register (0x04 bits [6:0]) respectively.

Power Amplifier Synchronization (TX)

The STROBE/TX pin, when set to TX mode, serves as a Power Amplifier Synchronization input. This is designed to reduce the flash LED current and thus limit the battery current during high battery current conditions such as PA transmit events. When the ET93011 is engaged in Internal Flash event, and the TX pin is pulled high, the LED current is forced into Torch Mode at the programmed Torch current setting. If the TX pin is then pulled low before the Flash pulse terminates, the LED current returns to the previous Flash current level. At the end of the Flash time-out, whether the TX pin is high or low, the LED current turns off.

Additionally, The TX mode can be enable by setting bit [6] of 0x06 Register (TX Enable) to ‘1’. TX Interrupt event is only valid to the internal flash mode (R01 bits [1:0], M1, M0=11).Once TX is enable, the externally Flash and IR mode are not valid.

After TX Interrupt event, TX flag (bit [5] of 0x06 Register) is set .Upon an I2C read of the 0x06 register, the TX flag is cleared.

Input Voltage Flash Monitor (IVFM)

The ET93011 has the ability to adjust the flash current based upon the voltage level present at the IN pin utilizing the Input Voltage Flash Monitor (IVFM). The adjustable threshold ranges from 2.9 V to 3.6 V in 100mV steps .The IVFM threshold is controlled by bits [7:5], in the configuration Register (0x02). The Flag Register has the IVFM flag bit set when the input voltage crosses the IVFM threshold value. Additionally, the IVFM threshold sets the input voltage boundary that forces the ET93011 to stop ramping and hold the flash current during startup.

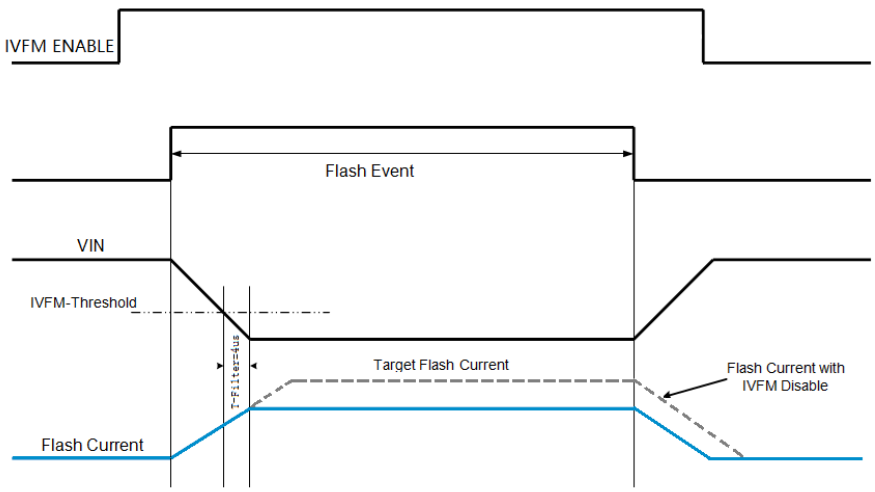


Figure 5. IVFM Modes

Flash Timeout

The Flash Timeout period sets the maximum time of one flash event, whether a flash stop command is received or not. The ET93011 has 16 timeout levels ranging from 40ms to 1.6s (see 0x02 bits [4:1] for more detail).

Under Voltage Lock Output (UVLO)

The ET93011 has an internal comparator that monitors the voltage at IN and forces the ET93011 into standby if the input voltage drops to 2.5V. If the UVLO monitor threshold is tripped, the UVLO flag bit is set in the Flags Register. If the input voltage rises above 2.5V, the ET93011 is not available for operation until there is an I²C read of the Flags Register. Upon an I²C read of the Flags register, the Flags register is cleared, and normal operation can resume if the input voltage is greater than 2.5V.

LED Short Fault

The LED Short Fault flag read back a '1' if the device is active in Flash or Torch mode and either active LED output experiences a short condition. An LED short condition is determined if the voltage at LED goes below 500mV (typ.) while the device is in Torch or Flash mode. There is a deglitch time of 256us before the LED Short Fault flag is valid. The mode bits are cleared upon an LED short fault. The LED short fault can be reset to 0 by removing power to the ET93011, or setting the software reset field (Register 0x06 bit [7]) to a 1, or by reading back the Flag Register.

Thermal Scale-Back (TSB)

When the ET93011 die temperature reaches 125° C, the thermal scale-back (TSB) circuit trips and TSB flag (bit [2]) of Flags Register (0x05) is set. The LED current then shifts to torch current level, set by the LED Torch Brightness Register (0x04 bits [6:0]) for the duration of the flash pulse, set by the flash time-out in the Configuration Register (0x02 bits [4:1]). After I²C read of the Flags Register and upon re-flash, if the die temperature is still above 125° C, the ET93011 re-enters into torch current level and sets the TSB flag bit again.

Thermal Shutdown (TSD)

When the ET93011 die temperature reaches 150° C, the thermal shutdown detection circuit trips, forcing the ET93011 into standby and writing a '1' to the Thermal Shutdown Fault flag of the Flags Register . The ET93011 restarts only after the Flags Register is read, which clears the fault flag. Upon restart, if the die temperature is still above 150° C, the ET93011 resets the TSD flag and re-enters standby.

Programming

I²C Interface

I²C Compatible Chip Address

The device address for the ET93011 is 1100100 (0x64). After the START condition, the I²C compatible master sends the 7-bit address followed by an eighth read or write bit (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data is written. The third byte contains the data for the selected register.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Acknowledge

ACK means the successful transfer of I^2C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I^2C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I^2C stop.

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

(1). Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

(2). Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

(3). Slave device sends acknowledge signal if the slave address is correct.

(4). Master sends control register address (8-bit)

(5). Slave sends acknowledge signal

(6). Master sends data byte to be written to the addressed register

(7). Slave sends acknowledge signal

(8). If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step 6, 7)

(9). Master generates STOP condition to indicate write cycle end

I²C Writing Command Register Interface Protocol (single)：

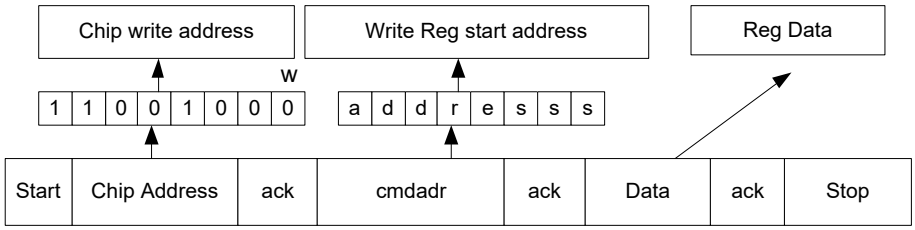


Figure 6. I²C Writing Command Register Protocol (single)

I²C Writing Command Register Interface Protocol (continuous)：

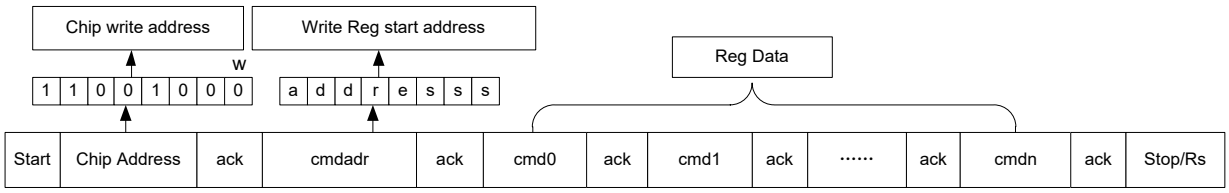


Figure 7. I²C Writing Command Register Protocol (continuous)

Read Cycle

In a read cycle, the following steps should be followed:

(1). Master device generates START condition

(2). Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

(3). Slave device sends acknowledge signal if the slave address is correct.

(4). Master sends control register address (8-bit)

(5). Slave sends acknowledge signal

(6). Master generates STOP condition followed with START condition or REPEAT START condition

(7). Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

(8). Slave device sends acknowledge signal if the slave address is correct.

(9). Slave sends data byte from addressed register.

(10). If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

(11). If the master device generates STOP condition, the read cycle is ended.

I²C Reading Command Register Interface Protocol(single)

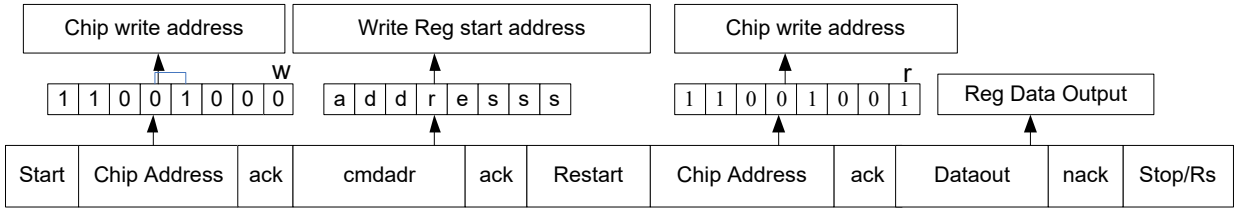


Figure 8. I²C Reading Command Register Interface Protocol(single)

I²C Reading Command Register Interface Protocol(continuous)

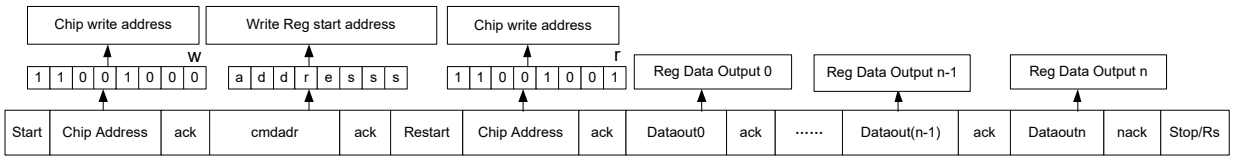


Figure 9. I²C Reading Command Register Interface Protocol(continuous)

Register Descriptions

Addr	Reg Name	Type	Reset-Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x01	Enable	R/W	20	RFU	RFU	RFU	IVFM_EN	STROBE_TYPE	STROBE_EN	MODE[1:0]	
0x02	Config	R/W	15	IVFM_LEVEL [2:0]			FLASH_TIMEOUT[3:0]				TORCH_RAMP
0x03	LED_F	R/W	80	TSB	LED_FBRIGHT[6:0]						
0x04	LED_T	R/W	00	RFU	LED_TBRICHT[6:0]						
0x05	Flags	R/W	00	RFU	F_IVFM	F_SHORT	RFU	F_TSB	F_TSD	F_UVLO	F_TIMEOUT
0x06	Chip_ID	R/W	29	SOFT_RST	TX_EN	Device ID[2:0]			F_TX	Silicon Revision Bits[1:0]	

Register Detailed Description

Address: 0x01h-- Enable Register

Bit	Name	Description	
7		**RFU**	
6		**RFU**	
5		**RFU**	
4	IVFM_EN	**IVFM Enable**	
		0 = Disabled (Default)	1 = Enabled
3	STROBE_TYPE	**Strobe Type**	
		0 = Level Triggered (Default)	1 = Edge Triggered
2	STROBE_EN	**Strobe Enable**	
		0 = Disabled (Default)	1 = Enabled
1: 0	MODE[1:0]	**Mode Bits: M1, M0**	
		00 = Standby (Default)	01 = IR Drive
		10 = Torch	11 = Flash

Control Truth Table

MODE1	MODE0	STROBE EN	STROBE PIN	ACTION
0	0	0	X	Standby
0	0	1	Pos edge	Ext Flash
1	0	X	X	Int Torch
1	1	X	X	Int Flash
0	1	0	X	IR LED Standby
0	1	1	0	IR LED Standby
0	1	1	Pos edge	IR LED enabled

Address: 0x02h-- Configuration Register

Bit	Name	Description	
7:5	IVFM_LEVEL[2:0]	**IVFM Levels (IVFM-D)**	
		000 = 2.9 V (Default)	001 = 3 V
		010 = 3.1 V	011 = 3.2 V
		100 = 3.3V	101 = 3.4 V
		110 = 3.5V	111 = 3.6V
4:1	FLASH_TIMEOUT[3:0]	**Flash Time-out Duration**	
		0000 = 40 ms	0001 = 80 ms
		0010 = 120 ms	0011 = 160 ms
		0100 = 200 ms	0101 = 240 ms
		0110 = 280 ms	0111 = 320 ms

		1000 = 360 ms	1001 = 400 ms
		1010 = 600 ms (Default)	1011 = 800 ms
		1100 = 1000 ms	1101 = 1200 ms
		1110 = 1400 ms	1111 = 1600 ms
0	TORCH_RAMP	**Torch Ramp**	
		0 = No Ramp	1 = 1 ms (Default)

Address: 0x03h-- LED Flash Brightness Register

Bit	Name	Description	
7	TSB	**Thermal Current Scale-Back** If enabled, LED current shifts to torch current level if TJ reach 125℃	
		0 = Disabled	1 = Enabled (Default)
6:0	LED_FBRIGHT[6:0]	**LED Flash Brightness Level**	
		0000000 = 11mA (Default)	0010101 (0x15) = 0.257A .....
		0111111 (0x3F) = 0.75A	0101111 (0x5F) = 1.03A .....
		1100110 (0x66) = 1.2A	1111111 (0x7F) = 1.5A

Address: 0x04h--LED Torch Brightness Register

Bit	Name	Description	
7		**RFU**	
6:0	LED_TBRICHT[6:0]	**LED Torch Brightness Levels**	
		0000000 = 2.4mA (Default)	0010101 (0x15) = 64mA .....
		0111111 (0x3F) = 188mA	0101111 (0x5F) = 258mA .....
		1100110 (0x66) = 302mA	1111111 (0x7F) = 375mA

Address: 0x05h--Flags Register

Bit	Name	Description
7		**RFU**
6	F_IVFM	IVFM Trip Flag
5	F_SHORT	V_{OUT} / V_{LED} Short Fault
4		**RFU**
3	F_TSB	Thermal Current Scale-back (TSB) Flag
2	F_TSD	Thermal Shutdown (TSD) Fault
1	F_UVLO	UVLO Fault
0	F_TIMEOUT	Flash Time-Out Flag

Address: 0x06h--Device ID and RESET Register (0x06)

Bit	Name	Description	
7	SOFT_RST	**Software RESET**	
		0 = Normal (Default)	1 = Force device RESET
6	TX_EN	**TX Enable**	
		0 = Disabled (Default)	1 = Enabled
5:3	Device ID	101 (Default)	
2	F_TX	**TX Flag:**	
		0 = Normal(Default)	1 = TX-mode
1:0	Silicon Revision Bits	01 (Default)	

Absolute Maximum Ratings

Symbol	Item	Rating	Unit
V_{IN} V_{LED}	IN, LED	-0.3 to 6.0	V
V_{IO}	SDA, SCL, STROBE/TX	-0.3 to V_{IN}+0.3	V
I_{MAX}	Continuous Power Dissipation	Internally limited	mA
θ_{JA}	Thermal Resistance, Junction-to-Ambient	130	˚C/W
T_J	Operating Junction Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-65 to 150	˚C
T_{SOLD}	Lead Temperature (Soldering, 10 sec)	300	˚C
V_{ESD}	HMB (JEDEC JS-001)	±4000	V
	CDM (JESD22-C101)	±1000	V

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Parameter	Min	Max	Unit
V_{IN}	2.5	5.5	V
Junction Temperature (T_J)	-40	125	˚C
Ambient Temperature (T_A)	-40	85	

Electrical Characteristics

(Unless otherwise noted, V_{DD}=5V ,T_A=25˚C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IC SUPPLY						
V_{IN}	Input Voltage Range		2.5		5.5	V
V_{UVLO}	Under-Voltage Lockout Threshold	Rising edge	2.4	2.5	2.6	V
$V_{UVLOhys}$	Under-Voltage Lockout Hysteresis			0.05		V
I_Q	Supply Current	Not switching		300		uA
I_{SB}	Standby Supply Current	Device disable 2.5 V ≤ V_{IN} ≤ 5.5 V		0.8	4	uA
V_{IVFM}	Input Voltage Flash Monitor Trip Threshold	Reg 0x02, bits [7:5] = '000'	- 3%	2.9	3%	V
CURRENT SOURCE SPECIFICATIONS						
I_{LED}	Current Source Accuracy	V_{OUT} = 4 V, flash code = 0x7F = 1.5 A	- 10%	1.5	10%	A
		V_{OUT} = 4 V, torch code = 0x7F =375mA	- 10%	375	10%	mA
V_{SHORT}	LED Short Checking Voltage			500		mV
STROBE/TX VOLTAGE SPECIFICATIONS						
V_{IL}	Input Logic Low	2.5 V ≤ V_{IN} ≤ 5.5 V			0.4	V
V_{IH}	Input Logic High	2.5 V ≤ V_{IN} ≤ 5.5 V	1.2			V
I²C-COMPATIBLE INTERFACE SPECIFICATIONS (SCL, SDA)						
V_{IL}	Input Logic Low	2.5 V ≤ V_{IN} ≤ 5.5 V			0.4	V
V_{IH}	Input Logic High	2.5 V ≤ V_{IN} ≤ 5.5 V	1.2			V
V_{OL}	Output Logic Low	I_{LOAD} = 3 mA			400	mV

I²C Timing Specifications

Symbol	Parameter	Min	Max	Unit
f_{SCL}	I²C SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		us
t_{LOW}	Low Period of I²C SCL Clock	1.3		us
t_{HIGH}	High Period of I²C SCL Clock	0.6		us
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		us
$t_{HD;DAT}$	Data Hold Time	0		us
$t_{SU;DAT}$	Data Set-up Time	100		ns
t_r	Rise Time of I²C_SDA and I²C_SCL Signals		300	ns
t_f	Fall Time of I²C_SDA and I²C_SCL Signals		300	ns
$t_{SU;STQ}$	Set-up Time for STOP Condition	0.6		us
t_{BUF}	Bus-Free Time between STOP and START Conditions	1.3		us
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns
C_b	Capacitive Load for each Bus Line		550	pF

I²C Timing Waveform

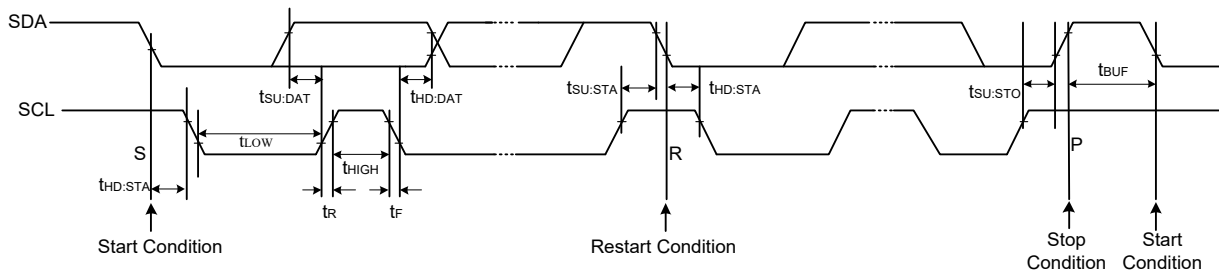


Figure 10. Definition of Timing for I²C Bus

Application circuit

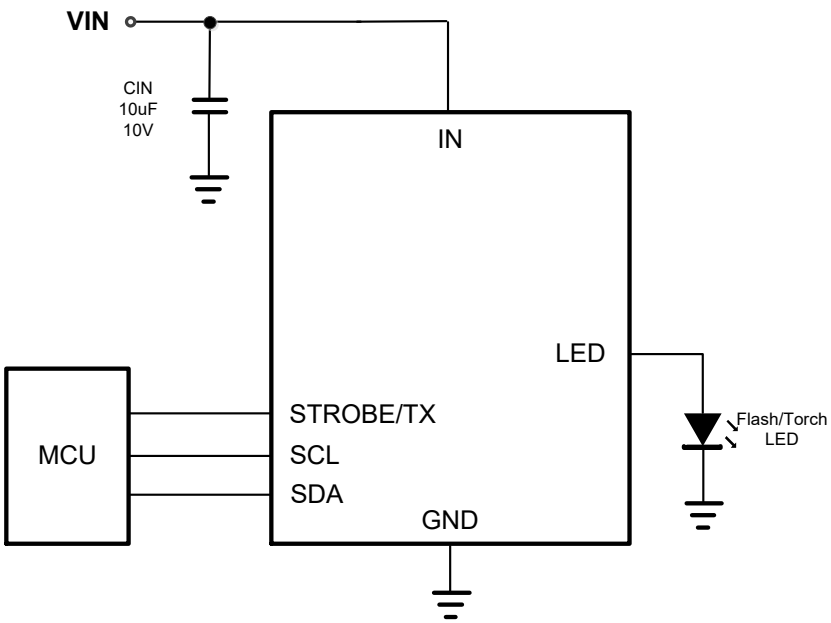


Figure 11. Typical Application(*)

Notes*:

1. Please place CIN as close to the chip as possible.

2. For the sake of driving capability, the power lines, output lines, and the connection lines of LED should be short and wide as possible.

Application Information

The ET93011 can drive a flash LEDs at currents up to 1.5A. Below are some peripheral selection guidelines.

Input Capacitor Selection

In the typical application circuit a 10μF ceramic input capacitor works well. It is important to place the input capacitor as close as possible to the ET93011 input (IN) pin. This reduces the series resistance and inductance that can inject noise into the device. Table 1 lists various input capacitors recommended for use with the ET93011.

Table 1. Recommended Input Capacitors (X5R/X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE	VOLTAGE RATING
TDK	C1608JB0J106M	10uF	0603	6.3V
TDK	C2012JB1A106M	10uF	0805	10V
Murata	GRM188R60J106M	10uF	0603	6.3V
Murata	GRM21BR61A106KE19	10uF	0805	10V

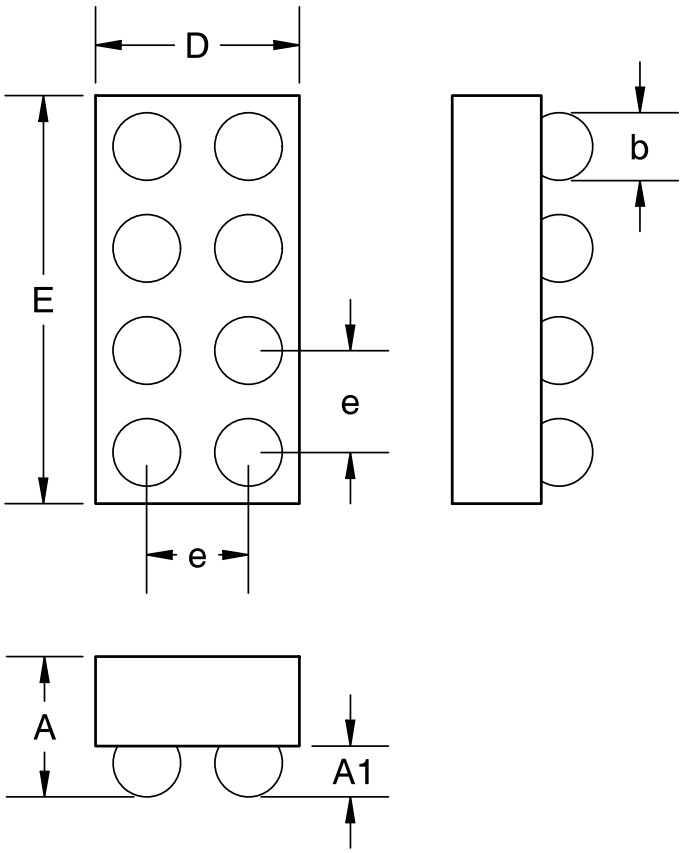
PCB Layout Guidelines

The large currents of the ET93011 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

(1). Place C_{IN} on the top layer (same layer as the ET93011) and as close to the device as possible. Connect the input capacitor through short, wide traces to both the IN and GND pins .

(2). Terminate the Flash LED cathodes directly to the GND pin of the ET93011. If possible, route the LED returns with a dedicated path so as to keep the high amplitude LED currents out of the GND plane. For Flash LEDs that are routed relatively far away from the ET93011, a good approach is to sandwich the forward and return current paths over the top of each other on two layers. This helps reduce the inductance of the LED current paths.

Package

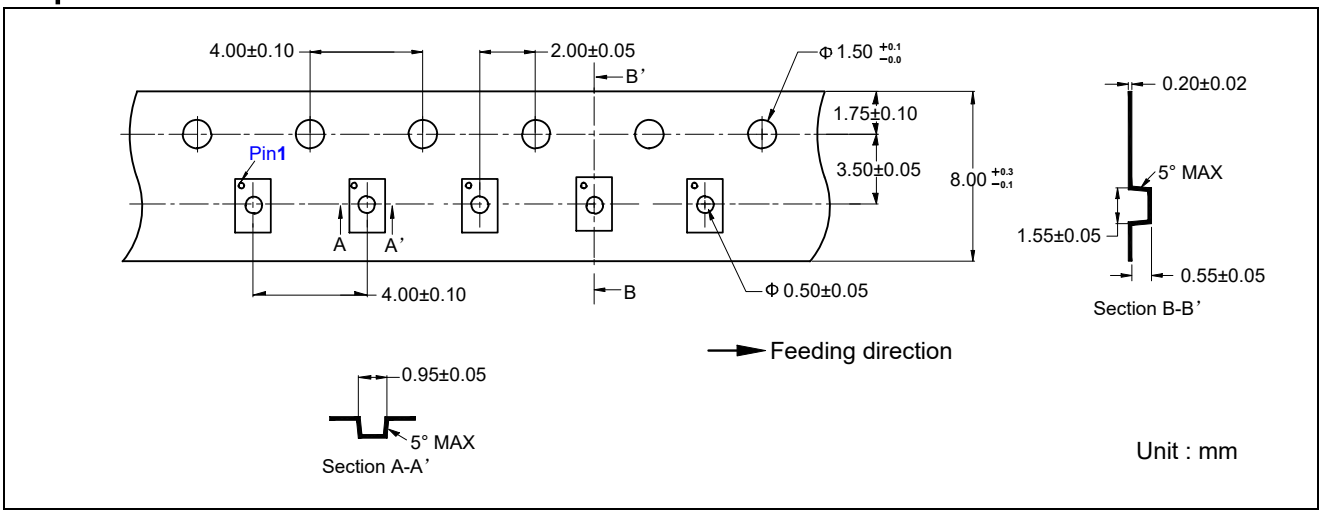


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.393	0.450	0.507
A1	0.130	0.155	0.175
b	0.188	0.213	0.238
D	0.770	0.800	0.830
E	1.490	1.520	1.550
e	0.350BSC		

Tape



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2019-11-26	Original Version	Lih	Liuyg	Liujy
1.1	2021-04-15	Add TX-function	Lih	Liuyg	Liujy
1.2	2021-07-01	Add Tape	Wangp	Liuyg	Liujy
1.3	2023-10-15	Update Typeset	Lvyj	Liuyg	Liujy