RAM Mapping 64×8 LCD Controller and Driver

General Description

The ET6625 is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 512 patterns (64×8). It also supports serial interface, buzzer sound, Watchdog Timer or time base timer functions.

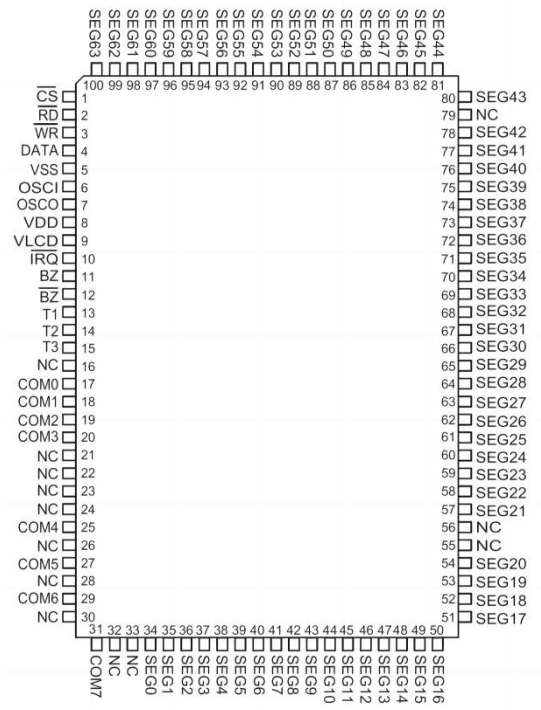
The ET6625 is a memory mapping and multi-function LCD controller. The software configuration feature of the ET6625 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the MCU and the ET6625.

Features

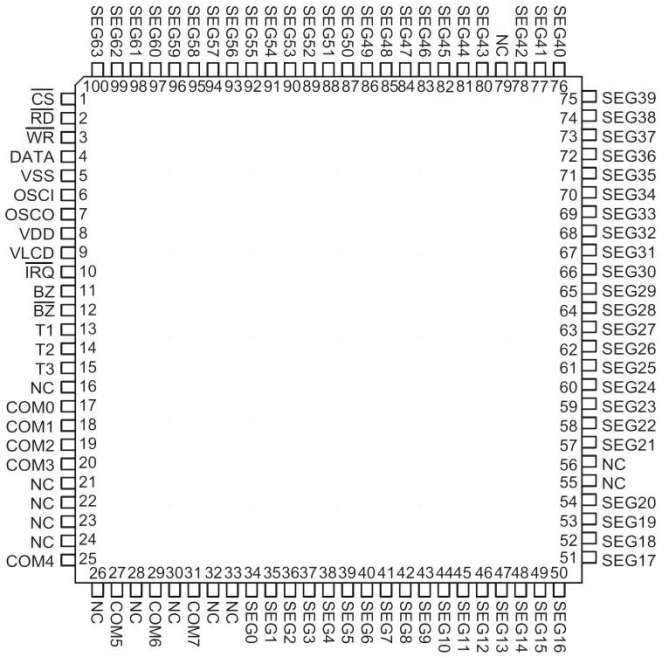
- Operating voltage: 2.7V~5.2V
- Built-in RC oscillator
- External 32.768kHz crystal or 32kHz frequency source input
- 1/4 bias, 1/8 duty, frame frequency is 64Hz
- Max. 64×8 patterns, 8 commons, 64 segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base or WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Two select-able buzzer frequencies (2kHz or 4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- Part No. and Package

Part No.	Package
ET6625B	QFP100 (14mm ×20mm)
ET6625L	LQFP100 (14mm ×14mm)

Pin Configuration



QFP100(ET6625B)



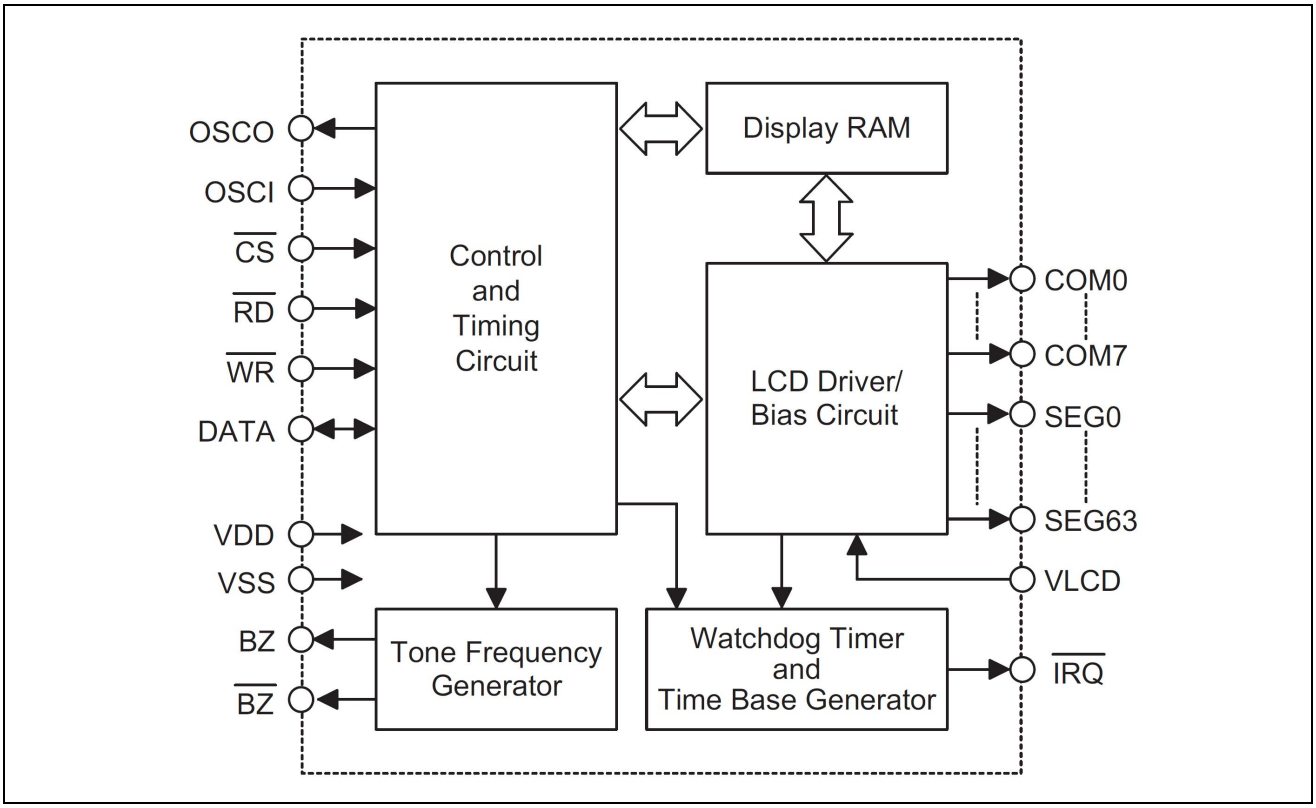
LQFP100(ET6625L)

Pin Function

Pin No.	Pin Name	I/O	Function
1	$\overline{CS}$	I	Chip selection input with pull-high resistor. When the CS is logic high, the data and command read from or write to the ET6625 are disabled. The serial interface circuit is also reset. But if the CS is at logic low level and is input to the CS pad, the data and command transmission between the host controller and the ET6625 are all enabled.
2	$\overline{RD}$	I	READ clock input with pull-high resistor. Data in the RAM of the ET6625 are clocked out on the falling edge of the RD signal. The clocked out data will appear on the data line. The host controller can use the next rising edge to latch the clocked out data.
3	$\overline{WR}$	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the ET6625 on the rising edge of the WR signal.
4	DATA	I/O	Serial data input or output with pull-high resistor.
5	VSS	-	Negative power supply, ground.
6	OSCI	I	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
7	OSCO	O	

8	VDD	-	Positive power supply.
9	VLCD	I	LCD operating voltage input pad.
10	$\overline{IRQ}$	O	Time base or Watchdog Timer overflow flag, NMOS open drain output.
11，12	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair.
13-15	T1~T3	I	Not connected.
16	NC	-	Not connected.
17-31	COM0~COM7	O	LCD common outputs. 21,22,23,24,26,28,30 are NC, not connected.
32~100	SEG0~SEG63	O	LCD segment outputs. 32,33,55,56,79 are NC, not connected.

Block Diagram



Functional Description

Display Memory -RAM Structure

The static display RAM is organized into 128×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

Time Base and Watchdog Timer -WDT

The time base generator and WDT share the same divided (1/256) counter. TIMER DIS/EN/CLR,WDT DIS/EN/CLR and IRQ EN/DIS are independent from each other. Once the WDT time-out occurs, the IRQ pin will remain at logic low level until the CLR WDT or the IRQ DIS command is issued.

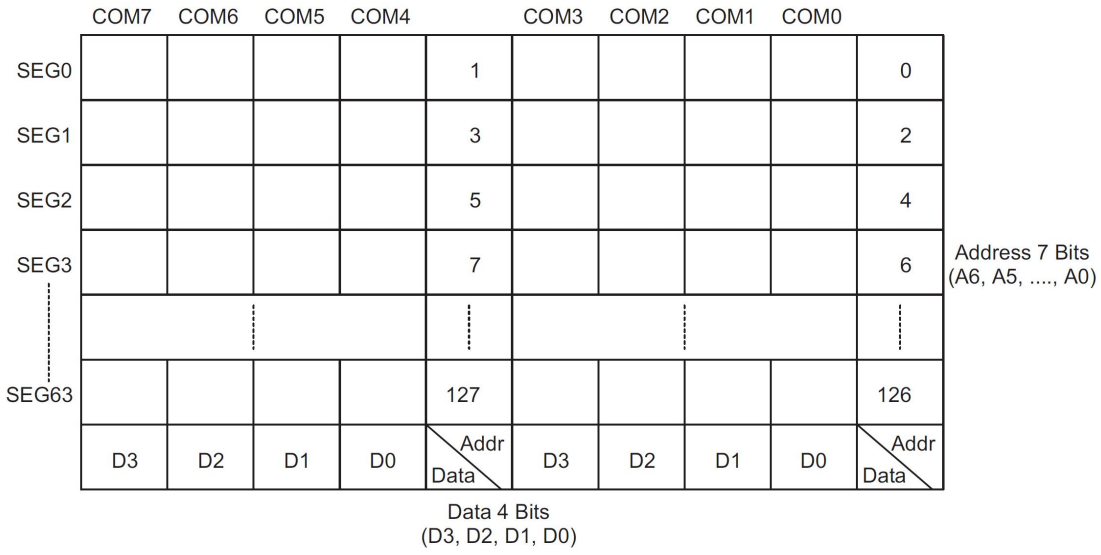
If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

Buzzer Tone Output

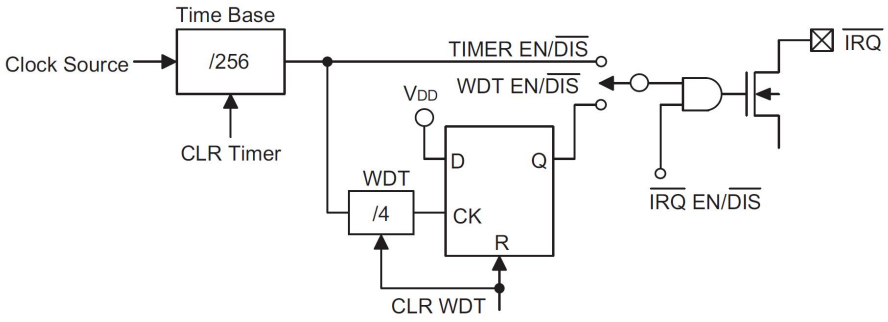
A simple tone generator is implemented in the ET6625.The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$ which are used to generate a single tone.

Command Format

The ET6625 can be configured by the software setting. There are two mode commands to configure the ET6625 resource and to transfer the LCD display data.



RAM Mapping



Timer and WDT Configurations

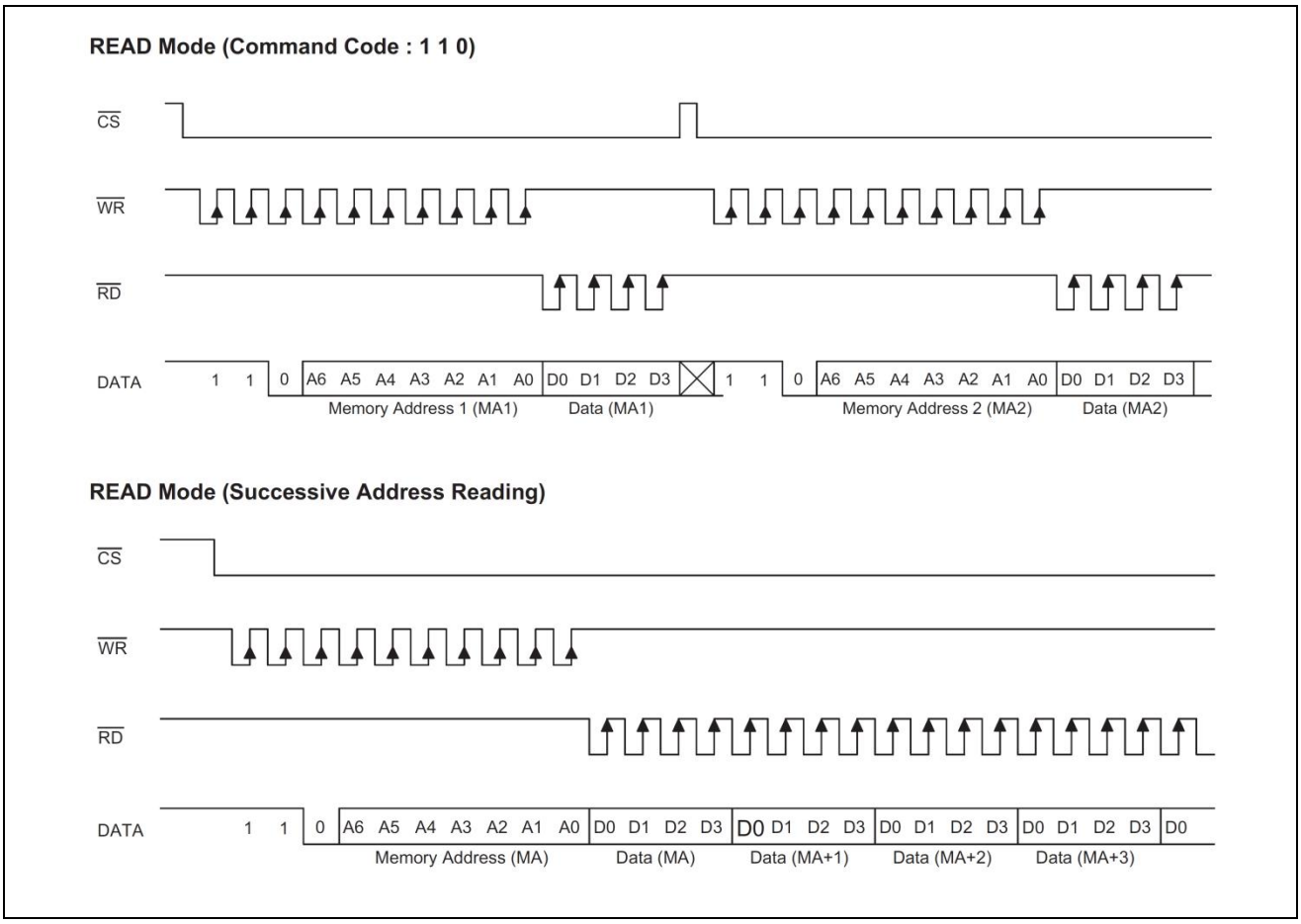
The following are the data mode ID and the command mode ID:

OPERATION	MODE	ID
Read	Data	110
Write	Data	101
Read-Modify-Write	Data	101
Command	Command	100

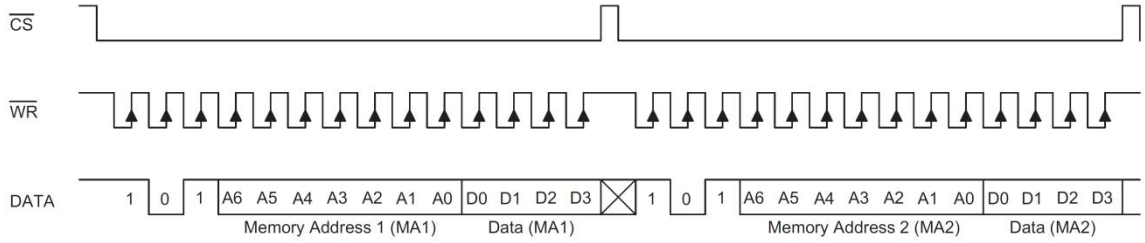
NAME	COMMAND CODE	FUNCTION
TONE OFF	0000-1000-X	Turn-off tone output
TONE 4K	010X-XXXX-X	Turn-on tone output, tone frequency is 4kHz
TONE 2K	0110-XXXX-X	Turn-on tone output, tone frequency is 2kHz

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will be reset also. The $\overline{CS}$ pin returns to "0", a new operation mode ID should be issued first.

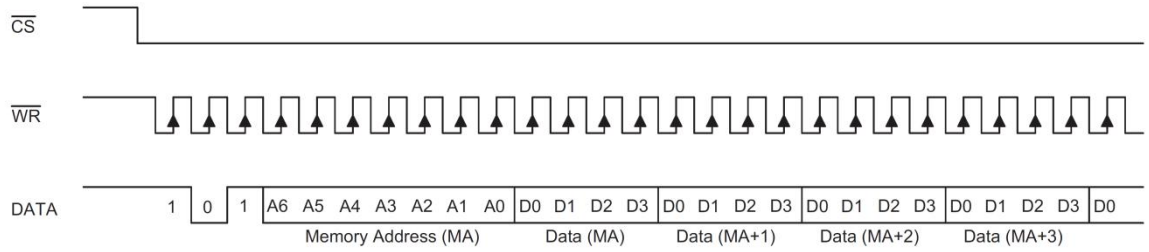
Timing Diagrams



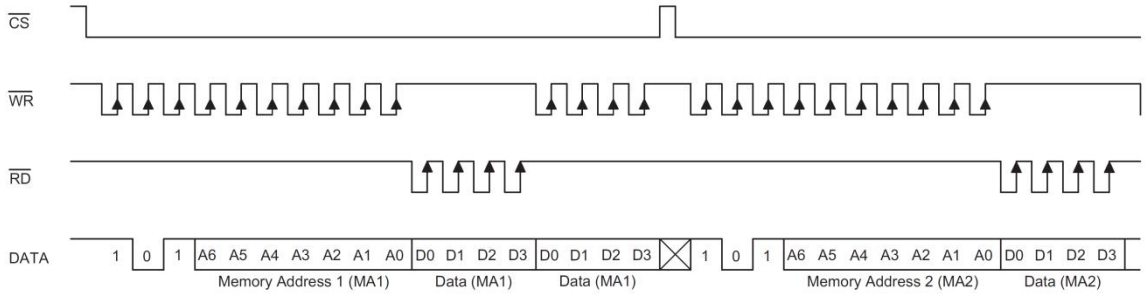
WRITE Mode (Command Code : 1 0 1)



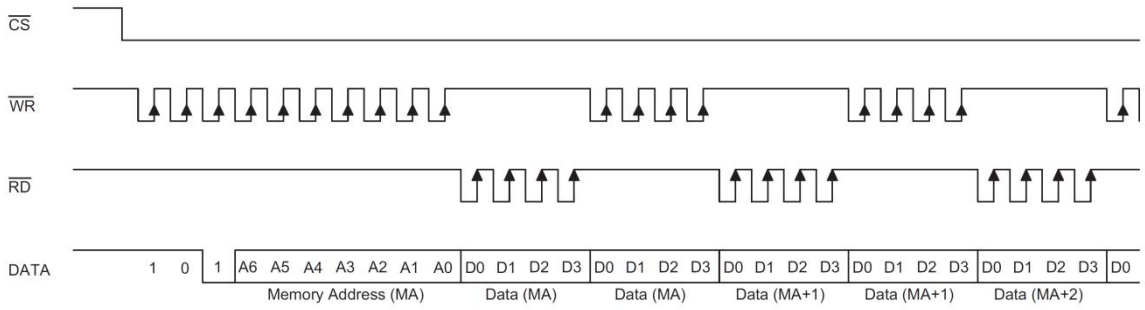
WRITE Mode (Successive Address Writing)

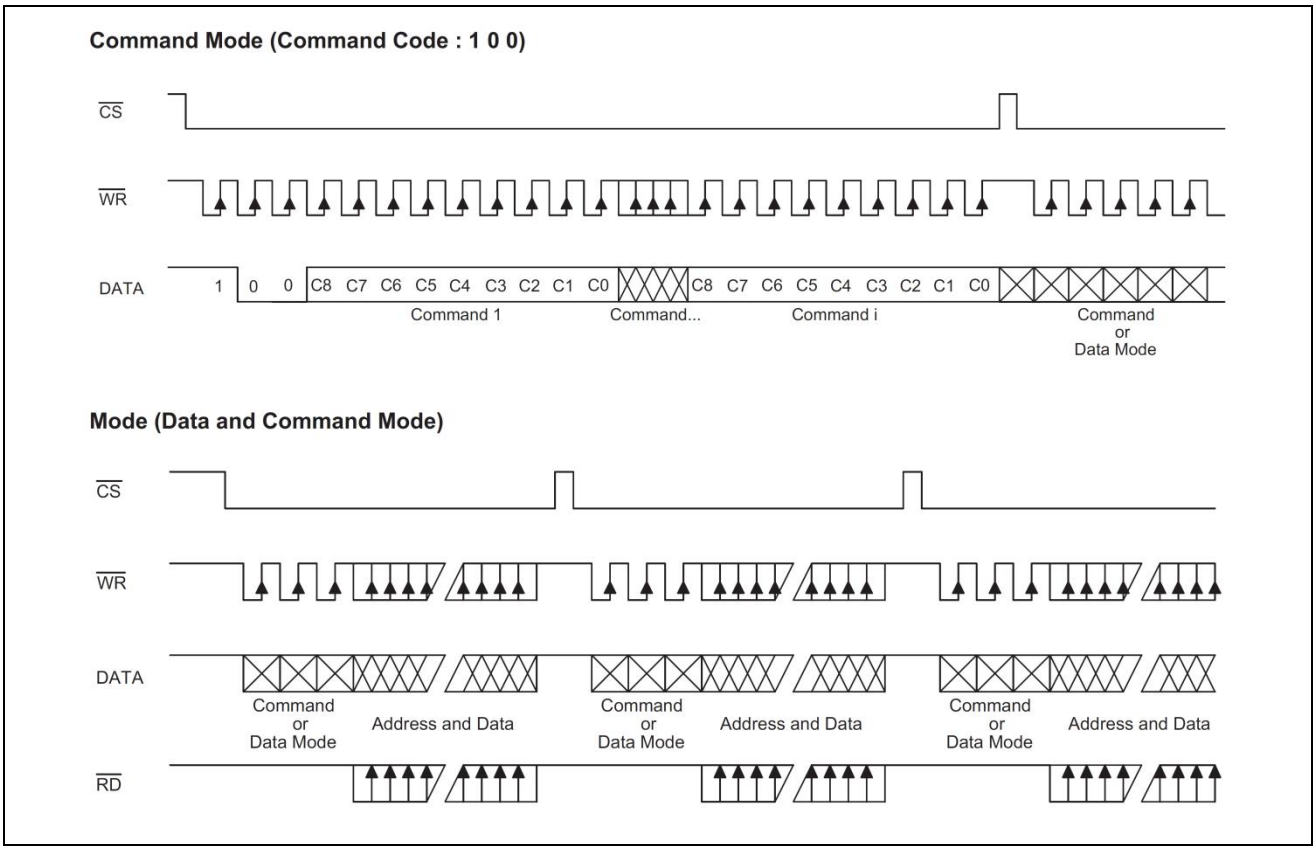


READ-MODIFY-WRITE Mode (Command Code : 1 0 1)



READ-MODIFY-WRITE Mode (Successive Address Accessing)





Command Summary

Name	ID	Command Code	D/C	Function	Def
READ	110	A6A5A4A3A2A1A0D 0D1D2D3	D	Read data from the RAM	
WRITE	101	A6A5A4A3A2A1A0D 0D1D2D3	D	Write data to the RAM	
READ-MODIFY WRITE	101	A6A5A4A3A2A1A0D 0D1D2D3	D	Read and Write data to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD display	Yes
LCD ON	100	0000-0011-X	C	Turn on LCD display	
TIMER DIS	100	0000-0100-X	C	Disable time base output	Yes
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag output	Yes
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	Yes
CLR TIMER	100	0000-1101-X	C	Clear the contents of the time base generator	
CLR WDT	100	0000-1111-X	C	Clear the contents of the WDT stage	
RC 32K	100	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes

EXT (XTAL) 32K	100	0001-11XX-X	C	System clock source, external 32kHz clock source or crystal oscillator 32.768kHz	
TONE 4K	100	010X-XXXX-X	C	Tone frequency output: 4kHz	
TONE 2K	100	0110-XXXX-X	C	Tone frequency output: 2kHz	
$\overline{\text{IRQ}}$ DIS	100	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}}$ EN	100	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	100	101X-0000-X	C	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	100	101X-0001-X	C	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	100	101X-0010-X	C	Time base clock output: 4Hz The WDT time-out flag after: 1s	
F8	100	101X-0011-X	C	Time base clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-0100-X	C	Time base clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-0101-X	C	Time base clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-0110-X	C	Time base clock output: 64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-0111-X	C	Time base clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	100	1110-0000-X	C	Test mode, user don't use.	
NORMAL	100	1110-0011-X	C	Normal mode	Yes

Notes:

X : Don't care

A6~A0 : RAM address

D3~D0 : RAM data

D/C : Data/Command mode

Def. : Power on reset default

All the bold forms, namely 1 1 0, 1 0 1, and 1 0 0, are mode commands. Of these, 1 0 0 indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base or WDT clock frequency can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the ET6625 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the ET6625.

Absolute Maximum Ratings

Parameter	Symbol	Range	Unit
Supply Voltage	V_{DD}	-0.3～5.5	V
Input Voltage	V_{IN}	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	ºC
Operating Junction Temperature	T_J	-40～+150	ºC

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Range	Unit
Supply Voltage	V_{DD}	2.7～5.2	V
Operating Temperature	T_A	-25～+75	ºC

Electronic Characteristics

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage			2.7		5.2	V
I_{DD1}	Operating Current	3V	No load or LCD ON; On-chip RC oscillator		155	310	uA
		5V			260	420	uA
I_{DD2}	Operating Current	3V	No load or LCD ON; Crystal oscillator		150	310	uA
		5V			250	420	uA
I_{DD11}	Operating Current	3V	No load or LCD OFF; On-chip RC oscillator		8	30	uA
		5V			20	60	uA
I_{DD22}	Operating Current	3V	No load or LCD OFF; Crystal oscillator			20	uA
		5V				35	uA
I_{STB}	Standby Current	3V	No load, Power down mode		1	12	uA
		5V			2	24	uA
V_{IL}	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0		0.6	V
		5V		0		1.0	V
V_{IH}	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4		3	V
		5V		4.0		5	V
I_{OL1}	BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	V_{OL}=0.3V	0.9	1.8		mA
		5V	V_{OL}=0.5V	1.7	3		mA
I_{OH1}	BZ, $\overline{BZ}$	3V	V_{OH}=2.7V	-0.9	-1.8		mA
		5V	V_{OH}=4.5V	-1.7	-3		mA

I_{OL1}	DATA	3V	V_{OL}=0.3V	0.9	1.8		mA
		5V	V_{OL}=0.5V	1.7	3		mA
I_{OH1}	DATA	3V	V_{OH}=2.7V	-0.9	-1.8		mA
		5V	V_{OH}=4.5V	-1.7	-3		mA
I_{OL2}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	160		uA
		5V	V_{OL}=0.5V	180	360		uA
I_{OH2}	LCD Common Source Current	3V	V_{OH}=2.7V	-40	-80		uA
		5V	V_{OH}=4.5V	-90	-180		uA
I_{OL3}	LCD Segment Sink Current	3V	V_{OL}=0.3V	50	100		uA
		5V	V_{OL}=0.5V	120	240		uA
I_{OH3}	LCD Segment Source Current	3V	V_{OH}=2.7V	-30	-60		uA
		5V	V_{OH}=4.5V	-70	-140		uA
R_{PH}	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	100	200	300	kΩ
		5V		50	100	150	kΩ

Electronic Characteristics

A.C. Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	5V	On-chip RC oscillator	24	32	40	kHz
f_{SYS2}	System Clock		External clock source		32		kHz
f_{LCD1}	LCD Frame Frequency	5V	On-chip RC oscillator	48	64	80	Hz
f_{LCD2}	LCD Frame Frequency		External clock source		64		Hz
t_{COM}	LCD Common Period		n:Number of COM		n/f_{LCD}		sec
f_{CLK1}	Serial Data Clock ($\overline{WR}$ Pin)	3V	Duty cycle 50%	4		150	kHz
		5V		4		300	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ Pin)	3V	Duty cycle 50%			75	kHz
		5V				150	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)		$\overline{CS}$	700	800		ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34		125	us
			Read mode	6.67			
		5V	Write mode	1.67		125	us
			Read mode	3.34			
tr, tf	Rise or Fall Time Serial Data Clock Width (Figure 1)				120	160	ns
tsu	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)			60	120		ns
t_h	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)				700	800	ns

t_{su1}	Setup Time for CS to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)				500	600	ns
t_{h1}	Hold Time for CS to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)			50	100		ns
f_{tone}	Tone Frequency (2KHz)	5V	On-chip RC oscillator	1.5	2.0	2.5	kHz
	Tone Frequency (4KHz)			3.0	4.0	5.0	kHz
t_{OFF}	V_{DD} OFF Times (Figure 4)		V_{DD} drop down to 0V	20			ms
t_{SR}	V_{DD} Rising Slew Rate (Figure 4)			0.05			V/ms
t_{RSTD}	Delay Time after Reset (Figure 4)			1			ms

Notes:

1. If the conditions of Power-on Reset timing are not satisfied in power On/Off sequence, the internal Power-on Reset (POR) circuit will not operate normally.

2. If the VDD drops below the minimum voltage of operating voltage spec. during operating, the conditions of Power-on Reset timing must be satisfied also. That is, the VDD must drop to 0V and keep at 0V for 20ms (min.) before rising to the normal operating voltage.

Test Waveform

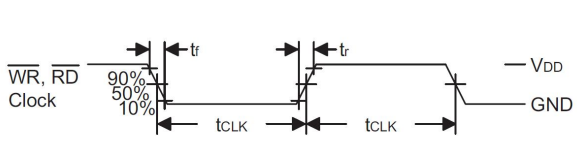


Figure 1

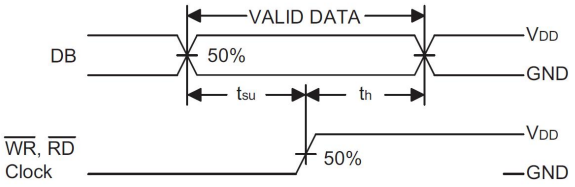


Figure 2

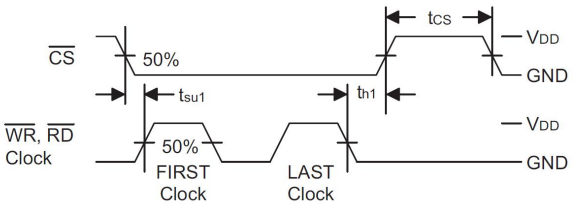


Figure 3

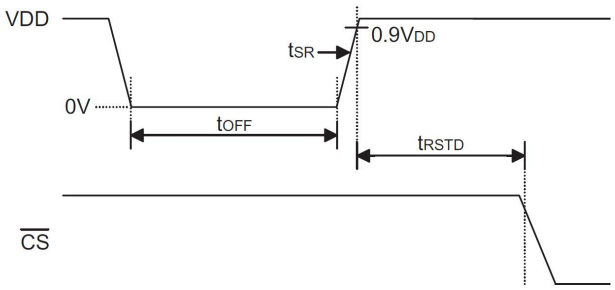
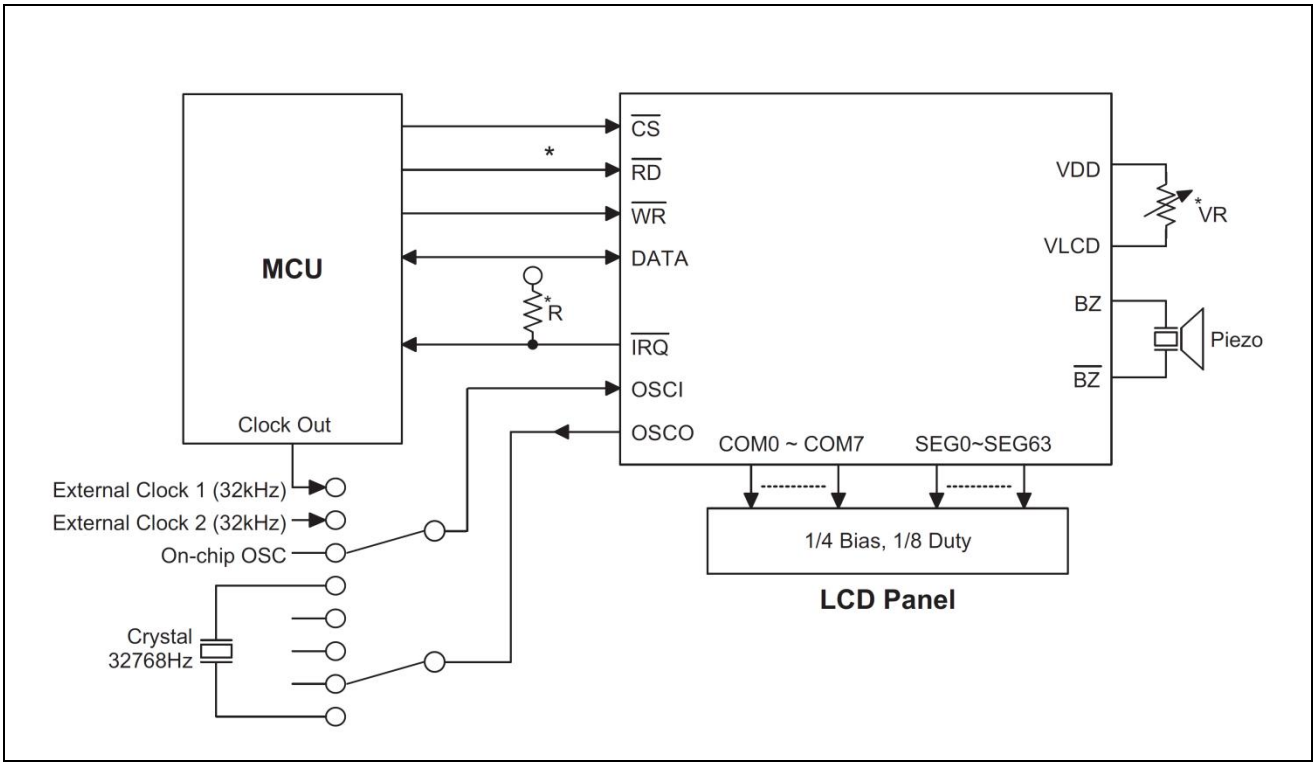


Figure 4 Power-on Reset Timing

Application Circuit



Notes:

1. The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the MCU.

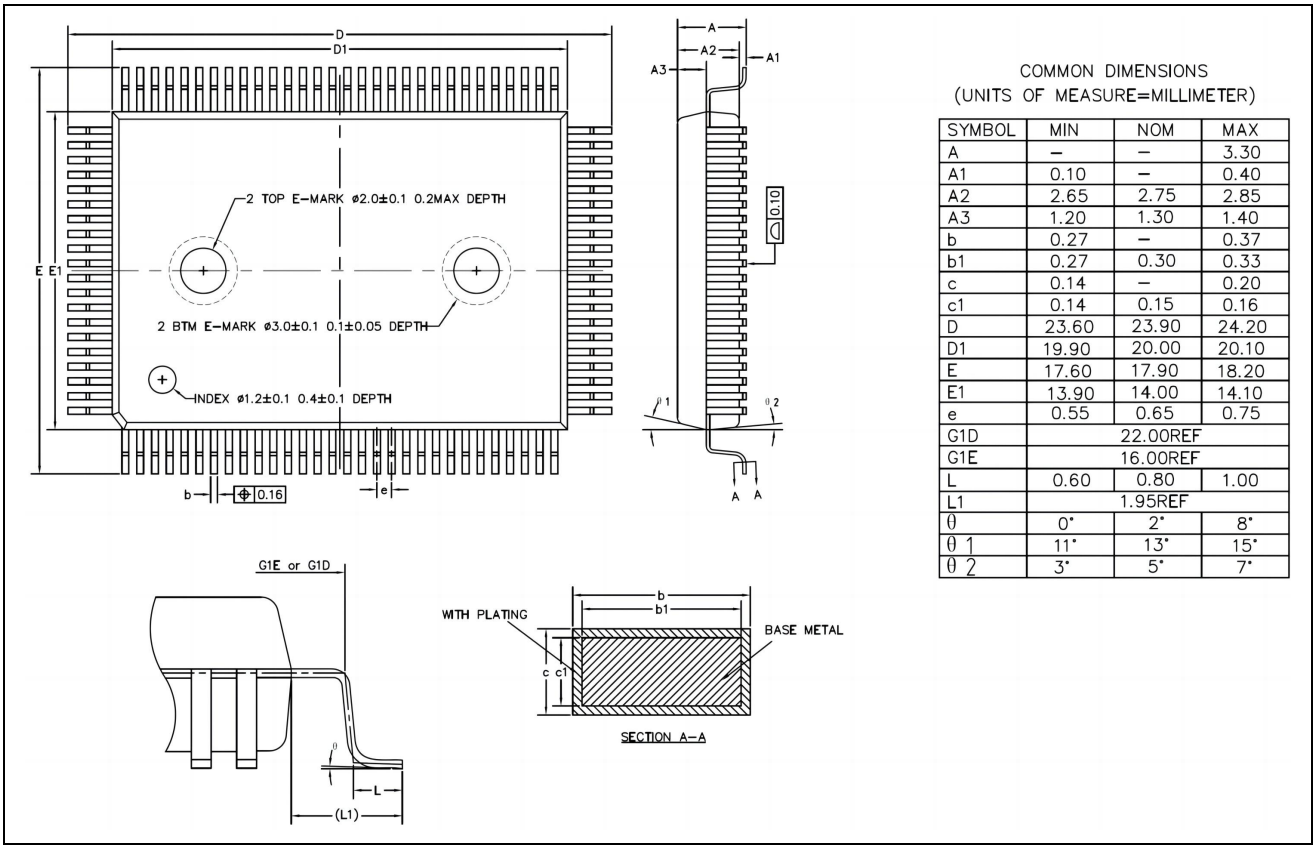
2. The voltage applied to V_{LCD} pin must be equal to or lower than V_{DD}.

3. Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR=15kΩ ± 20%.

4. Adjust R (external Pull-high resistance) to fit user's time base clock.

Package Dimension

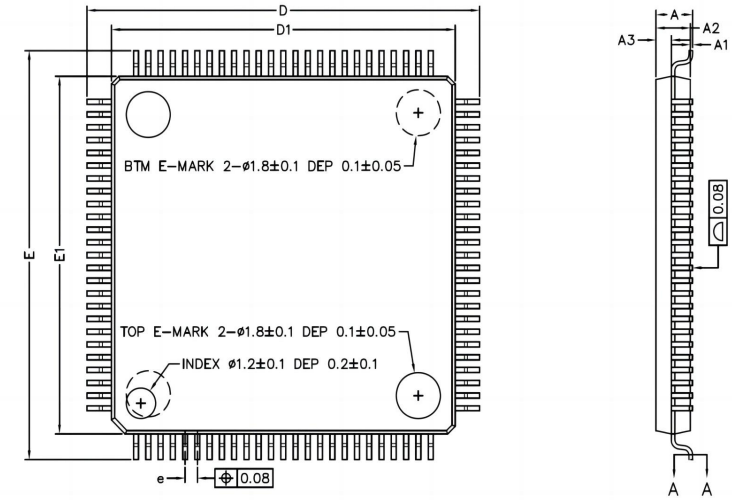
QFP100 (ET6625B)

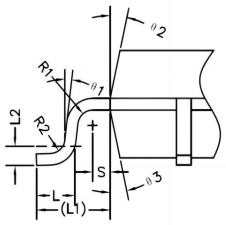


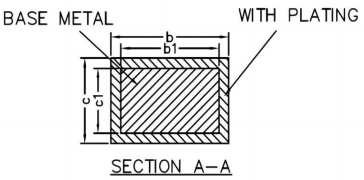
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	3.30
A1	0.10	–	0.40
A2	2.65	2.75	2.85
A3	1.20	1.30	1.40
b	0.27	–	0.37
b1	0.27	0.30	0.33
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	23.60	23.90	24.20
D1	19.90	20.00	20.10
E	17.60	17.90	18.20
E1	13.90	14.00	14.10
e	0.55	0.65	0.75
G1D		22.00REF	
G1E		16.00REF	
L	0.60	0.80	1.00
L1		1.95REF	
θ	0°	2°	8°
θ1	11°	13°	15°
θ2	3°	5°	7°

LQFP100 (ET6625L)







COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2018-01-25	Original Version	Wanggp	Wanggp	Zhujl
1.1	2019-06-11	Add LQFP100 package	Wanggp	Wanggp	Zhujl
1.2	2023-8-13	Update Typeset	Shibo	Shilj	Liujy