RAM Mapping 48×8 LCD Controller for I/O

General Description

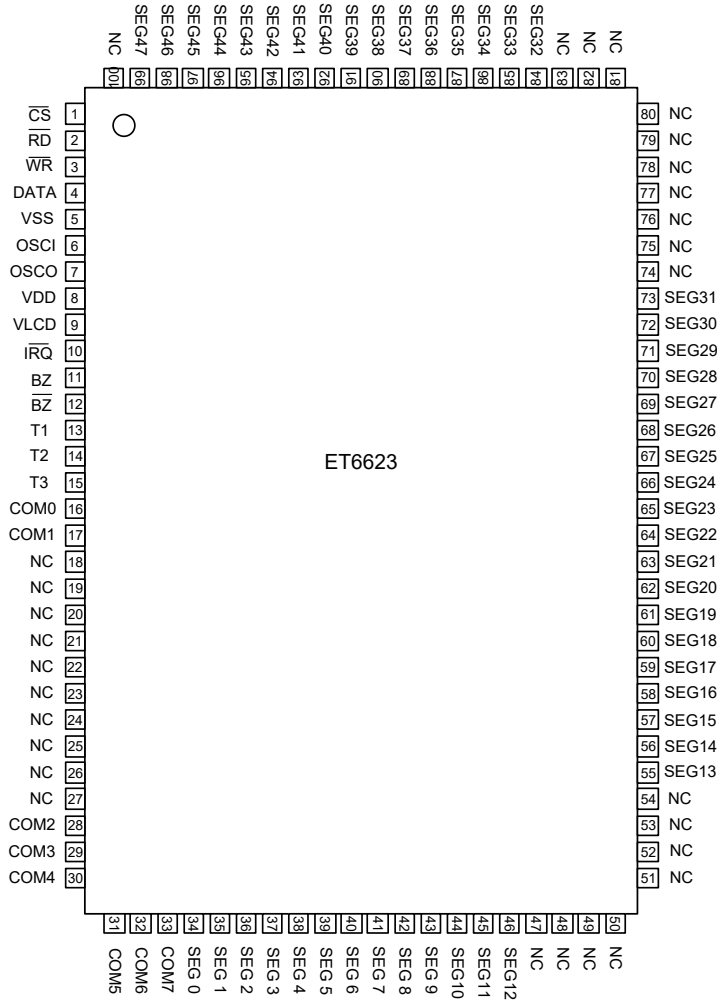
ET6623 is a memory mapping and multi-function LCD controller, specially designed for I/O type MCU used to expand the display capability. The max. Display segment of the device are 384 patterns (48×8).Using the Power down command can reduce power consumption.

Features

- Operating voltage: 2.7V~5.2V
- Built-in 32 kHz RC oscillator
- 1/4bias, 1/8duty, frame frequency is 64Hz
- Max.48×8 patterns, 8 commons, 48 segments
- Built-in internal resistor type bias generator
- 3 or 4-wire serial interface
- 8 kinds of time base/WDT selection
- Time base or WDT over flow output
- Built-in LCD display RAM
- R/W address auto increment
- Tow selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- Cascade application
- Part No. and package

Part No.	Package
ET6623	QFP100 (14mm×20mm)

Pin Configuration

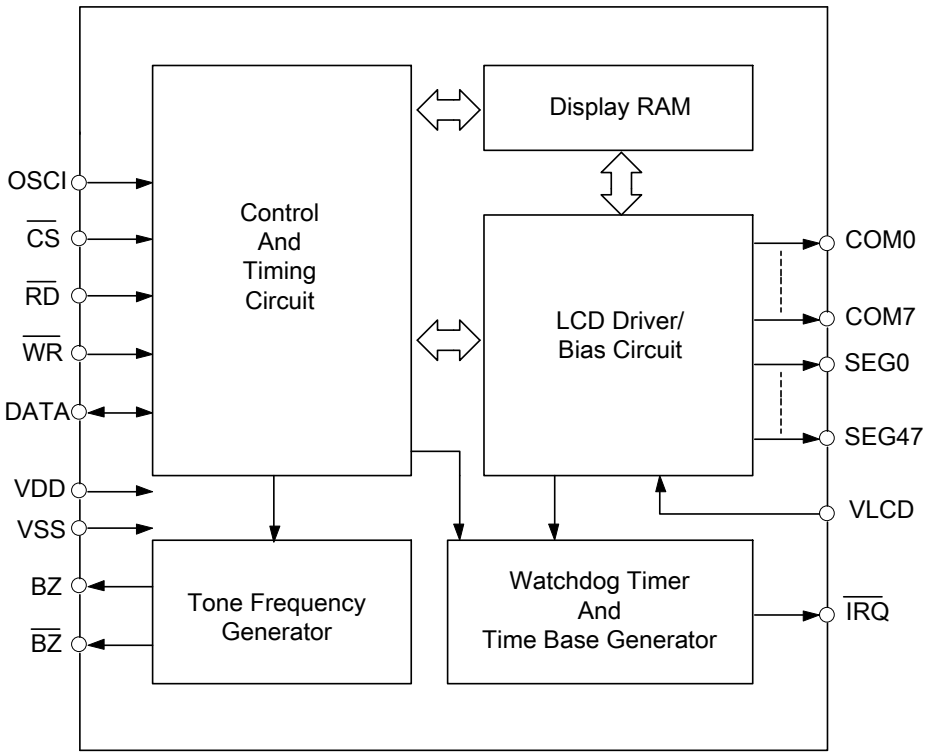


TOP VIEW

Pin Function

Pin Name	I/O	Function
$\overline{CS}$	I	Chip selection input with Pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or written to the ET6623 are disabled. The serial interface circuit is also reset. But if $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the ET6623 are all enabled.
$\overline{RD}$	I	READ clock input with Pull-high resistor. Data in the RAM of the ET6623 are clocked out on the rising edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next falling edge to latch the clocked out data.
$\overline{WR}$	I	WRITE clock input with Pull-high resistor. Data on the DATA line are latched into the ET6623 on the rising edge of the $\overline{WR}$ signal.
DATA	I/O	Serial data input/output with Pull-high resistor.
VSS	-	Negative power supply, ground.
OSCI, OSCO	I	If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad.
VDD	-	Positive power supply.
VLCD	I	LCD operating voltage input pad.
$\overline{IRQ}$	O	Time base or Watchdog Timer overflow flag, NMOS open drain output.
BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair.
T1～T3	I	Not connected.
COM0～COM7	O	LCD common outputs.
SEG0～SEG47	O	LCD segment outputs.

Block Diagram



Functions Description

Display memory-RAM structure

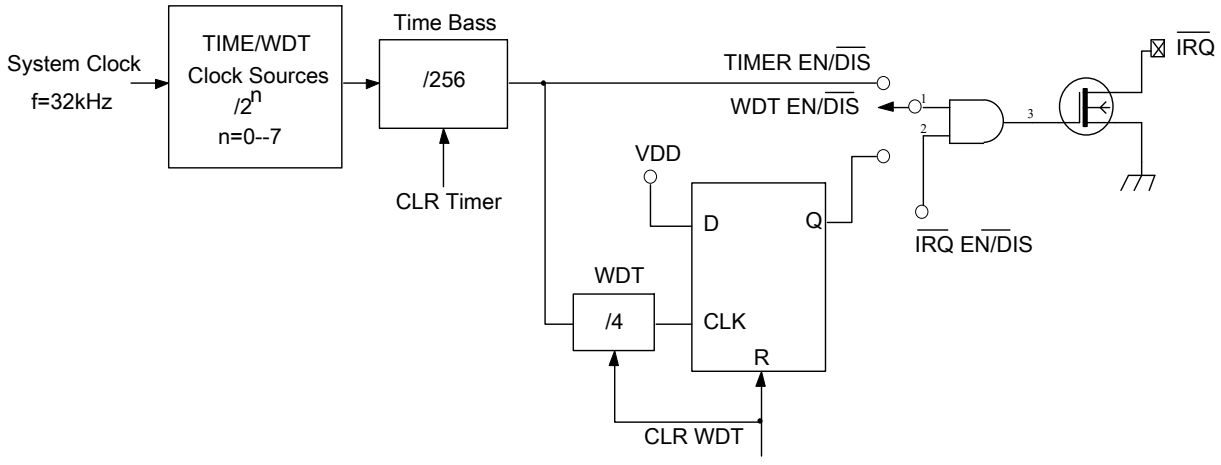
The static display RAM is organized into 96×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

	COM7	COM6	COM5	COM4		COM3	COM2	COM1	COM0		
SEG0					1					0	ADDR 7bit （A6，A5～A0）
SEG1					3					2	
SEG2					5					4	
SEG3					7					6	
⋮					⋮					⋮	
SEG47					95					94	
	D3	D2	D1	D0	Data\Addr	D3	D2	D1	D0	Data\Addr	

RAM mapping

Time base and Watchdog Timer (WDT)

The time base generator and WDT share the same divided (/256) counter. TIMERDIS/EN/CLR, WDT DIS/EN/CLR and $\overline{IRQ}$ EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will remain at logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued.



Timer and WDT configurations

If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

Buzzer Tone Output

A simple tone generator is implemented in the ET6623. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$ which are used to generate a single tone.

Name	Command Code	Function
TONE OFF	0000-1000-X	Turn-off tone output
TONE 4k	010X-XXXX-X	Turn-off tone output, tone frequency is 4kHz
TONE 2k	0110-XXXX-X	Turn-off tone output, tone frequency is 2kHz

Command Format

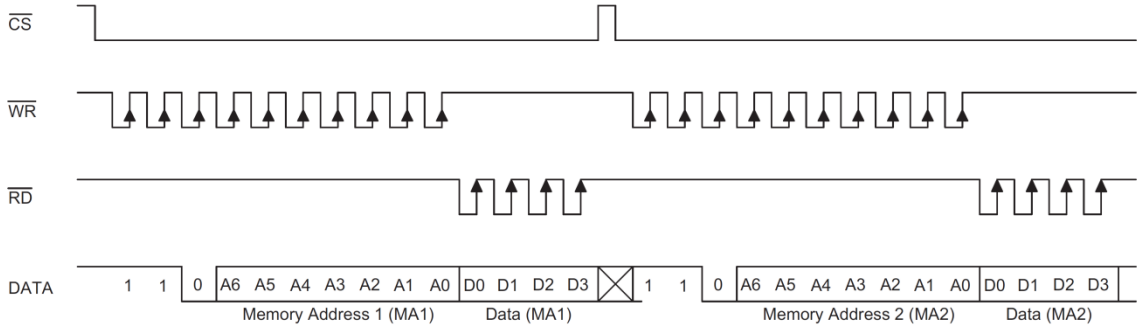
The ET6623 can be configured by the software setting. There are two mode commands to con-figure the ET6623 resource and to transfer the LCD display data.

Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

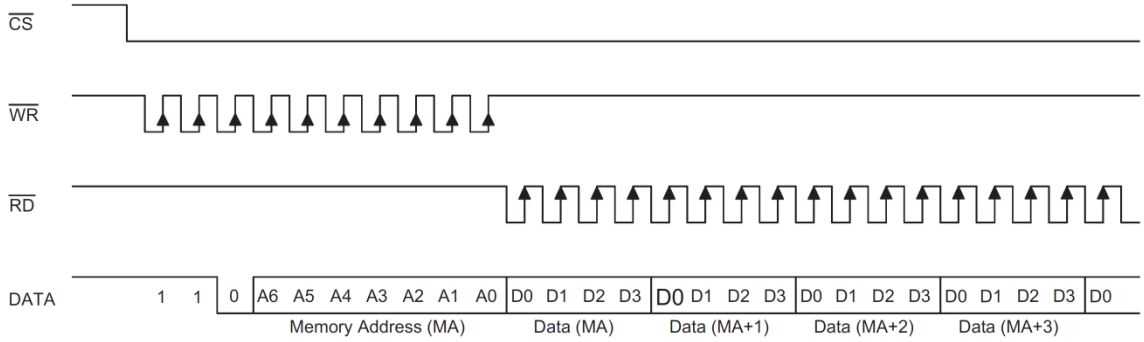
If successive commands have been issued, the command mode ID can be omitted. While the system is operating in a non-successive command or a non-successive address data mode, the $\overline{CS}$ pin should be set to”1” and the previous operation mode will be reset also. The $\overline{CS}$ pin returns to”0”, a new operation mode ID should be issued first.

Timing Diagrams

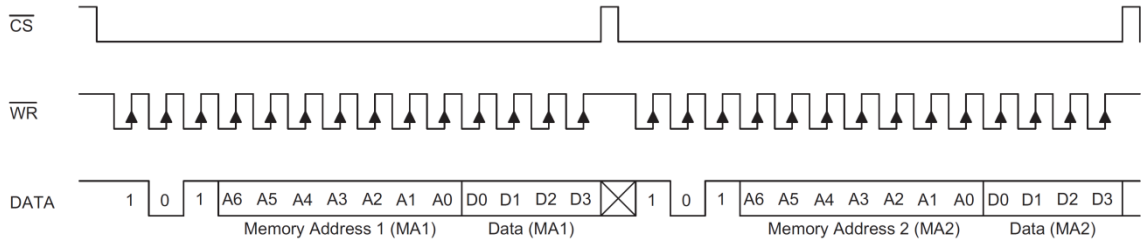
READ Mode (Command Code : 1 1 0)



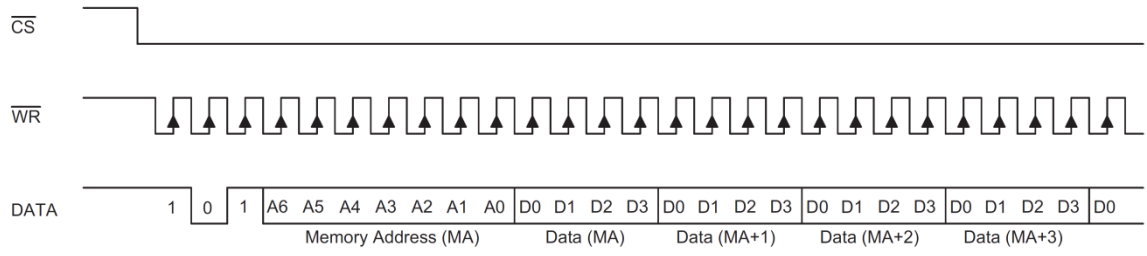
READ Mode (Successive Address Reading)



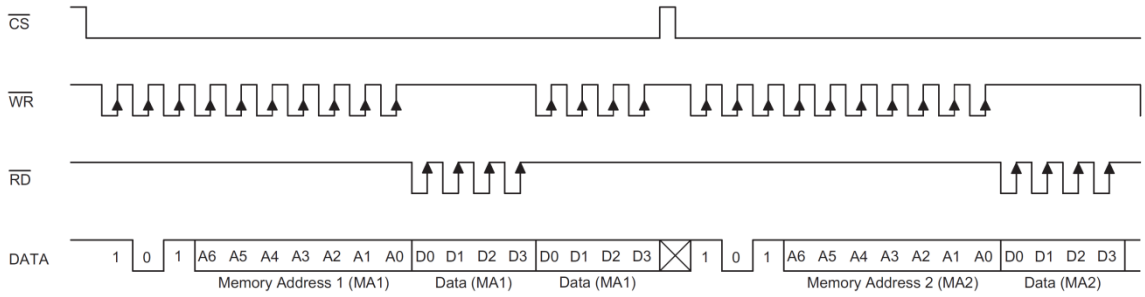
WRITE Mode (Command Code : 1 0 1)



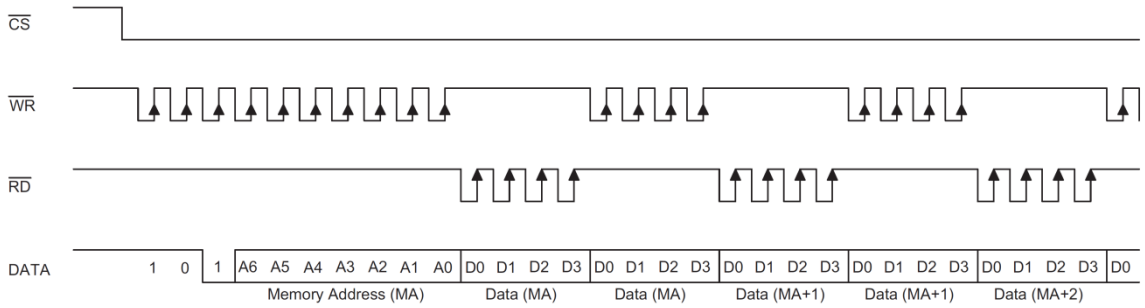
WRITE Mode (Successive Address Writing)



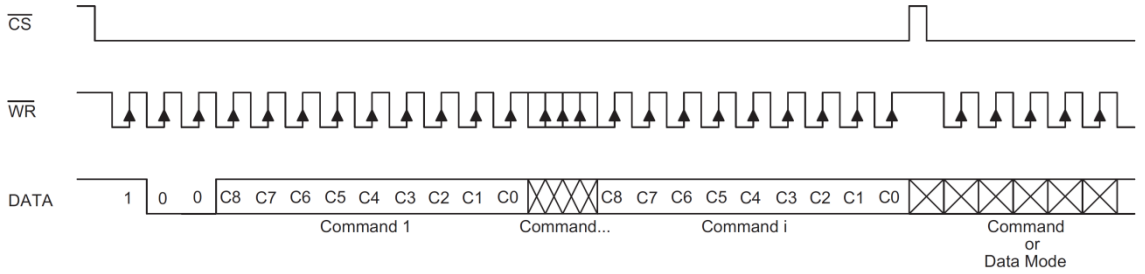
READ-MODIFY-WRITE Mode (Command Code : 1 0 1)



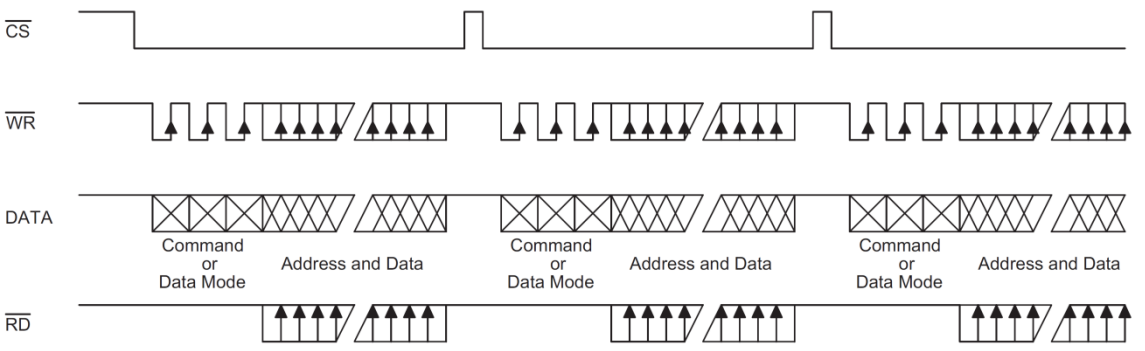
READ-MODIFY-WRITE Mode (Successive Address Accessing)



Command Mode (Command Code : 1 0 0)



Mode (Data and Command Mode)



Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A6A5A4A3A2A1A0D0D1D2D3	D	Read and Write data to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD display	Yes
LCD ON	100	0000-0011-X	C	Turn on LCD display	
TIMER DIS	100	0000-0100-X	C	Disable time base output	Yes
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag output	Yes
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone output	Yes
CLR TIMER	100	0000-1101-X	C	Clear the contents of the time base generator	
CLR WDT	100	0000-1111-X	C	Clear the contents of WDT stage	
RC 32k	100	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT 32k	100	0001-11XX-X	C	System clock source, external clock source	
TONE 4k	100	010X-XXXX-X	C	Tone frequency output:4kHz	
TONE 2k	100	0110-XXXX-X	C	Tone frequency output:2kHz	
$\overline{\text{IRQ}}$ DIS	100	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}}$ EN	100	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	100	101X-0000-X	C	Time base clock output:1Hz， The WDT time-out flag after: 4s	
F2	100	101X-0001-X	C	Time base clock output:2Hz， The WDT time-out flag after: 2s	
F4	100	101X-0010-X	C	Time base clock output:4Hz， The WDT time-out flag after: 1s	
F8	100	101X-0011-X	C	Time base clock output:8Hz， The WDT time-out flag after: 1/2s	
F16	100	101X-0100-X	C	Time base clock output:16Hz， The WDT time-out flag after: 1/4s	

Command summary (Continued)

Name	ID	Command Code	D/C	Function	Def.
F32	100	101X-0101-X	C	Time base clock output:32Hz， The WDT time-out flag after: 1/8s	
F64	100	101X-0110-X	C	Time base clock output:64Hz， The WDT time-out flag after: 1/16s	
F128	100	101X-0111-X	C	Time base clock output:128Hz， The WDT time-out flag after: 1/32s	Yes
TEST	100	1110-0000-X	C	Test mode, user don't use	
NORMAL	100	1110-0011-X	C	Normal mode	Yes

Notes:

1. X: Don't care.
2. A6~A0: RAM address.
3. D3~D0: RAM data.
4. D/C: Data/Command mode.
5. Def: Power on reset default.
6. All the bold forms, namely 110, 101, and 100, are mode commands. Of these, 100 indicate the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted.
7. It is recommended that the host controller should initialize the ET6623 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the ET6623.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3～5.5	V
V_{IO}	Input Voltage	V_{SS}-0.3～V_{DD}+0.3	V
T_{STG}	Storage Temperature	-50～125	˚C
T_J	Junction Temperature	-40～150	˚C

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	Supply Voltage	2.7～5.2	V
T_A	Operating Temperature	-25～+75	˚C

Electrical Characteristics

DC Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	-	-	2.7	-	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON	-	155	310	μA
		5V	On-chip RC oscillator	-	260	420	μA
I_{DD2}	Operating Current	3V	No load/LCD OFF	-	8	30	μA
		5V	On-chip RC oscillator	-	20	60	μA
I_{STB}	Standby Current	3V	No load	-	1	10	μA
		5V	Power down mode	-	2	20	μA
V_{IL}	Input Low Voltage	3V	DATA，$\overline{WR}$，$\overline{CS}$，$\overline{RD}$	0	-	0.6	V
		5V		0	-	1.0	V
V_{IH}	Input High Voltage	3V	DATA，$\overline{WR}$，$\overline{CS}$，$\overline{RD}$	2.4	-	3.0	V
		5V		4.0	-	5.0	V
I_{OL1}	BZ，$\overline{BZ}$，$\overline{IRQ}$	3V	V_{OL}=0.3V	0.9	1.8	-	mA
		5V	V_{OL}=0.5V	1.7	3.0	-	mA
I_{OH1}	BZ，$\overline{BZ}$	3V	V_{OH}=2.7V	-0.9	-1.8	-	mA
		5V	V_{OH}=4.5V	-1.7	-3.0	-	mA
I_{OL1}	DATA	3V	V_{OL}=0.3V	0.9	1.8	-	mA
		5V	V_{OL}=0.5V	1.7	3	-	mA
I_{OH1}	DATA	3V	V_{OH}=2.7V	-0.9	-1.8	-	mA
		5V	V_{OH}=4.5V	-1.7	-3	-	mA
I_{OL2}	LCD COM Sink Current	3V	V_{OL}=0.3V	80	160	-	μA
		5V	V_{OL}=0.5V	180	360	-	μA
I_{OH2}	LCD COM Source Current	3V	V_{OH}=2.7V	-40	-80	-	μA
		5V	V_{OH}=4.5V	-90	-180	-	μA
I_{OL3}	LCD SEG Sink Current	3V	V_{OL}=0.3V	50	100	-	μA
		5V	V_{OL}=0.5V	120	240	-	μA
I_{OH3}	LCD SEG Source Current	3V	V_{OH}=2.7V	-30	-60	-	μA
		5V	V_{OH}=4.5V	-70	-140	-	μA
R_{PH}	Pull-high Resistor	3V	DATA，$\overline{WR}$，$\overline{CS}$，$\overline{RD}$	100	200	300	kΩ
		5V		50	100	150	kΩ

AC Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	3V	On-chip RC oscillator	22	32	40	kHz
		5V		24	32	40	kHz
f_{SYS2}	System Clock	3V	External clock source	-	32	-	kHz
		5V		-	32	-	kHz
f_{LCD1}	LCD Frame Frequency	3V	On-chip RC oscillator	44	64	80	Hz
		5V		48	64	80	Hz
f_{LCD2}	LCD Frame Frequency	3V	External clock source	-	64	-	Hz
		5 V		-	64	-	Hz
t_{COM}	LCD COM Period	-	n: Number of COM	-	n/f_{LCD}	-	s
f_{CLK1}	Serial Data Clock ($\overline{WR}$ pin)	3V	Duty cycle 50%	-	-	150	kHz
		5V				300	
f_{CLK2}	Serial Data Clock ($\overline{RD}$ pin)	3V	Duty cycle 50%	-	-	75	kHz
		5V				150	
f_{TONE}	Buzzer output Frequency	-	Built-in RC oscillation	-	2.0/ 4.0	-	kHz
t_{CS}	Serial Inter face Reset Pulse Width (Figure3)	-	$\overline{CS}$	-	250	-	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure1)	3V	Write mode	3.34	-	-	μs
			Read mode	6.67			
		5V	Write mode	1.67	-	-	
			Read mode	3.34			
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure1)	3V	-	-	120	-	ns
		5V					
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure2)	3V	-	-	120	-	ns
		5V					
t_h	Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure2)	3V	-	-	120	-	ns
		5V					
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure3)	3V	-	-	100	-	ns
		5V					
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure3)	3V	-	-	100	-	ns
		5V					

Timing test diagram

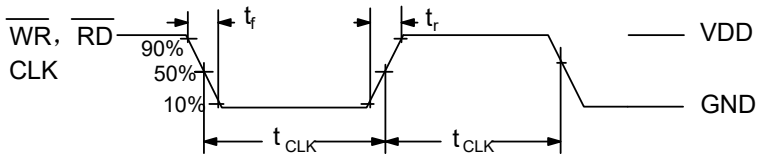


Figure 1. $\overline{WR}$，$\overline{RD}$ CLK timing diagrams

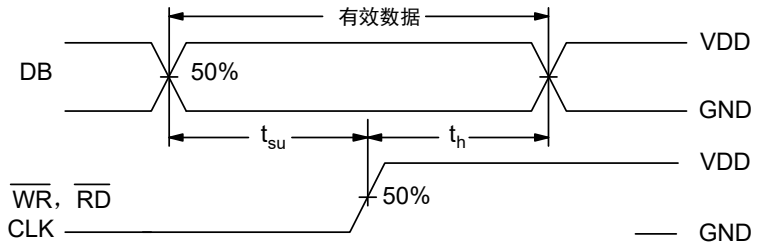


Figure 2. Serial data establishment and maintenance timing

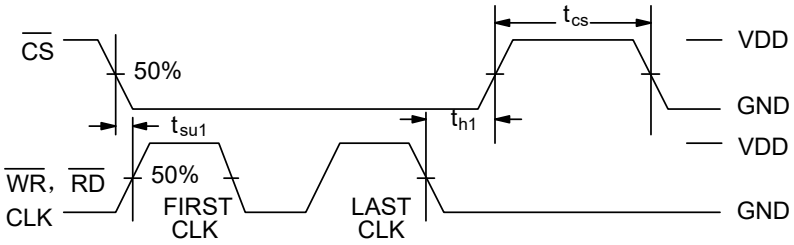
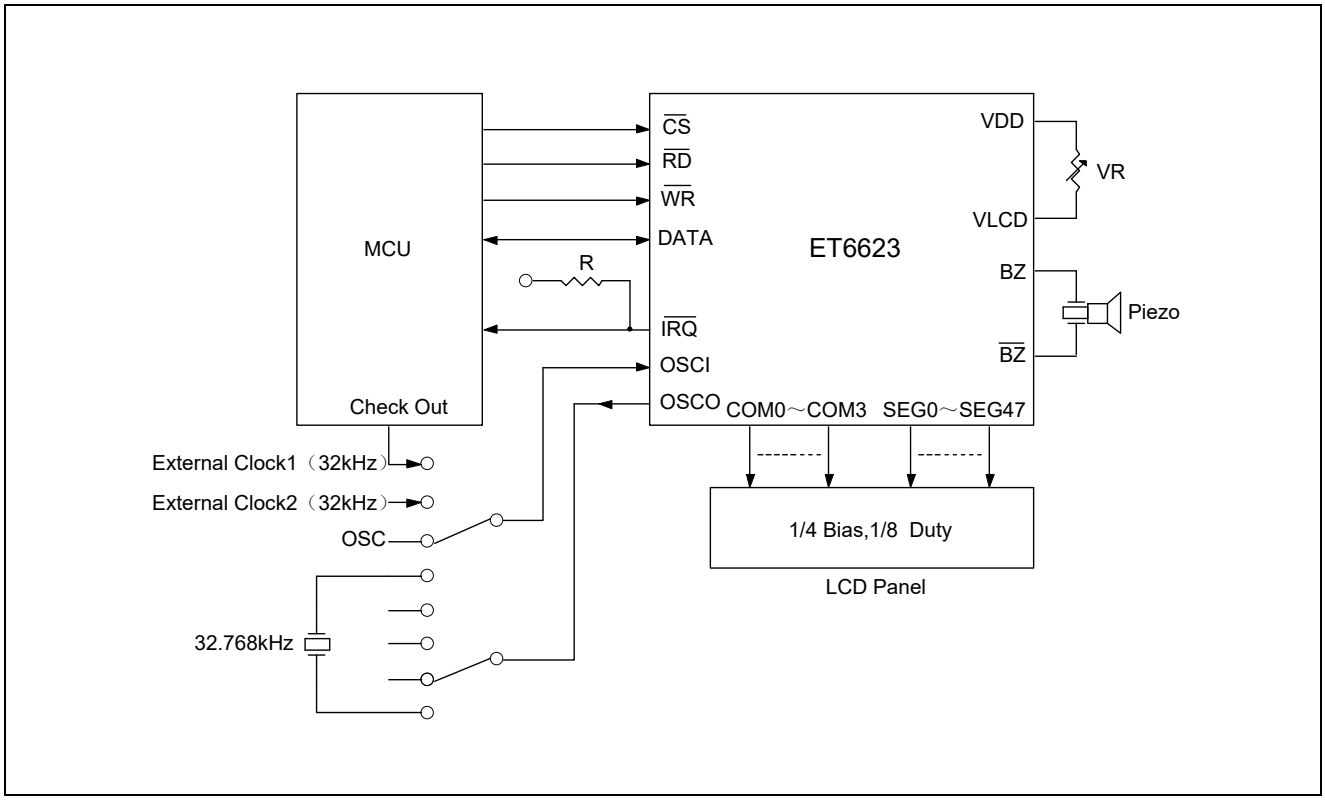


Figure 3. $\overline{CS}$ establish and maintain timing

Application Circuits

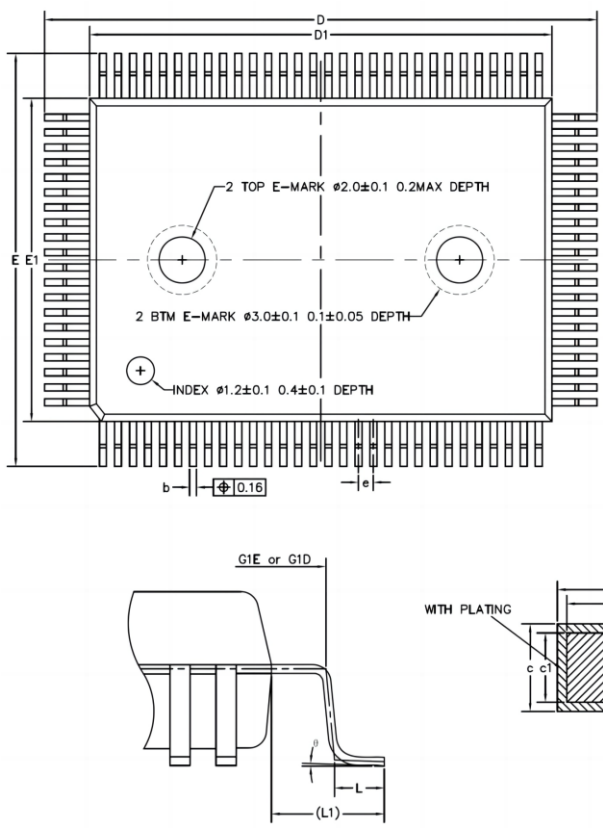


Note1: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the MCU.
The voltage applied to VLCD pin must not higher than VDD.
Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, V_R=15k±20%.
Adjust R (external pull-high resistance) to fit user's time base clock.

Note2: Initialization process required to add "NORMAL" command in order to avoid program into non-normal operating mode.

Package Dimension

QFP100



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	3.30
A1	0.10	–	0.40
A2	2.65	2.75	2.85
A3	1.20	1.30	1.40
b	0.27	–	0.37
b1	0.27	0.30	0.33
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	23.60	23.90	24.20
D1	19.90	20.00	20.10
E	17.60	17.90	18.20
E1	13.90	14.00	14.10
e	0.55	0.65	0.75
G1D		22.00REF	
G1E		16.00REF	
L	0.60	0.80	1.00
L1		1.95REF	
θ	0°	2°	8°
θ1	11°	13°	15°
θ2	3°	5°	7°

Unit：mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2015-08-18	Original Version	Wanggp	Wanggp	Zhujl
1.1	2019-02-28	Update Package Size	Wanggp	Wanggp	Liujy
1.2	2023-8-16	Update Format	Zoucm	Shib	Shib