ET6143 - Constant Current Matrix LED Controller

General Description

ET6143 is a constant current array LED controller ,which supports up to 10×12 array output and each point has 256 steps PWM current adjustment function.

ET6143 uses the I^2C interface and supports continuous read and write mode as well. It can set a variety of display effects by setting multiple Internally integrated registers.

ET6143 is mainly used in the display driver of household appliances, with the advantages of rich display effect and simple operation.

Features

- 12 constant current driver channels, max output current 50mA
- Support 1-10 scan application, the maximum application matrix is 10×12
- Each point supports 256 steps brightness adjustment
- I^2C interface, two chip-address can be set
- Oscillation mode: built in RC oscillation（1MHz±10%）
- Built in power on reset circuit
- Built in automatic blanking circuit
- Package: SOP28(ET6143M),EQSOP28(ET6143S),QFN28(ET6143Y)

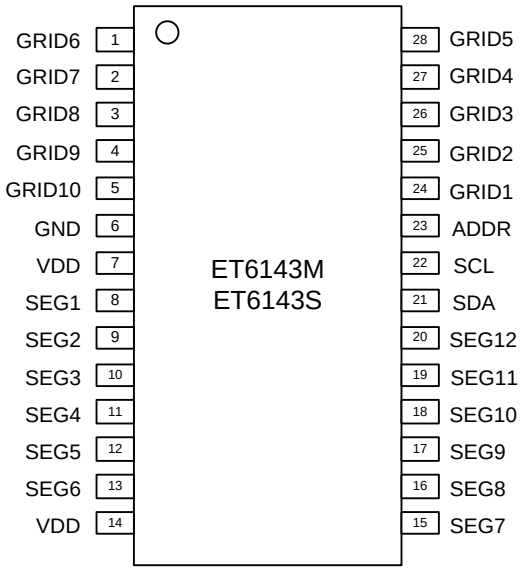
Device Information

Part No.	Package	Size
ET6143M	SOP28	7.6mm × 17.5mm
ET6143S	EQSOP28	3.8mm × 9.8mm
ET6143Y	QFN28	4mm × 4mm

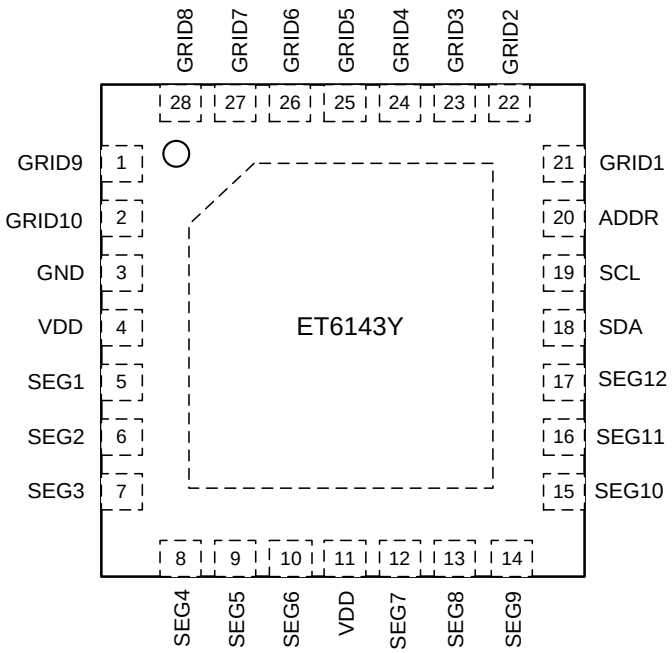
Application

- Household appliances, Toy display
- Smart portable devices, Smart audio

Pin Assignments



ET6143M (SOP28)/ET6143S(EQSOP28)



ET6143Y (QFN28)

Figure 1. Pin Assignments (Top View)

Pin. Function

Pin No.		Name	Function
QFN28	SOP28/EQSOP28		
21~28,1~2	24~28,1~5	GRID1~GRID6	Grid output, connected to LED cathode
3	6	GND	GND
4,11	7,14	VDD	Supply voltage
5~10,12~17	8~13,15~20	SEG1~SEG12	Segment output, connected to LED anode
18	21	SDA	I^2C data input
19	22	SCL	I^2C clock input
20	23	ADDR	Chip-address select

Block Diagram

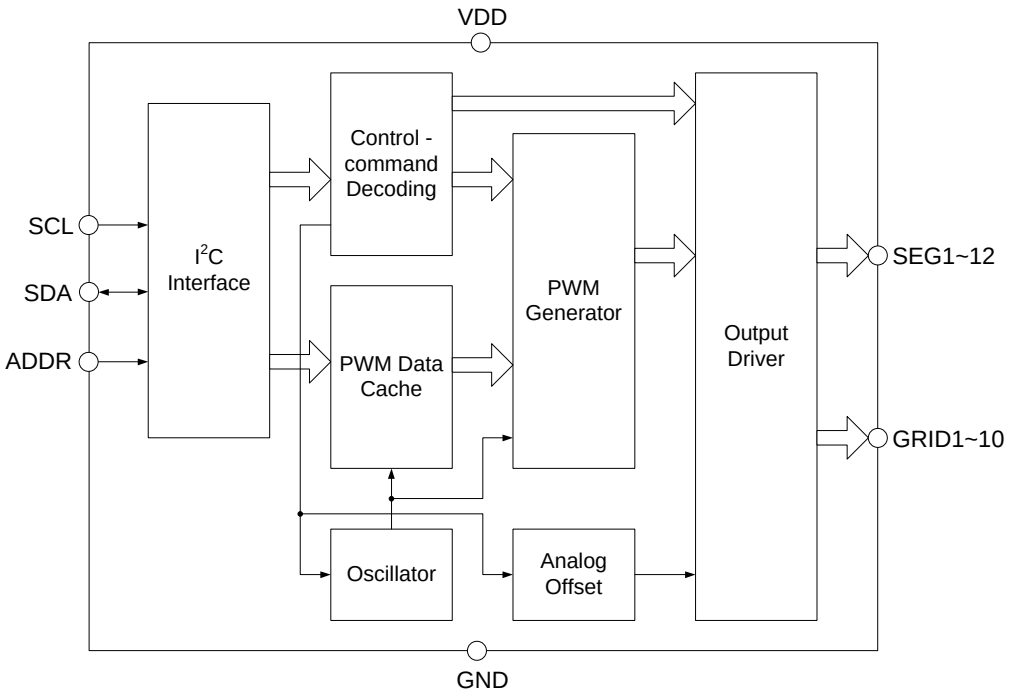


Figure 2. Block Diagram

Functions Description

Serial Port Interface

MCU can transmit data with ET6143 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET6143 will send a low level response signal with one period width to the SDA port. During the reading mode, ET6143 will not send response signal and the host will send a high response signal one period width to the SDA.

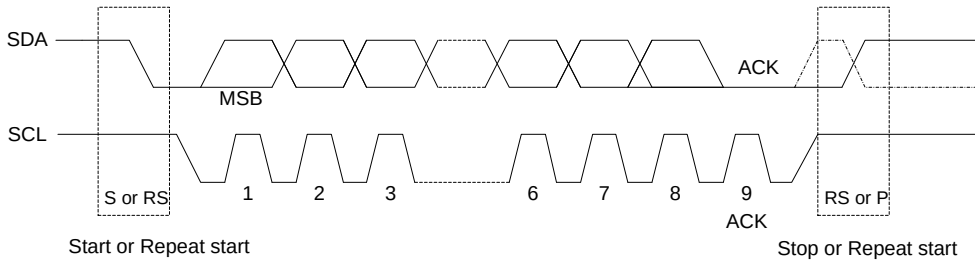


Figure 3. I²C Write Mode

Note：ACK=Acknowledge

MSB=Most Significant Bit

S=Start Conditions RS=Restart Conditions P=Stop Conditions

Fastest Transmission Speed =400KBITS/S

Restart: SDA-level turnover as expressed by the dashed line waveform

Chip-Address

ET6143 has 2 chip-address:

ADDR pin connect signal	Chip-Address(7-bit)
VDD	0110011b
GND	0110010b

I²C Writing Command Register Interface Protocol (continuous)：

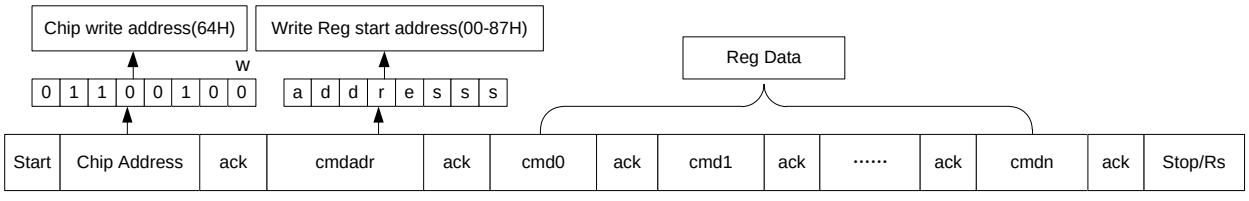


Figure 4. I²C Writing Command Register Protocol (continuous)

- Start = Start Conditions
- Chip Address = Write register address = 0110010+0(w)b
- ack = Acknowledge from ET6143
- Write Reg start address byte = cmdadr (REG's 8bit address)
- ack = Acknowledge from ET6143
- Command Reg data 0=cmd0(Command data)
- ack = Acknowledge from ET6143
- ……
- Command Reg data n=cmdn(Command data)
- ack = Acknowledge from ET6143
- Stop/Rs=Stop Condition/Restart Condition

I²C Writing Command Register Interface Protocol (single)：

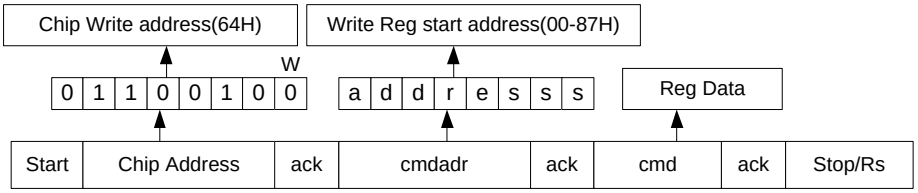


Figure 5. I²C Writing Command Register Protocol (single)

- Start =Start Conditions
- Chip Address = Write register address = 0110010+0(w)b
- ack = Acknowledge from ET6143
- Write Reg start address byte = cmdadr(REG's 8bit address)
- ack = Acknowledge from ET6143
- Command Reg data =cmd(Command data)
- ack = Acknowledge from ET6143
- Stop

I²C Reading Command Register Interface Protocol(continuous)

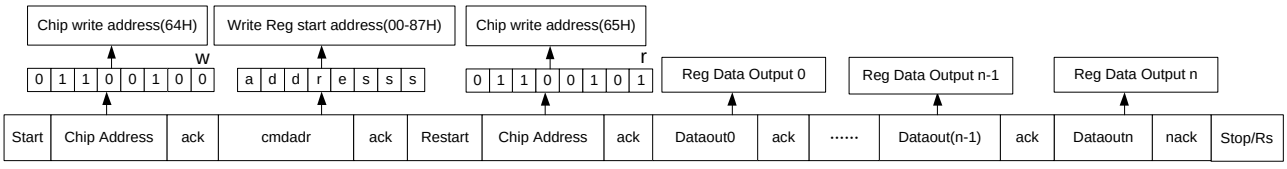


Figure 6. I²C Reading Command Register Interface Protocol(continuous)

- Start =Start Conditions
- Chip Address = Write register address = 0110010+0(w)b
- ack = Acknowledge from ET6143
- Write Reg start address byte = cmdadr(REG's 8bit address)

- ack = Acknowledge from ET6143
- Restart = Restart condition
- Chip address = Read register address= 0110010+1(w)b
- ack = Acknowledge from ET6143
- Dataout0=Register data output 0
- ack=Acknowledge from Host
- ……
- Dataoutn=Register data output n
- nack=No Acknowledge from Host
- Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol(single)

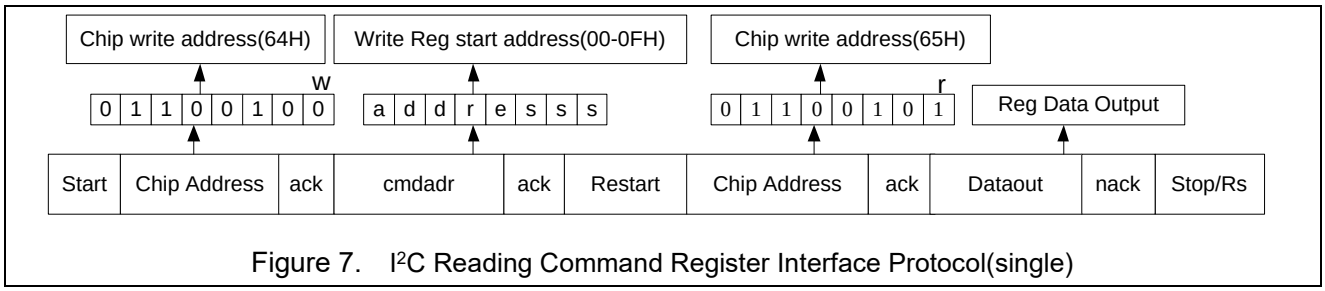


Figure 7. I²C Reading Command Register Interface Protocol(single)

- Start =Start Conditions
- Chip Address = Write register address = 0110010+0(w)b
- ack = Acknowledge from ET6143
- Write Reg start address byte = cmdadr(REG's 8bit address)
- ack = Acknowledge from ET6143
- Restart = Restart condition
- Chip address = Read register address= 0110010+1(w)b
- ack = Acknowledge from ET6143
- Dataout=Register data output
- nack=No Acknowledge from Host
- Stop/Rs=Stop Condition/Restart Condition

Register Map

Addr	Description
00H~03H	Status Control Register
10H~87H	PWM Data Register

Status Control Register

Addr: 00h			Control Register 1			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
00H	7:3	Soft_ Reset	00000	W/R	Write 11011b to reset all register, All other data are invalid	
	2:1	RFU	00	W/R	00	1MHz
					01	2MHz
					10	4MHz
					11	8MHz
	0	Shutdown	0	W/R	0	Shutdown
					1	Operating mode
Addr: 01h			**Control Register 2**			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
01H	7：6	RFU	00	-	-	
	5：2	Scan rows	0110	W/R	1010	10 Grids
					……	……
					0110	6 Grids (default)
					……	……
					0001	1 Grids
					Note	0000,1101~1111 is invalid
	1：0	Line feed time	00	W/R	00	4 PWM clock cycles
					01	8 PWM clock cycles
					10	12 PWM clock cycles
					11	16 PWM clock cycles
Addr: 02h			**Control Register 3**			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
02H	7:4	Chip ID	0110	R	Chip ID	
	3:2	SEG Blanking	01	W/R	SEG Blanking	
					00	Disable blanking
					01	Weak level blanking
					10	Middle level blanking
					11	High level blanking
	1:0	GRID Blanking	00	W/R	GRID Blanking	
					0X	Disable blanking
					10	Weak blanking
					11	High level blanking

Addr: 03h			Control Register 4			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
03H	7：6	RFU	0	-	-	
	5:1	Brightness	01111	W/R	SEG port output constant current	
					11111	50mA
					11110	48.75mA
					……	……
					01111	30mA (default)
					……	……
					0000	11.25mA
	0	Status control	0	W/R	0	Display off
					1	Display on
Addr: 10~87h			**PWM Registers**			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
10~87H	7:0	PWM DATA	00H	W/R	00H	0/255
					……	
					FFH	255/255

Note: After power on, you can configure other registers only after the 00 register is set to operating mode.

When the chip is in the shutdown state, other registers cannot be written.

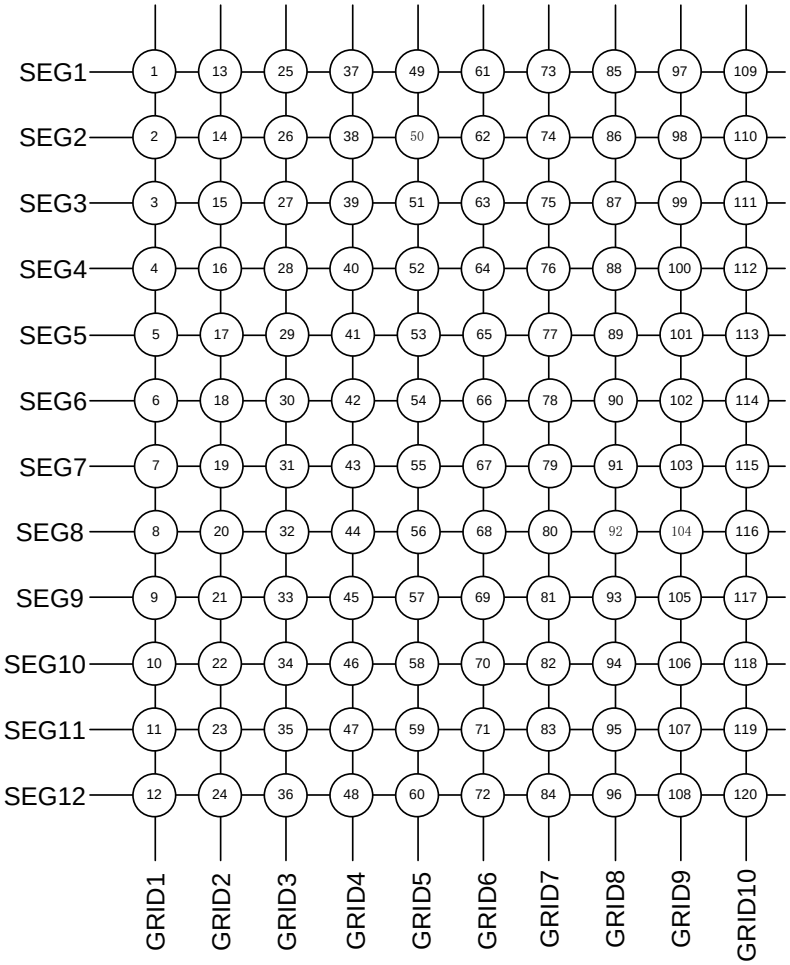


Figure 8. Output Matrix Diagram

PWM Data Register

Addr	Description	Addr	Description	Addr	Description	Addr	Description
10H	LED1PWM	11H	LED2PWM	12H	LED3PWM	13H	LED4PWM
14H	LED5PWM	15H	LED6PWM	16H	LED7PWM	17H	LED8PWM
18H	LED9PWM	19H	LED10PWM	1AH	LED11PWM	1BH	LED12PWM
1CH	LED13PWM	1DH	LED14PWM	1EH	LED15PWM	1FH	LED16PWM
20H	LED17PWM	21H	LED18PWM	22H	LED19PWM	23H	LED20PWM
24H	LED21PWM	25H	LED22PWM	26H	LED23PWM	27H	LED24PWM
28H	LED25PWM	29H	LED26PWM	2AH	LED27PWM	2BH	LED28PWM
2CH	LED29PWM	2DH	LED30PWM	2EH	LED31PWM	2FH	LED32PWM
30H	LED33PWM	31H	LED34PWM	32H	LED35PWM	33H	LED36PWM
34H	LED37PWM	35H	LED38PWM	36H	LED39PWM	37H	LED40PWM
38H	LED41PWM	39H	LED42PWM	3AH	LED43PWM	3BH	LED44PWM
3CH	LED45PWM	3DH	LED46PWM	3EH	LED47PWM	3FH	LED48PWM
40H	LED49PWM	41H	LED50PWM	42H	LED51PWM	43H	LED52PWM
44H	LED53PWM	45H	LED54PWM	46H	LED55PWM	47H	LED56PWM
48H	LED57PWM	49H	LED58PWM	4AH	LED59PWM	4BH	LED60PWM

4CH	LED61PWM	4DH	LED62PWM	4EH	LED63PWM	4FH	LED64PWM
50H	LED65PWM	51H	LED66PWM	52H	LED67PWM	53H	LED68PWM
54H	LED69PWM	55H	LED70PWM	56H	LED71PWM	57H	LED72PWM
58H	LED73PWM	59H	LED74PWM	5AH	LED75PWM	5BH	LED76PWM
5CH	LED77PWM	5DH	LED78PWM	5EH	LED79PWM	5FH	LED80PWM
60H	LED81PWM	61H	LED82PWM	62H	LED83PWM	63H	LED84PWM
64H	LED85PWM	65H	LED86PWM	66H	LED87PWM	67H	LED88PWM
68H	LED89PWM	69H	LED90PWM	6AH	LED91PWM	6BH	LED92PWM
6CH	LED93PWM	6DH	LED94PWM	6EH	LED95PWM	6FH	LED96PWM
70H	LED97PWM	71H	LED98PWM	72H	LED99PWM	73H	LED100PWM
74H	LED101PWM	75H	LED102PWM	76H	LED103PWM	77H	LED104PWM
78H	LED105PWM	79H	LED106PWM	7AH	LED107PWM	7BH	LED108PWM
7CH	LED109PWM	7DH	LED110PWM	7EH	LED111PWM	7FH	LED112PWM
80H	LED113PWM	81H	LED114PWM	82H	LED115PWM	83H	LED116PWM
84H	LED117PWM	85H	LED118PWM	86H	LED119PWM	87H	LED120PWM

Note: Each address has 8bits of data corresponding to the PWM order of that point (256 steps).

The default value for each set of registers is 00H.

Display cycle

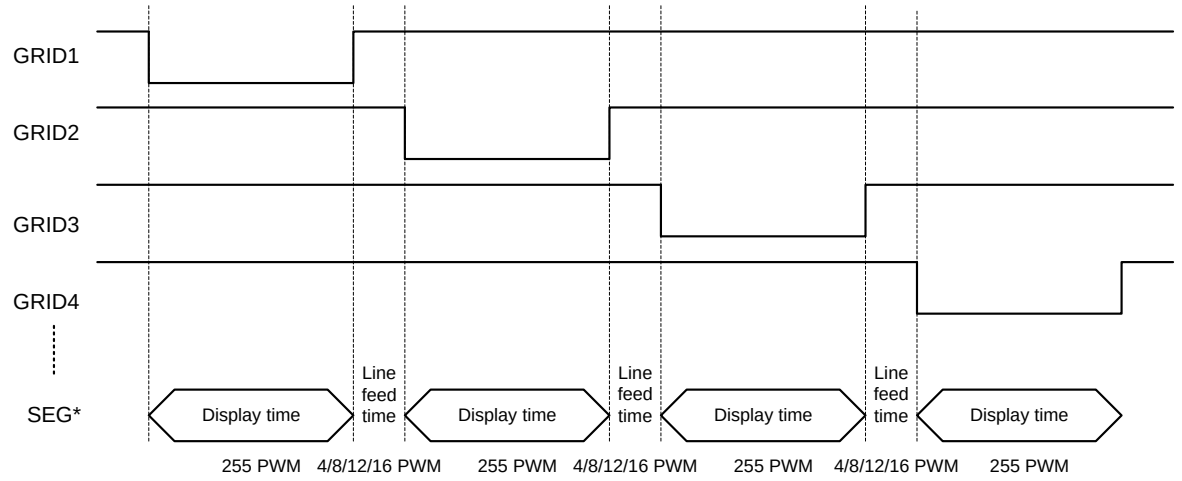


Figure 9. Display Cycle: Scan line × (4/8/12/16 Line feed time+255 steps PWM time)

Absolute Maximum Ratings

(Unless otherwise noted ,T_A=25℃)

Symbol	Characteristic	Rating	Unit
V_{DD}	Supply voltage	-0.5~6.0	V
V_I	Input Voltage	-0.5~V_{DD}+0.5	V
I_{O1}	LED SEG drive output current	-55	mA
I_{O2}	LED GRID drive output current	660	mA
P_{DMAX}	Power Dissipation（QFN28/EQSOP28）	1250	mW
	Power Dissipation（SOP28）	850	
θ_{JA}	Thermal Resistance（QFN28/EQSOP28）	46	°C/W
	Thermal Resistance（SOP28）	72	
T_J	Junction Temperature	-40～150	°C
T_{STG}	Storing Temperature	-65～150	°C
ESD	HBM	±2	KV
	CDM	±1	KV

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{IH}	Logic high level	0.6V_{DD}	—	V_{DD}	V
V_{IL}	Logic low level	0	—	0.25V_{DD}	*V*
T_A	Operating Temperature	-40		+85	°C

Electrical Characteristics

(Unless otherwise noted, V_{DD}=5V ,T_A=25℃)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage			5.0		V
V_{IH}	Logic high level	SCL, SDA	0.6×V_{DD}		V_{DD}	V
V_{IL}	Logic low level	SCL, SDA	0		0.25×V_{DD}	V
I_I	Input current	SDA, SCL：V_I = V_{DD}	-	-	±1	μA
I_{OH}	LED SEG drive output current	Default set is 30mA，SEGn,V_O=V_{DD} -1V	-27	-30	-33	mA
I_{OL}	LED GRID drive output current	GRID1~GRID10,V_O=0.5V	600		-	mA
I_{DD}	Dynamic current Dissipation	No load, Display off		3		mA
V_{RST}	Reset voltage			2.3		V
I_{SD}	Shutdown current			2	8	μA

Switching Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
T_{TZH}	SEGn Rising Time	C_L=300pF, R_L=1K			0.5	μs
T_{THZ}	GRIDn Falling Time	C_L=300pF			120	μs
C_I	Input capacitance	SDA , SCL			15	pF

I²C Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	0	-	400	KHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	1.3	-	-	μs
$t_{HD:STA}$	Hold Time(Repeated) START Condition	0.6	-	-	μs
t_{LOW}	Low Period of SCL Clock	1.3	-	-	μs
t_{HIGH}	HIGH Period of SCL Clock	0.6	-	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	0.6	-	-	μs
$t_{HD:DAT}$	Data Hold Time	0.1	-	0.9	μs
$t_{SU:DAT}$	Data Setup Time	100	-	-	ns
t_R	Data Hold Time2	-	20+0.1Cb[1]	300	ns
t_F	Data Hold Time2	-	20+0.1Cb[1]	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	0.6	-	-	μs

1: Cb=total capacitance of one bus line in PF unit.

I²C Timing Waveform

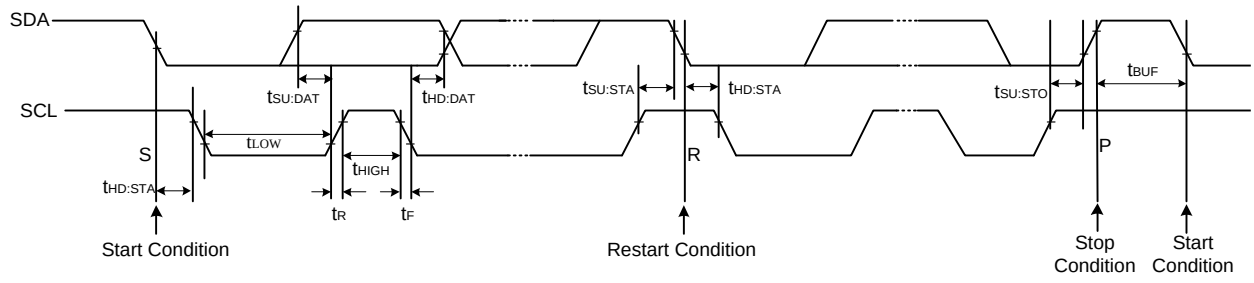


Figure 10. Definition of Timing for I²C Bus

Application circuit

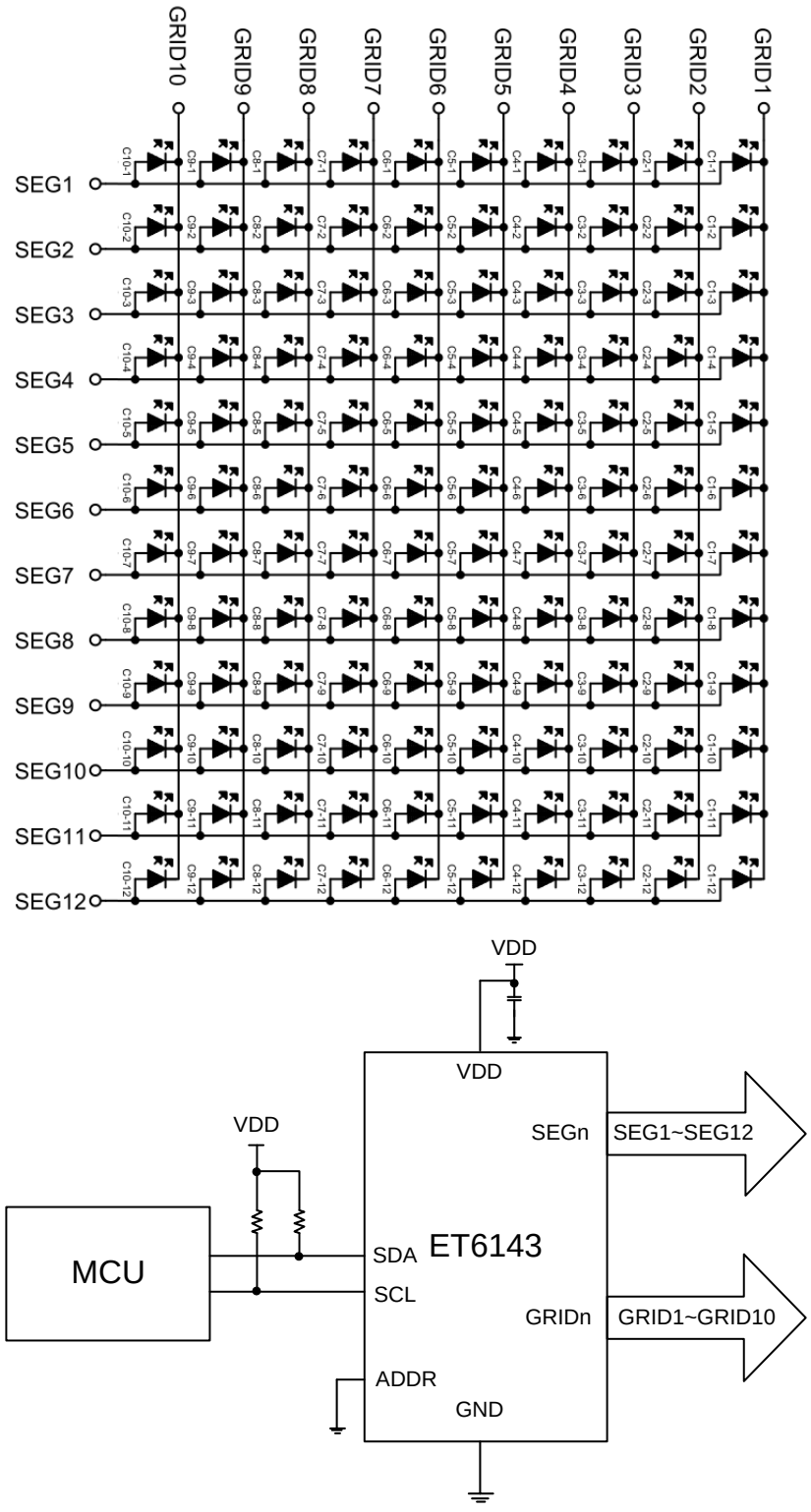
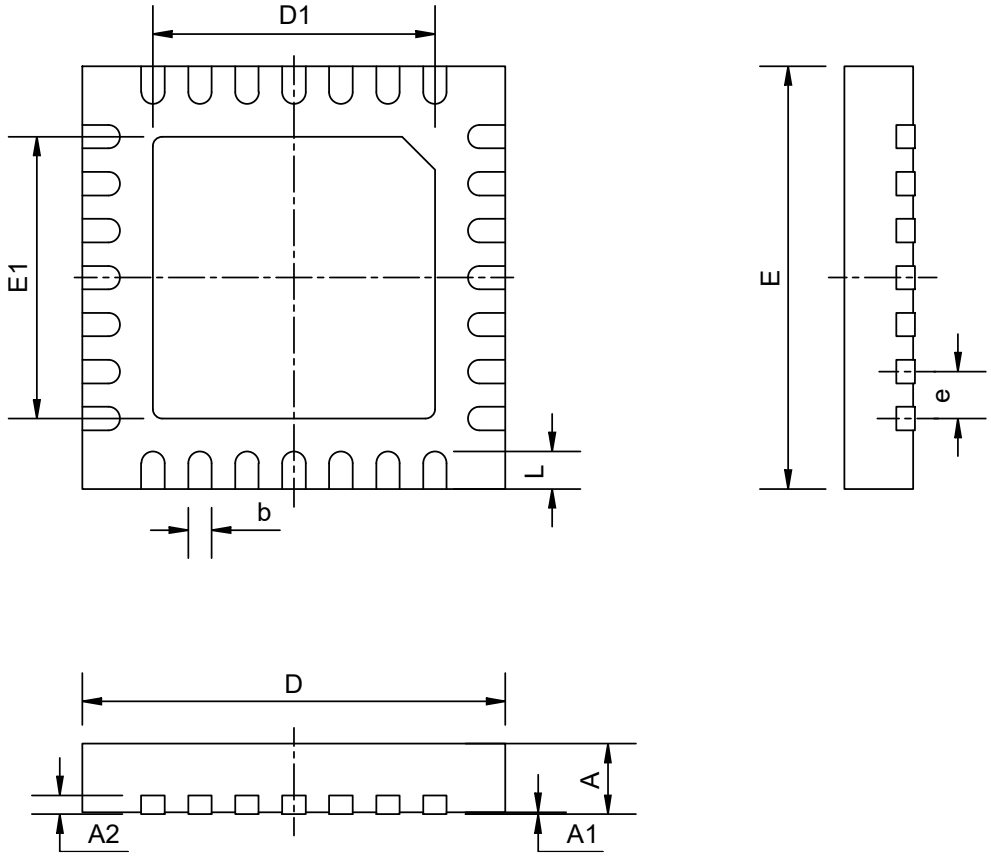


Figure 11. 10×12 LED Matrix Display Application Circuit

Note：This application circuit is only for reference.

Package

QFN28

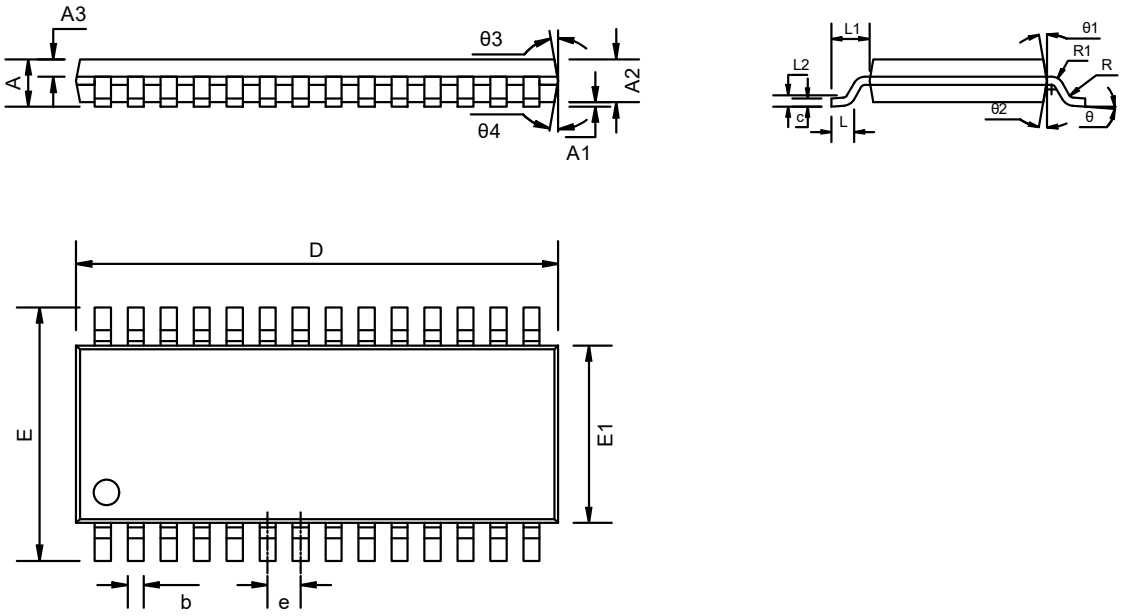


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	--	0.05
A2		0.20 REF	
b	0.15	0.20	0.25
D	3.95	4.00	4.05
E	3.95	4.00	4.05
D1	2.15	2.30	2.40
E1	2.15	2.30	2.40
e		0.40 BSC	
L	0.30	0.40	0.50

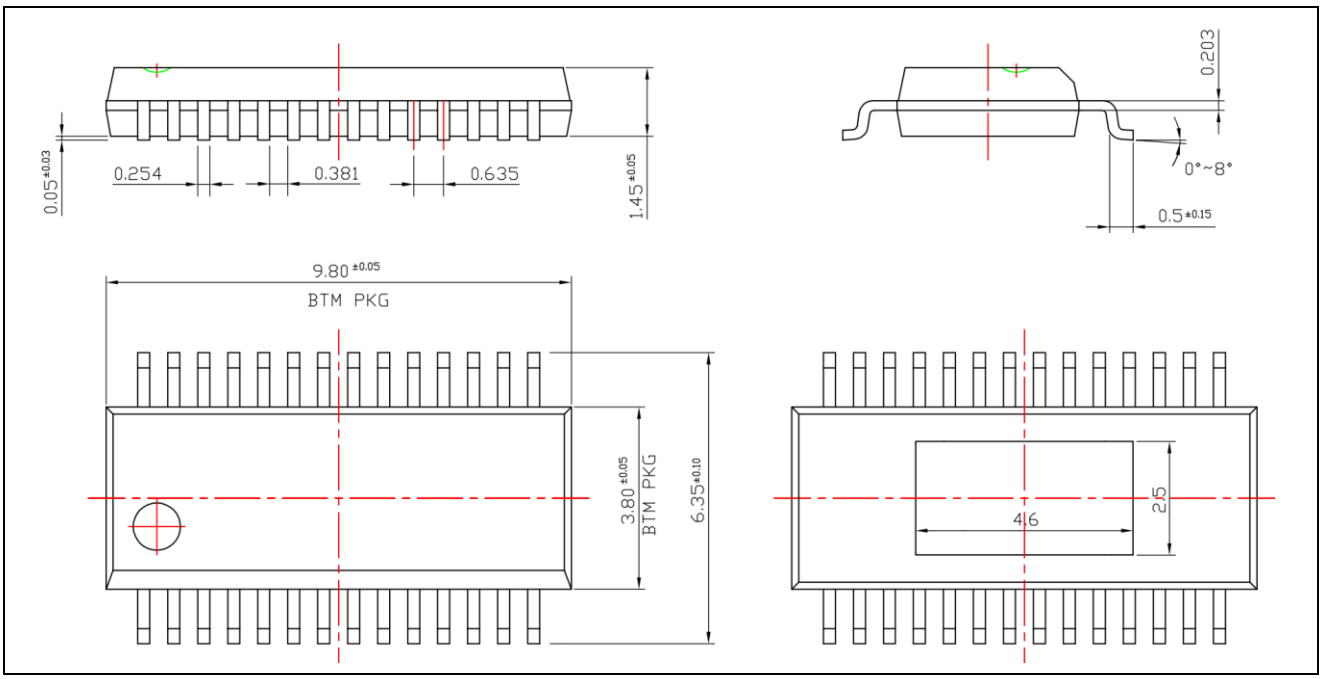
SOP28



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

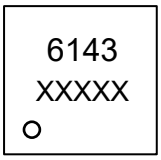
SYMBOL	MIN	NOM	MAX
A	--	--	2.95
A1	0.10	0.20	0.30
A2	2.25	2.45	2.65
A3	1.20	1.30	1.40
b	0.41	--	0.54
c	0.15	--	0.20
D	17.40	17.50	17.60
E	10.20	10.40	10.60
E1	7.50	7.60	7.70
e	1.27BSC		
L	0.40	0.60	0.80
L1	1.30REF		
L2	0.25BSC		
R	0.10	--	--
R1	0.10	--	--
θ	0°	--	8°
θ1	13°	15°	17°
θ2	6°	8°	10°
θ3	9.5°	11.5°	13.5°
θ4	6°	8°	10°

EQSOP28

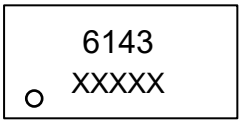


Marking

ET6143Y



ET6143M/S



XXXXX=Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2021-06-09	Original Version	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.1	2022-06-27	Update form	Shib	Shi Liang Jun	Shi Bo
1.2	2023-3-8	VIH to 0.6VDD	Shibo	Shi Liang Jun	Shi Bo
1.3	2024-6-17	Add description of 00H register	Shibo	Li Chen Xuan	Shi Bo