ET6930 - Constant Current Array LED Controller

General Description

ET6930 is designed for LED display with 96 dots constant current driver. The standard I^2C communication protocol is adopted. Internal integration of communication interface, data latch, LED constant current drive module. Especially suitable for small LED display driver, with high brightness, constant output current and other characteristics.

Features

- Up to 96 LEDs are supported
- Support 1～12 scan application, the maximum application matrix is 8 ×12 (8 SEG × 12 GRID)
- Output constant current driver
- 8 levels of brightness adjustment
- I^2C communication interface
- Built in RC oscillation
- Built in power on reset
- Package: SSOP24 (ET6930S)

Device Information

Part No.	Package	Size
ET6930S	SSOP24	8.65mm × 6.0mm

Application

- Household appliances, Toy display
- Smart portable devices, Smart audio

Pin Assignments

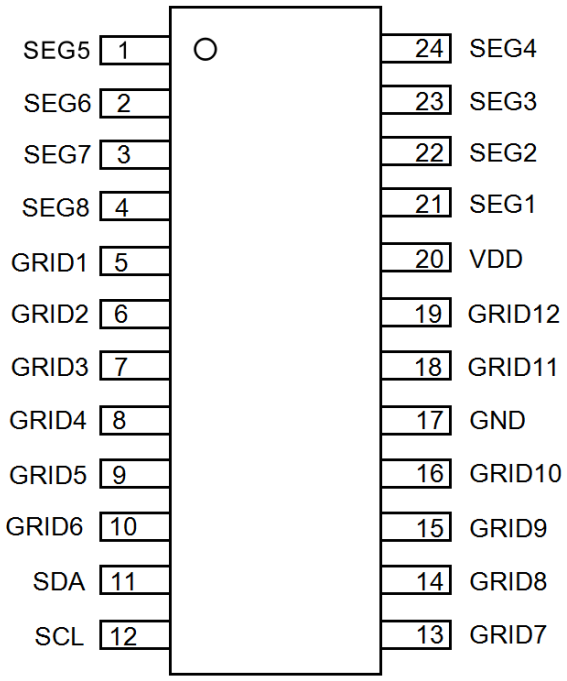


Figure 1. Pin Assignments (Top View)

Pin Description

Symbol	Pin number	Description
SEG1~SEG8	21~24,1~4	Segment output, connected to LED positive pole
GRID1~GRID12	5~10,13~16,18,19	Grid output, connected to LED negative pole
SDA	11	I^2C data input
SCL	12	I^2C clock input
GND	17	Ground
VDD	20	Power supply

Function Block Diagram

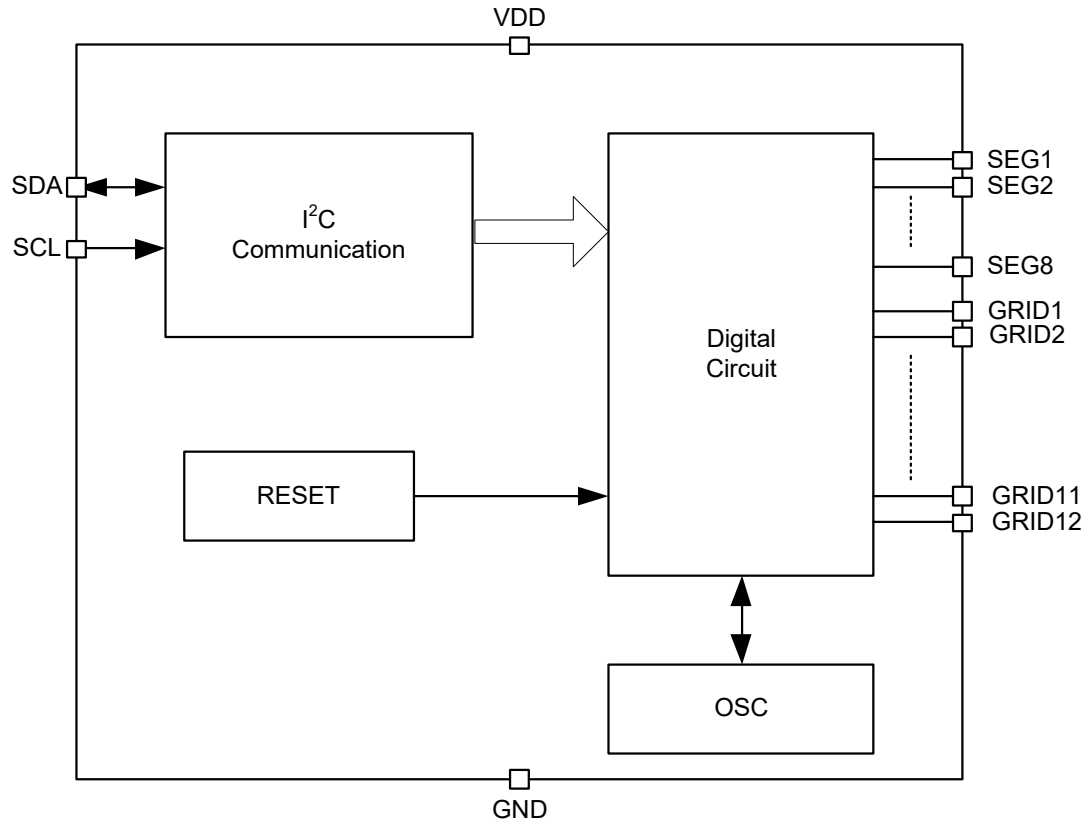


Figure 2. Function Block Diagram

Functions Description

Introduction

ET6930 is a constant current driver IC for LED display panel based on I²C communication protocol. It supports up to 8 Segs × 12 Girds output, and can adjust the number of scanning Grids through register configuration, so as to obtain larger single point drive current.

The traditional LED display panel constant voltage drive IC, when the number of lit led changes or the power supply voltage changes, the current of a single LED will change, which will affect the display effect and ET6930 adopts the constant current drive design, when the display mode is configured, the current of each LED will be constant, and will not fluctuate due to the number of lit led changes or the power supply voltage changes.

Serial Port Interface (I²C)

Bus Interface

MCU can transmit data with ET6930 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET6930 will send a low level response signal with one period width to the SDA port. During the reading mode, ET6930 will not send response signal and the host will send a high response signal one period width to the SDA.

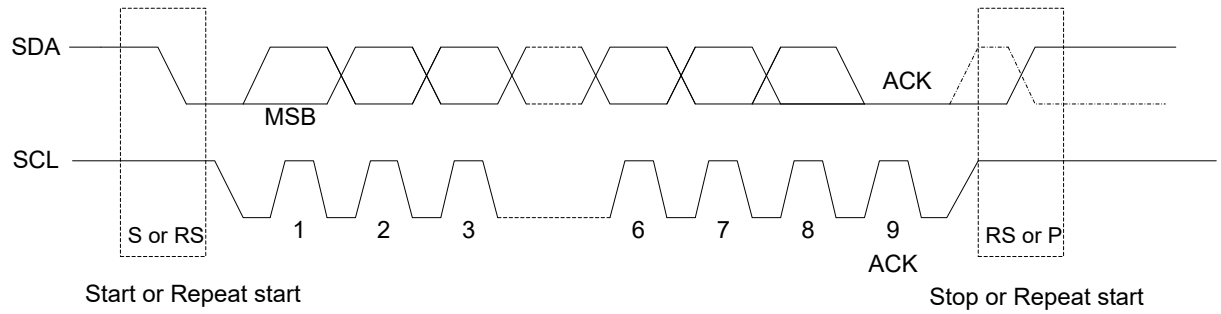


Figure 3. I²C write mode

Note：ACK=Acknowledge

MSB=Most Significant Bit

S=Start Conditions RS=Restart Conditions P=Stop Conditions

Fastest Transmission Speed =400KBITS/S

Restart: SDA-level turn over as expressed by the dashed line waveform

Chip-Address

Chip-Address	Description
84H(10000100B)	Only write mode is supported

I²C Writing Command Register Interface Protocol (continuous):

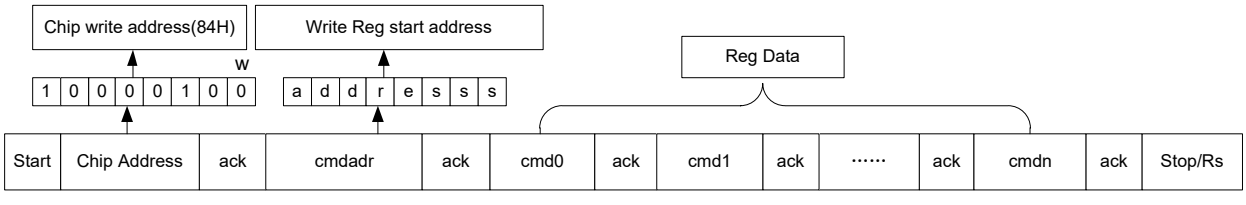


Figure 4. I²C Writing Command Register Protocol (continuous)

- Start = Start Conditions

- Chip Address = Write register address = 10000100
- ack = Acknowledge from ET6930
- Write Reg start address byte = cmdadr (REG's 8bit address)
- ack = Acknowledge from ET6930
- Command Reg data 0=cmd0(Command data)
- ack = Acknowledge from ET6930
- ……
- Command Reg data n=cmdn(Command data)
- ack = Acknowledge from ET6930
- Stop/Rs=Stop Condition/Restart Condition

I²C Writing Command Register Interface Protocol (single)：

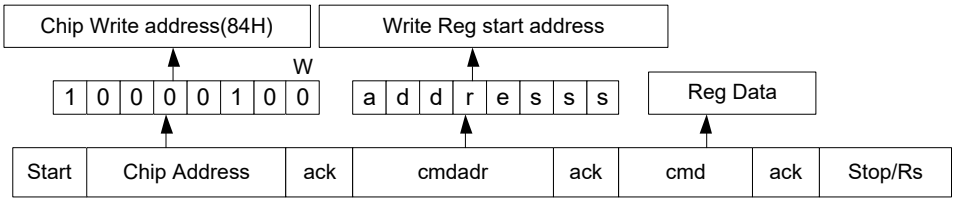


Figure 5. I²C Writing Command Register Protocol (single)

- Start =Start Conditions
- Chip Address = Write register address = 10000100
- ack = Acknowledge from ET6930
- Write Reg start address byte = cmdadr(REG's 8bit address)
- ack = Acknowledge from ET6930
- Command Reg data =cmd(Command data)
- ack = Acknowledge from ET6930
- Stop/Rs=Stop Condition/Restart Condition

Register Map

Addr	Description
00H~0BH	Display Data Register
10H~11H	Display Mode Register
12H	Status Control Register

Display Data Register

These register stores the display data of ET6930, with the address from 00H to 0BH, a total of 12 byte units, corresponding to the LED lights of the matrix connected to the SEGn and GRIDn pins respectively.

Addr	Parameter	Description	Defalt Value
00H	GRID1 Data	Grid1data<7:0> Corresponding control SEG8~SEG1	00H
01H	GRID2 Data	Grid2data<7:0> Corresponding control SEG8~SEG1	00H
02H	GRID3 Data	Grid3data<7:0> Corresponding control SEG8~SEG1	00H
03H	GRID4 Data	Grid4data<7:0> Corresponding control SEG8~SEG1	00H
04H	GRID5 Data	Grid5data<7:0> Corresponding control SEG8~SEG1	00H
05H	GRID6 Data	Grid6data<7:0> Corresponding control SEG8~SEG1	00H
06H	GRID7 Data	Grid7data<7:0> Corresponding control SEG8~SEG1	00H
07H	GRID8 Data	Grid8data<7:0> Corresponding control SEG8~SEG1	00H
08H	GRID9 Data	Grid9data<7:0> Corresponding control SEG8~SEG1	00H
09H	GRID10 Data	Grid10data<7:0> Corresponding control SEG8~SEG1	00H
0AH	GRID11 Data	Grid11data<7:0> Corresponding control SEG8~SEG1	00H
0BH	GRID12 Data	Grid12data<7:0> Corresponding control SEG8~SEG1	00H

Display Mode Register

Addr: 10h			Reset Register			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
10H	7:4	-	0000	-	-	
	3:0	Brightness	-	W	SEG port output constant current	
					0111	35mA
					0110	30.6mA
					0101	26.25mA
					……	……
					0000	4.37mA
Addr: 11h			**Reset Register**			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
11H	7:4	-	0000	-	-	
	3:0	Scan rows	-	W	Number of valid GRID scan rows	
					1011	12 row
					1010	11 row
					1001	10 row
					……	……
					0000	1 row

Note: The display mode reg should be configured after power on.

Status Control Register

Addr: 12h			Reset Register			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
12H	0	Shutdown	0	W	0	Shutdown
					1	Operating mode
	1	Status control	0	W	0	Display off
					1	Display on
	7:2	-	000000	-	-	Set to 0 please

Display Cycle

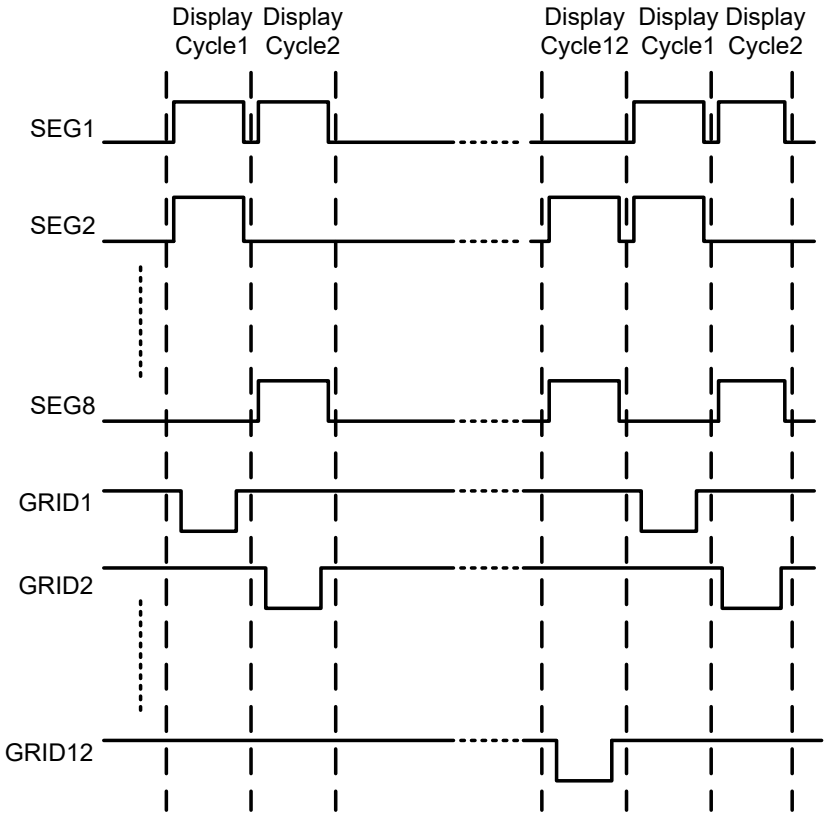


Figure 6. Data Display Cycle

Command Sequence

When power on for the first time, the state control register (12H) needs to be configured as 01h (that is, the circuit enters the normal working state).

Register writing order: state control register → display mode register → display data register → state control register.

Note: Once bit0 of the state control register is set to 0, when re-writing data, be sure to configure the state control register to 01h before performing other operations.

Software Flow Chart

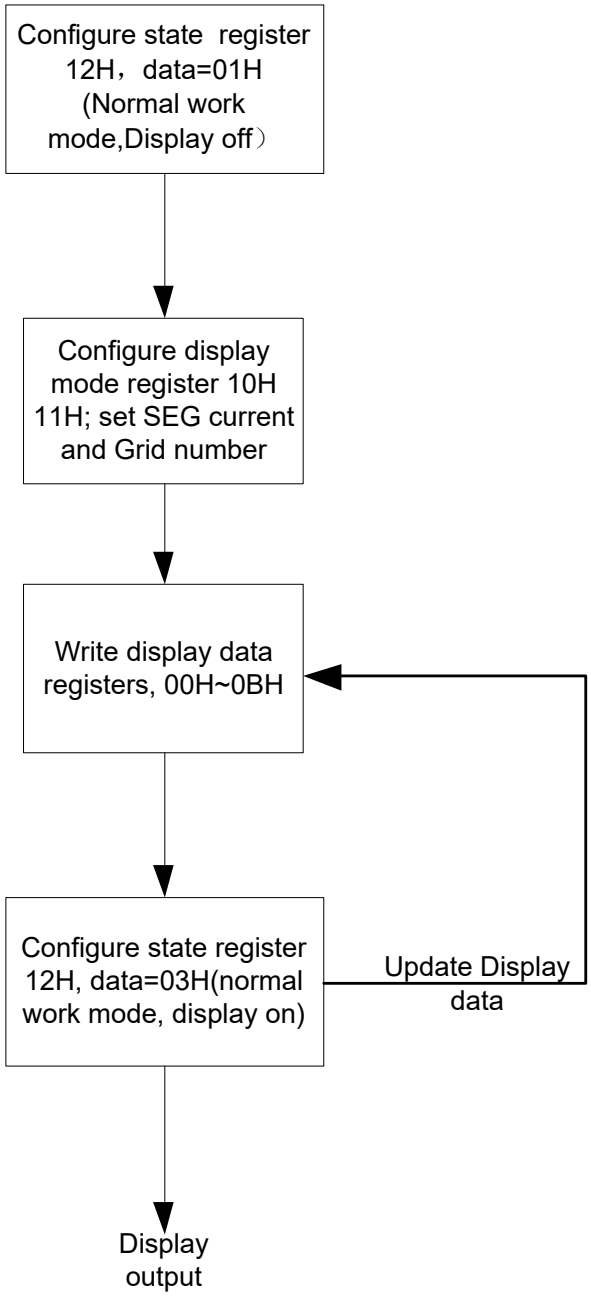


Figure 7. Instruction operation flow chart

Absolute Maximum Ratings

(Unless otherwise noted ,T_A = 25°C,GND = 0V)

Symbol	Parameter name	Condition	Value	Unit
V_{DD}	Supply Voltage		-0.3 ~ 6.0	V
I_{OS}	SEG drive current	V_{DD}=5V, T_A =25°C	-72	mA
I_{OG}	GRID drive current	V_{DD}=5V, T_A=25°C	600	mA
P_D	Max power deterioration		500	mW
θ_{JA}	Thermal resistance	SSOP24	128	°C/W
T_A	Junction temperature		-40~150	°C
T_{STG}	Store temperature		-65~150	°C

Recommended Operating Range

(Unless otherwise noted ,T_A = 25°C,GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
I_{DD}	Operate current			250	mA
V_{IH}	Input high voltage	0.7V_{DD}	-	V_{DD}	V
V_{IL}	Input low voltage	0	-	0.3V_{DD}	V
T_A	Operate temperature	-40		85	°C

DC Electrical Characteristics

(Unless otherwise noted ,T_A = 25°C,GND = 0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{SEG}	High level output current	V_{DD} = 5V V_O = V_{DD}-1V， ‘10H’ write 0x7	-31.5	-35	-38.5	mA
I_{OUT}	Low level output current	V_O = 0.8V		560	-	mA
I_{IN}	Input current	V_I = V_{DD}	-	-	±1	uA
V_{IH}	High level input voltage	SDA，SCL	0.7V_{DD}	-	-	V
V_{IL}	Low level input voltage	SDA，SCL	-	-	0.3V_{DD}	V
V_H	Hysteresis voltage	SDA，SCL	-	0.35	-	V
I_{DDDYN}	Dynamic current deterioration	No load, display off	-	-	1	mA
I_{SHDN}	Shutdown current	Shutdown enable			10	uA

AC Electrical Characteristics

(Unless otherwise noted, V_{DD} = 5V , GND = 0V, T_A=25°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_{ZH1}	Rising time	SEG1~8,C_L=300pF	-	-	2	us
T_{ZH2}	Rising time	GRID1~12,C_L=300pF	-	-	0.5	us
T_{ZH}	Dropping time	C_L=300pF, SEGn，GRIDn	-	-	120	us

I²CTiming Characteristics

(Unless otherwise noted, V_{DD} = 5V , GND = 0V, T_A=25°C)

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	-	-	400	KHz
t_{BUF}	Bus Free Time Between STOP and START Condition	1.3	-	-	μs
$t_{HD:STA}$	Hold Time(Repeated) START Condition	0.6	-	-	μs
t_{LOW}	Low Period of SCL Clock	1.3	-	-	μs
t_{HIGH}	High Period of SCL Clock	0.6	-	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	0.6	-	-	μs
$t_{HD:DAT}$	Data Hold Time	-	-	0.9	μs
$t_{SU:DAT}$	Data Setup Time	100	-	-	ns
t_R	Data Hold Time2		20+0.1Cb(1)	300	ns
t_F	Data Hold Time2		20+0.1Cb(1)	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	0.6	-	-	μs

Note1 : Cb=total capacitance of one bus line in PF.

I²C Timing Waveform

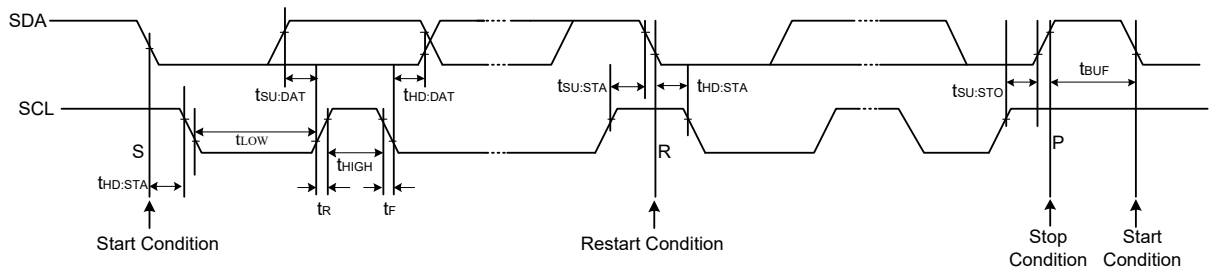
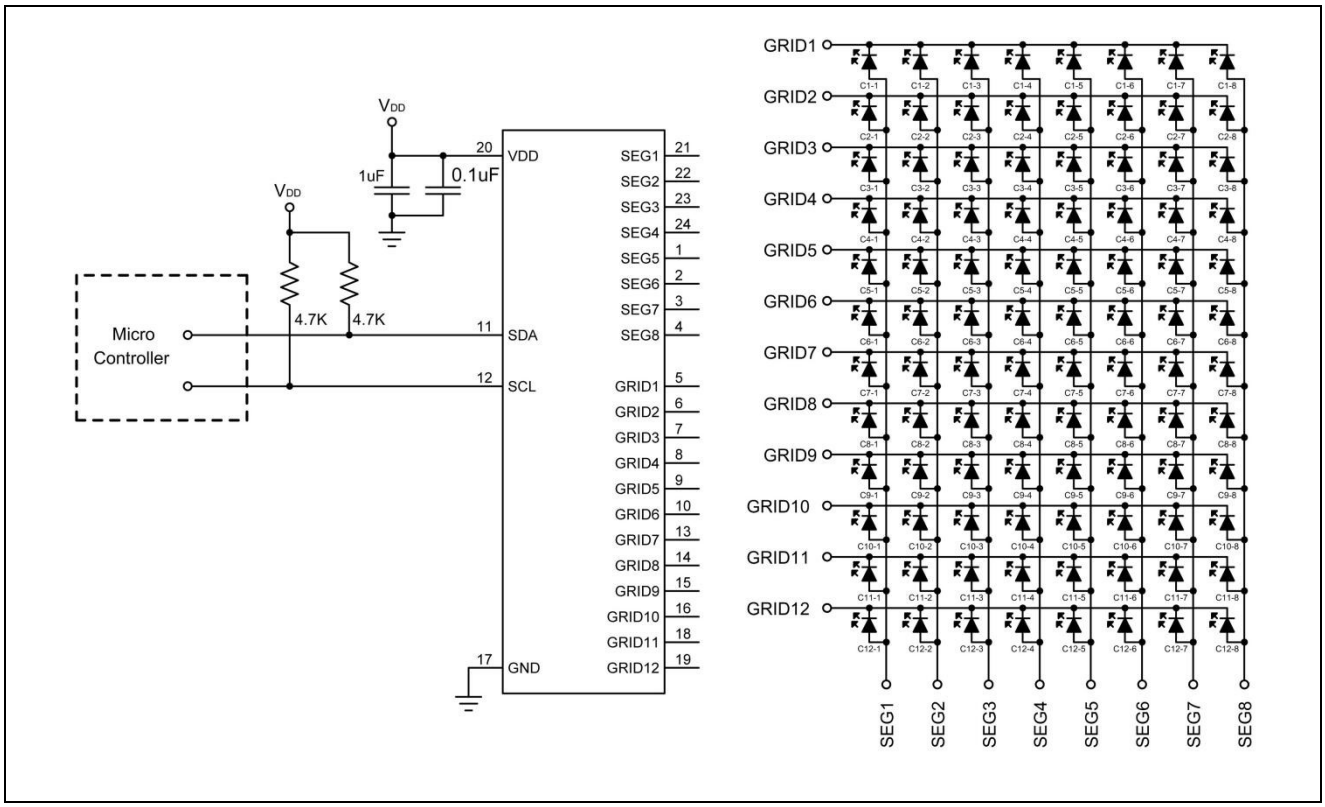


Figure 8. Definition of Timing for I²C Bus

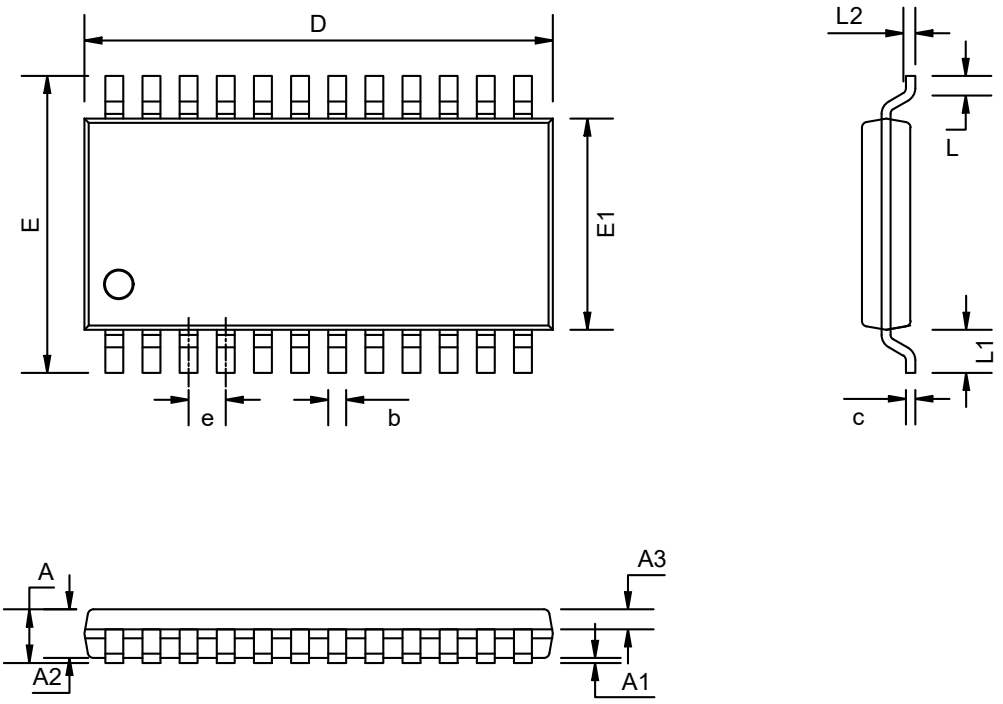
Application circuit



Note：This application circuit is only for reference, It is recommended that power filter capacitor should be close to the V_{DD} pin as far as possible.

Package

SSOP24



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

Symbol	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.34	0.39	0.44
b	0.23	0.28	0.33
c	0.10	-	0.19
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	0.635BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
L2	0.25BSC		

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2020-02-24	Original Version	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.1	2020-04-01	Updated Form	Shibo	Shi Liang Jun	Zhu Jun Li
1.2	2022-07-23	Updated Form	Shibo	Shi Liang Jun	Liujy