Common Anode of 8 Segments- 6 Bits LED Driver

General Description

ET1637 is a common anode LED digital tube drive control circuit with keyboard scanning interface, which is integrated with MCU digital interface, data latch, LED high voltage driver, keyboard scanning and other modules, using 2-wire serial interface. This product has excellent performance and reliable quality, and is mainly used in the display drive of induction cooker, microwave oven and small household appliances.

Features

- Power CMOS technology
- Display mode (8 segments × 6 bits),supports up to 48 LEDs and Common anode digital tube
- Support up to 16 keys (2×8bit)
- Support 8-level brightness adjustment
- Built in RC oscillation
- 2-wire serial interface (CLK, DIO)
- Built in power on reset
- Built in automatic blanking circuit
- Product name and package form:

Part No.	Package
ET1637M	SOP20
ET1637V	TSSOP20

Pin Assignments

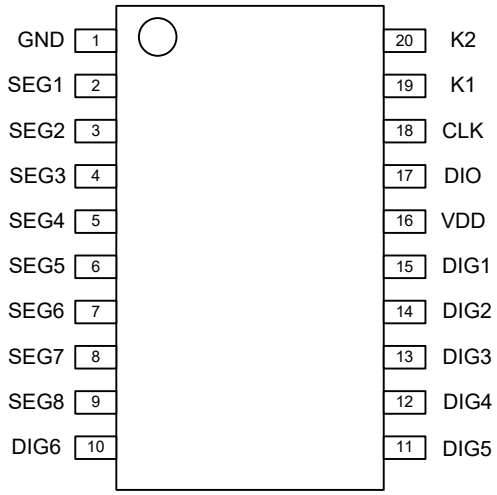


Figure 1. Pin Assignments (Top View)

Pin. Function

Pin No.	Symbol	Description
1	GND	Ground
2	SEG1	Segment output (Key scan), connected LED negative pole.
3	SEG2	Segment output (Key scan), connected LED negative pole.
4	SEG3	Segment output (Key scan), connected LED negative pole.
5	SEG4	Segment output (Key scan), connected LED negative pole.
6	SEG5	Segment output (Key scan), connected LED negative pole.
7	SEG6	Segment output (Key scan), connected LED negative pole.
8	SEG7	Segment output (Key scan), connected LED negative pole.
9	SEG8	Segment output (Key scan), connected LED negative pole.
10	DIG6	Bit output, connected LED positive pole.
11	DIG5	Bit output, connected LED positive pole.
12	DIG4	Bit output, connected LED positive pole.
13	DIG3	Bit output, connected LED positive pole.
14	DIG2	Bit output, connected LED positive pole.
15	DIG1	Bit output, connected LED positive pole.
16	VDD	Power supply.
17	DIO	Input data that changes at CLK low levels and transmitted at CLK high levels
18	CLK	Input/output data at rising edge.
19	K1	Key scan input port1, build in a pull up resistance.
20	K2	Key scan input port2, build in a pull up resistance.

Functions Description

The key scan matrix of ET1637 is composed of 8×2bit array:

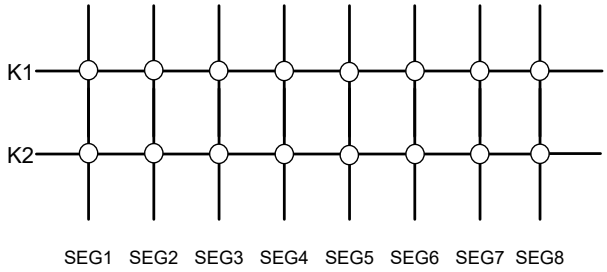


Figure 2. Key scan matrix

While key pressed, the read key data is as follows:

	SEG1	SEG2	SEG3	SEG4	SEG5	SG6	SEG7	SEG8
K1	1110_1111	0110_1111	1010_1111	0010_1111	1100_1111	0100_1111	1000_1111	0000_1111
K2	1111_0111	0111_0111	1011_0111	0011_0111	1101_0111	0101_0111	1001_0111	0001_0111

Note: When no key is pressed, the read key data is 1111_1111, with the low position in the front and the high position in the back.

Interface Description

Data from the microprocessor communicates with the ET1651 via a two-wire bus interface. When the data is input, the signal on DIO must remain unchanged when the CLK is high voltage. The signal on DIO can only change if the clock signal on CLK is at low level. When the initial condition of data input is high voltage CLK, DIO changes from high to low. The end condition is that DIO changes from low level to high level when CLK is high.

ET1637 data transmission with a response signal ACK, during the transmission of data, at the ninth clock of the clock line, the chip will generate an response signal ACK to pull down the DIO pin.

Data transmission (read key data time sequence):

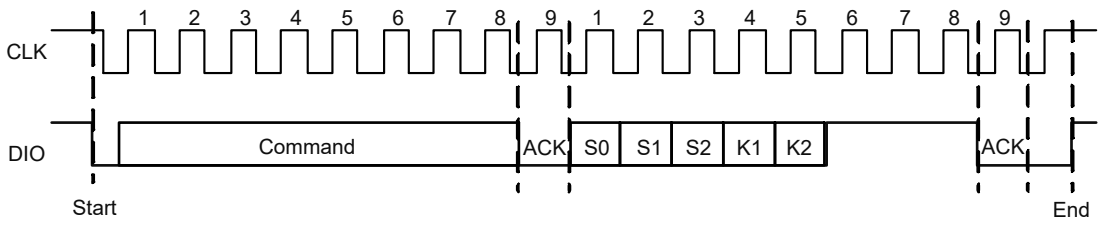


Figure 3. Data transmission

Command：Read key instruction.

S0, S1, S2, K1, K2 constitute the key code, S0, S1, S2 is the SEG code, K1, K2 is the K1 and K2 code

Write SRAM data addresses automatically increase by 1 mode

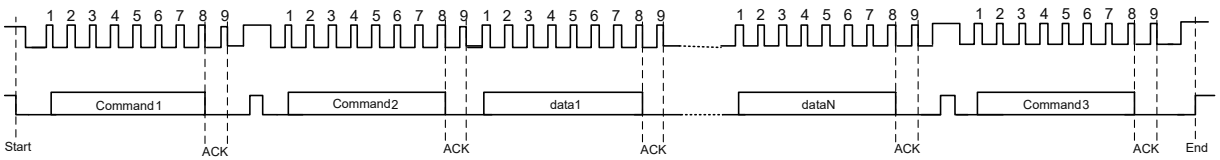


Figure 4. Automatic address adding mode

Command1：Set data command

Command2：Set data address

Data1 ~ N：Transfers display data to the address following the Command2

Command3：Displays control commands

Serial data transmission in fixed address mode

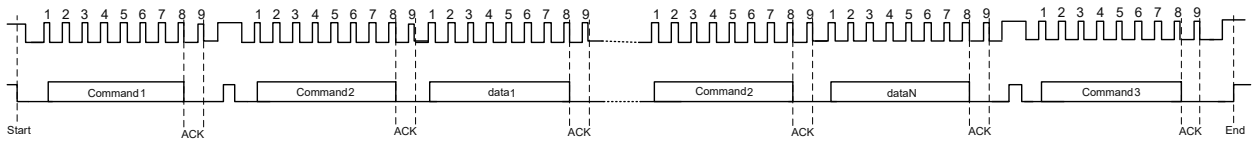


Figure 5. Fixed address mode

Command1：Set data command

Command2：Set display address 1

Data 1： Transfer display data to Command2 address

Command2：Display address n

Data N： Transmit display data to the last Command2 address

Command3：Display control command

Data Command

The command is used to set the display mode and LED driver status.

The first byte entered by DIO after the CLK falling edge serves as an instruction. After decoding, take the highest B7, B6 two digits to distinguish different instructions

B7	B6	Description
0	1	Data command setting
1	0	Display control command Settings
1	1	Address command setting

Data Command Setting

This command is used to set data write or read. Bits B1 and B0 cannot be set to 01 or 11.

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0	1	0	0			0	0	Data read/write mode setting	Display data input mode
0	1	0	0			1	0		Read key scan data
0	1	0	0		0			Address add mode setting	Automatic address increment
0	1	0	0		1				Fixed address
0	1	0	0	0				Test mode Settings (internal use)	Normal mode
0	1	0	0	1					Test mode

Address Command Setting

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display Address
1	1	0	0	0	0	0	0	00H
1	1	0	0	0	0	0	1	01H
1	1	0	0	0	0	1	0	02H
1	1	0	0	0	0	1	1	03H
1	1	0	0	0	1	0	0	04H
1	1	0	0	0	1	0	1	05H

This instruction is used to set the display register address; If the address is set to 0C4H or higher, the data is ignored until the valid address is set. During power-on, the default address is 00H.

Display Control Setting

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
1	0	0	0		0	0	0	Display duty cycle setting	Duty cycle is 1/16
1	0	0	0		0	0	1		Duty cycle is 2/16
1	0	0	0		0	1	0		Duty cycle is 4/16
1	0	0	0		0	1	1		Duty cycle is 10/16
1	0	0	0		1	0	0		Duty cycle is 11/16
1	0	0	0		1	0	1		Duty cycle is 12/16
1	0	0	0		1	1	0		Duty cycle is 13/16
1	0	0	0		1	1	1		Duty cycle is 14/16
1	0	0	0	0				Display ON/OFF setting	Display OFF
1	0	0	0	1					Display ON

Display and key scan cycle

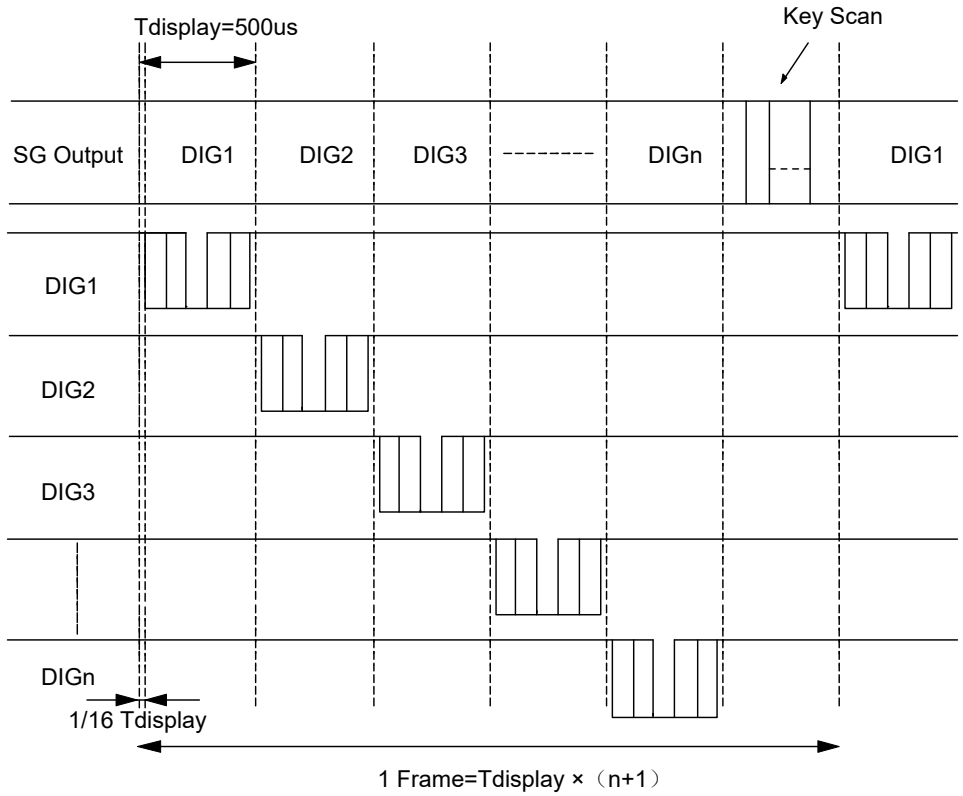


Figure6. Display and key scan cycle

Absolute Maximum Ratings

Symbol	Characteristic	Test Condition	Rating	Unit
V_{DD}	Supply Voltage		-0.5~+7.0	V
V_{H1}	Logic Input Voltage		-0.5~V_{DD}+0.5	V
I_{O1}	SEG Driver Output Current	V_{DD} = 5V	-50	mA
I_{O2}	GRID Driver Output Current	V_{DD} = 5V	200	mA
P_D	Power Dissipation		400	mW
T_J	Operating Junction Temperature		-40 ~ 150	˚C
T_{STG}	Storage Temperature		-65 ~ 150	˚C

Recommended Operating Conditions

Symbol	Characteristic	Recommend			Unit
		Min	Typ	Max	
V_{DD}	Supply Voltage	3.0	5.0	5.5	V
V_{IH}	High Level Input Voltage	0.7V_{DD}		V_{DD}	V
V_{IL}	Low Level Input Voltage	0		0.2V_{DD}	V
T_A	Operating Temperature	-40		+85	˚C

Electrical Characteristics

（Unless otherwise noted：T_A= -40℃~ 85℃，V_{DD} = 4.5V~ 5.5V，GND=0V)

Symbol	Characteristic	Test Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3.0	5.0	5.5	V
I_{OL1}	Low Level Output Current	SEG1~SEG8,V_O = 2V	-20	-25	-40	mA
I_{OL2}	Low Level Output Current	SEG1~SEG8,V_O = 3V	-20	-30	-50	mA
I_{OH1}	High Level Output Current	DIG1~DIG6,V_O = V_{DD}-2V	80	140		mA
I_{DOUT}	Low Level Output Current	V_O = 0.4V，DIO (output state)	4			mA
I_{TOLSG}	High Level Output Current Error	V_O = V_{DD}-3V, DIG1~DIG6			5	%
R_L	Pull-up Resistor	K1，K2		15		KΩ
V_{IH}	High Level Input Voltage	CLK，DIO	0.7V_{DD}		V_{DD}	V
V_{IL}	Low Level Input Voltage	CLK，DIO	0		0.2V_{DD}	V
V_H	Lagging Voltage	CLK，DIO		0.35		V
I_I	Input Current	V_I = V_{DD}			±1	uA
I_{DD}	Dynamic Current	No load, display off			1	mA

Switching parameter

(Unless otherwise noted：T_A= -40℃~ 85℃，V_{DD} = 4.5V~ 5.5V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
F_{osc}	Frequency Oscillation			450		KHz
T_{PLZ}	Transmission Delay Time	CLK→DIO CLK=15pF，R_L=10KΩ			300	ns
T_{PZL}					100	ns
T_{TZH1}	Rising Time	SEG1~8,CL=300pF, R_L=1K			2	us
T_{TZH2}		DIG1~6,C_L=300pF, R_L=1K			0.5	us
T_{THZ}	Falling Time	SEGn, DIGn，C_L=300pF, R_L=1K			120	us
F_{MAX}	Maximum Clock Frequency	Duty cycle is 50%			400	KHz
C_I	Input Capacitance				15	pF

Transformation Characteristic Time Sequence

(Unless otherwise noted：T_A = -40℃~ 85℃，V_{DD} = 4.5V~ 5.5V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
PW_{CLK}	Clock-pulse Width		400			ns
T_{setup}	Data Setup Time		100			ns
T_{hold}	Data Hold Time		100			ns
T_{wait}	Waiting Time	CLK↑→CLK↓	1			us

Time Sequence

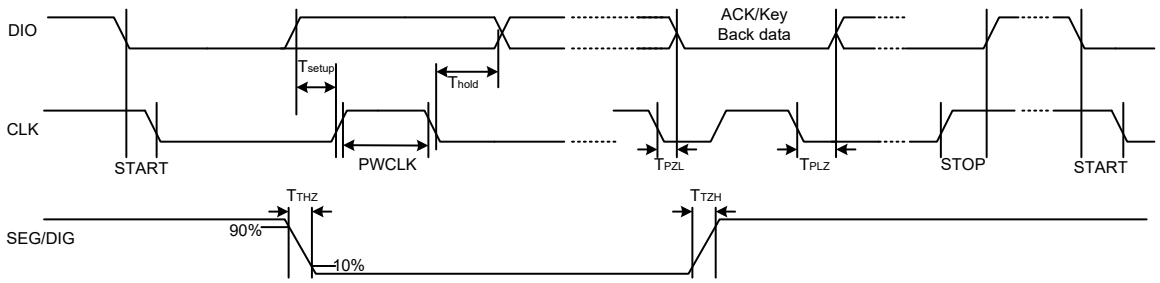


Figure7. Time sequence

Application circuit

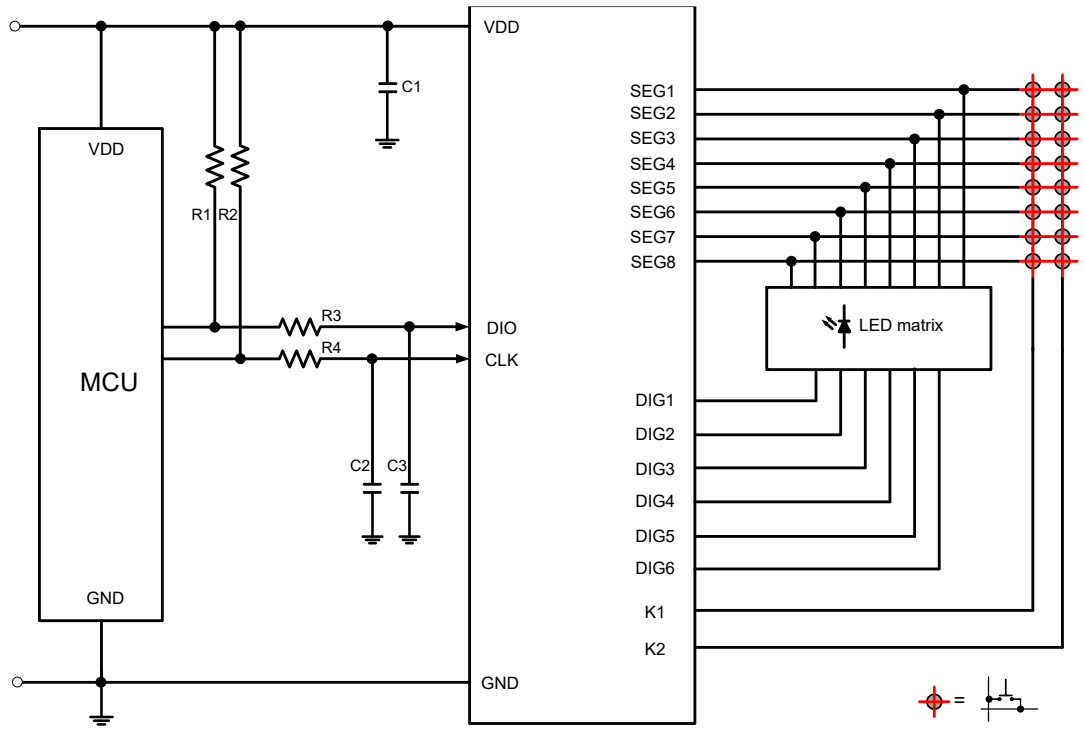


Figure8. Application circuit

Notes：

1. This application circuit is only for reference.

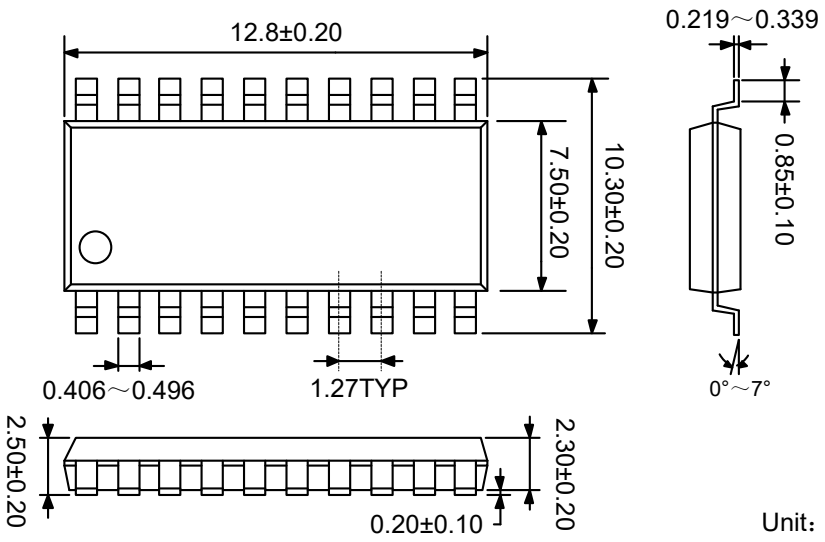
2. C1 = 1uF,and should be placed as close as possible to the VDD.

3. R1,R2 = 4.7kΩ, R3,R4 = 100Ω, C2,C3 = 100pF;

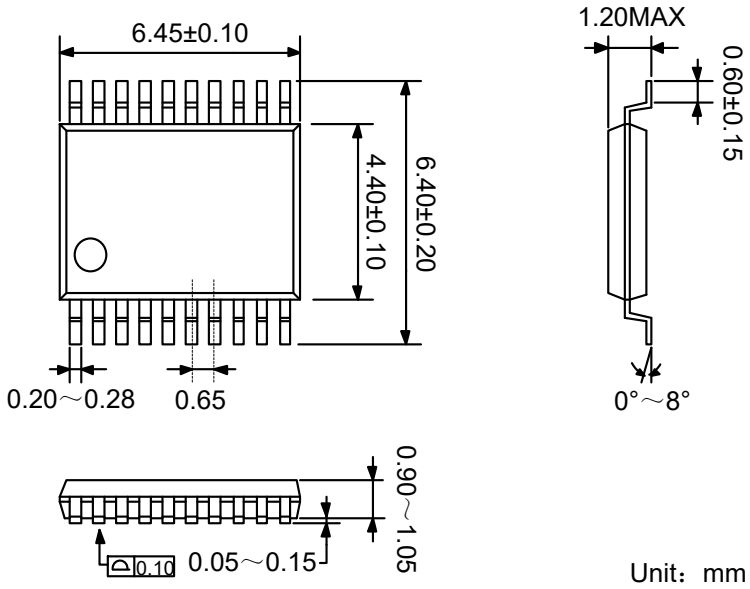
4. The series resistance of the communication port and the GND capacitor are placed as close as possible to ET1637, and the resistance value and capacitance value can be adjusted according to the actual anti-interference requirements and verification results.

Package

SOP20



TSSOP20



Revision History and Checking Table

No.	Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1	1.0	2020-01-19		Shilj	Shilj	Zhujl
2	1.1	2020-04-01	Specification document format	Shibo	Shilj	Shibo
3	1.2	2022-12-15	Update formatting	Shibo	Shilj	Zhuzq
4	1.3	2024-4-26	Update formatting	Wuyuchen	Shibo	Zhuzq