ET6218R - Matrix LED Controller and Driver

General Description

ET6218R is an LED Controller driver on a 1/7 to 1/8 duty factor, 7 segment output lines, 4 grid output lines, 1 segment/grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to ET6218R via a three-line serial interface.

ET6218R pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

Features

- CMOS Technology
- Low Power Consumption
- Multiple Display Modes (8Segs × 4Grids or 5Segs × 7Grids)
- Support 7 Key scanning (7×1 Matrix)
- 8-step Dimming Circuitry
- 3-Serial Interface for Clock, Data Input/Output, Strobe Pins
- Package: DIP18

Device Information

Part No.	Package	Size
ET6218R	DIP18	23mm × 6.5mm

Application

- Household appliances, Toy display
- Smart portable devices, Smart audio

Pin Assignments

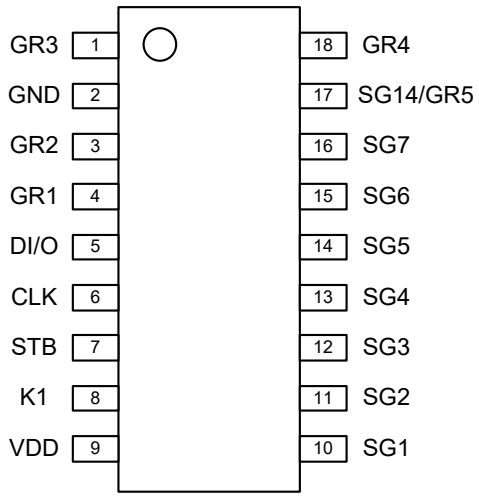


Figure 1. Pin Assignments (Top View)

Pin. Function

Pin No.	Pin Name	I/O	Description
5	DI/O (DIN&DOUT)	I/O	Data I/O Pin (Open-Drain) This pin outputs serial data at the falling edge of the shift clock and inputs serial data at the rising edge of the shift clock(starting from the lower bit)
6	CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge
7	STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command When this pin is “HIGH”, CLK is ignored
8	K1	I	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle (Interface Pull-Low Resistor)
2	GND	—	Ground Pin
10~16	SG1/KS1～ SG7/KS7	O	Segment Output Pins (connected to LED anode.) Also acts as the Key Source
17	SG14/GR5	O	Segment/Grid Output Pins
9	VDD	—	Power Supply
1,3,4,18	GR4～GR1	O	Grid Output Pins (connected to LED cathode)

Block Diagram

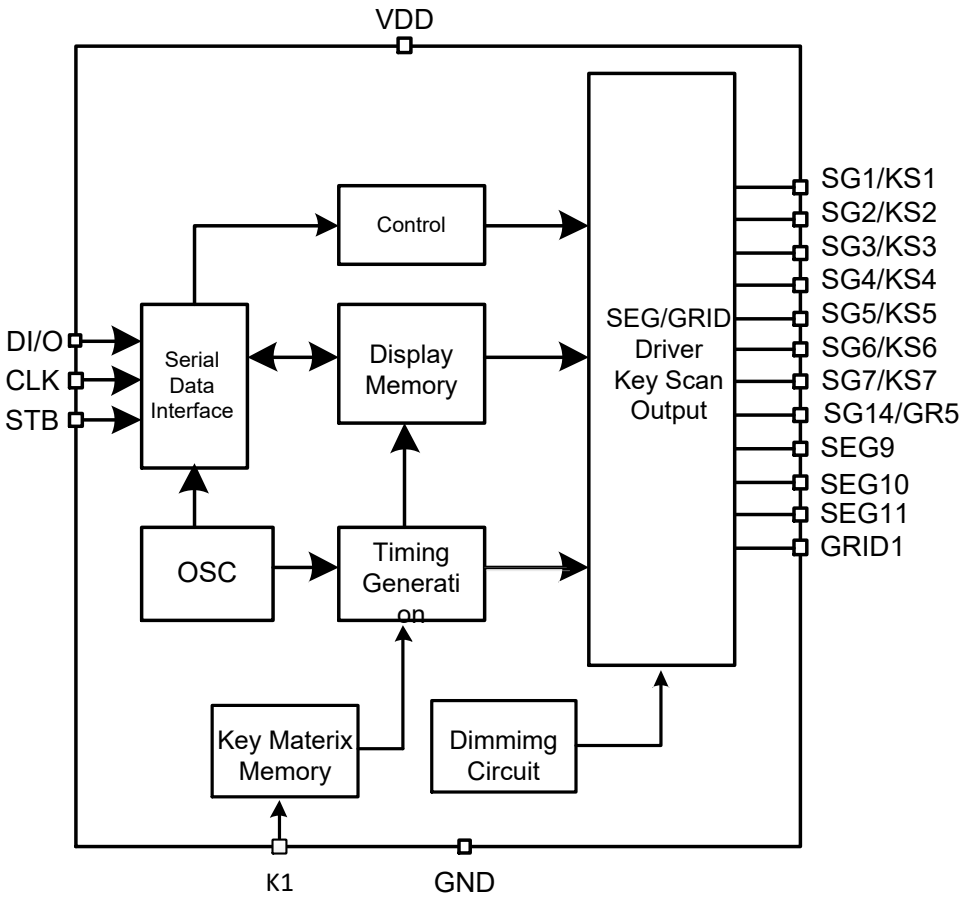


Figure 2. Block Diagram

Functions Description

Command

A command is the first byte (b0～b7) inputted to ET6218R via the DI/O Pin after STB Pin has changed from HIGH to LOW State. If for some reason the STB Pin is set to HIGH while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

Command 1：Display Mode Setting Commands

ET6218R provides 2 display mode settings as shown in the diagram below：As started earlier a command is the first one byte (b0～b7) transmitted to DI/O Pin when STB is LOW.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0	0	NC, Set to 0 please				0	0	Display segment and grid setting	8Segs×4Grids
0	0					0	1		7Segs×5 Grids

Command 2:Data Setting Commands

Data Setting Commands executes the Data Write or Data Read Modes for ET6218R. The data Setting Command, the bits 5 and 6(b4,b5) are ignored, bit 7(b6) is given the value of 1 while bit 8(b7) is given the value of 0. Please refer to the diagram below. When Power is turned ON, bit 4 to bit 1(b3～b0) are given the value of 0.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0	1	NC, Set to 0 please		0				Mode setting	Normal mode
0	1			1					Test mode
0	1				0			Address mode	Automatic address increase
0	1				1				Fixed address
0	1					0	0	Data write/read	Display data input mode
0	1					1	0		Read Key Data

Key Scan Matrix

The key scan matrix is composed of 7×1 array：

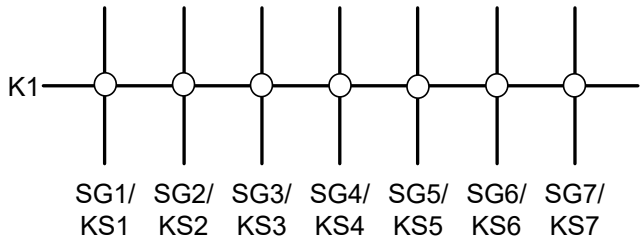


Figure 3. Key scan matrix

Key Scan Data Storage RAM

The input data is stored as follows: the READ command is used to READ from the highest bit.

	B0	B1	B2	B3	B4	B5	B6	B7
BYTE1	SG1/KS1	×		SG2/KS2	×			
BYTE2	SG3/KS3	×		SG4/KS4	×			
BYTE3	SG5/KS5	×		SG6/KS6	×			
BYTE4	SG7/KS7	×		SG8/KS8	×			
BYTE5	SG9/KS9	×		SG10/KS10	×			
	K1			K1				

READING SEQUENCE

Note：B1,B2, B4～B7 undefined.

Command3：Display Address Setting

The address setting command is used to set the display memory address.If the address ranges from 00H to 09H, the address is valid.If the address is 0AH or higher, the data is invalid unless the correct address is set again.When the power supply is powered on, the address is 00H.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Description
1	1	NC, fill in 0		0	0	0	0	Display address 00H
1	1			0	0	0	1	Display address 01H
1	1			0	0	1	0	Display address 02H
1	1			0	0	1	1	Display address 03H
1	1			0	1	0	0	Display address 04H
1	1			0	1	0	1	Display address 05H
1	1			0	1	1	0	Display address 06H
1	1			0	1	1	1	Display address 07H
1	1			1	0	0	0	Display address 08H
1	1			1	0	0	1	Display address 09H

Address assignment：

SG1……SG4	SG5……SG7	SG14	Matrix Address
$00H_L$(B0~B3)	$00H_U$(B4~B6)	$01H_U$(B5)	DIG1
$02H_L$	$02H_U$	$03H_U$	DIG2
$04H_L$	$04H_U$	$05H_U$	DIG3
$06H_L$	$06H_U$	$07H_U$	DIG4
$08H_L$	$08H_U$	$09H_U$	DIG5

Definition of H_U and H_L in RAM address：

B0	B1	B2	B3	B4	B5	B6	B7
××H_L				××H_U			
Low 4bits				High 4bits			

Command4：Display Control Setting

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
1	0	NC, fill in 0			0	0	0	Display duty cycle setting	Duty cycle is 1/16
1	0				0	0	1		Duty cycle is 2/16
1	0				0	1	0		Duty cycle is 4/16
1	0				0	1	1		Duty cycle is 10/16
1	0				1	0	0		Duty cycle is 11/16
1	0				1	0	1		Duty cycle is 12/16
1	0				1	1	0		Duty cycle is 13/16
1	0				1	1	1		Duty cycle is 14/16
1	0			0				Display ON / OFF setting	Display OFF
1	0			1					Display ON

Scan and Display Timing

Key scan and display sequence diagram as shown below.A cycle of key scanning consists of 2 frames.The data of the 7 x 1 matrix is stored in RAM.

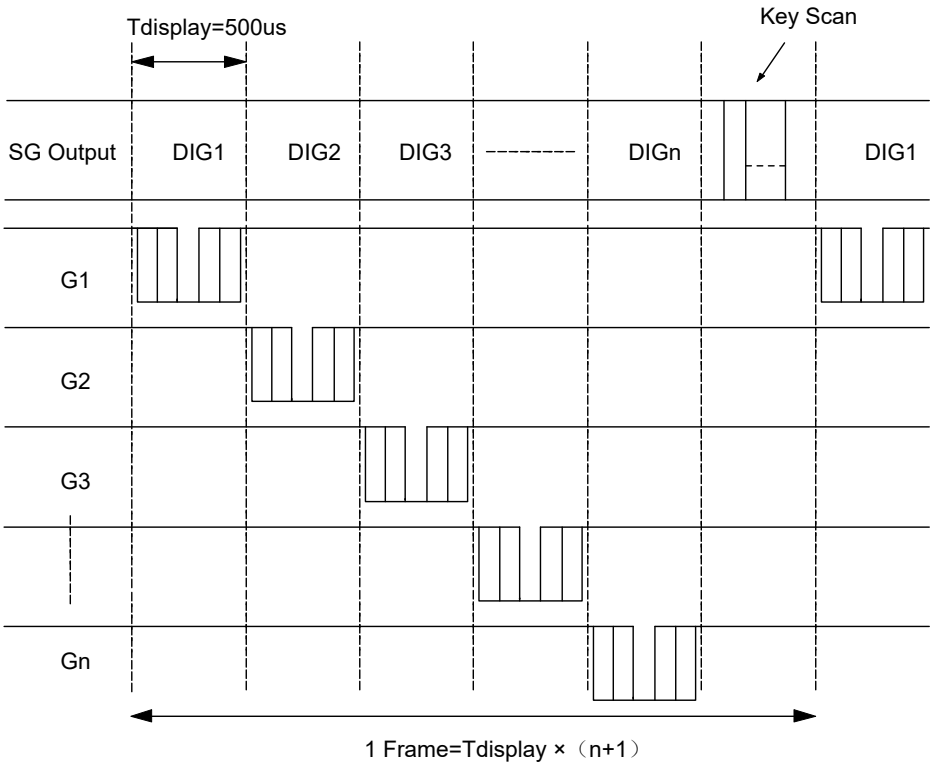


Figure 4.

Serial Communication Format

The following figure shows the serial communication format of ET6218R. It is recommended to connect a pull-up resistor (1K ~ 10K) to the DIO port.

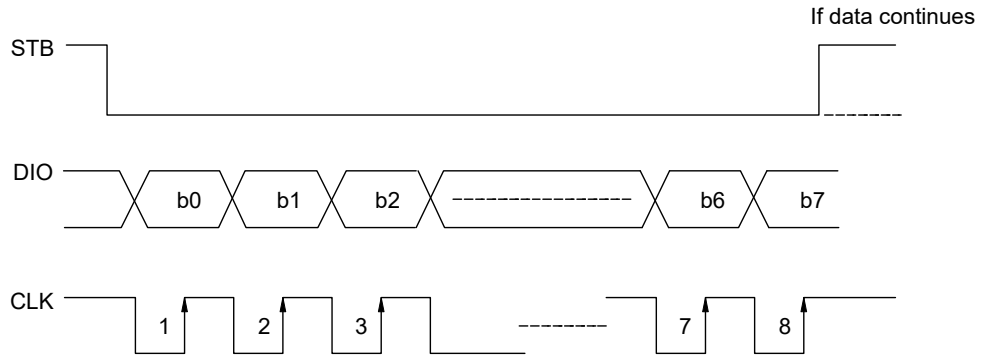
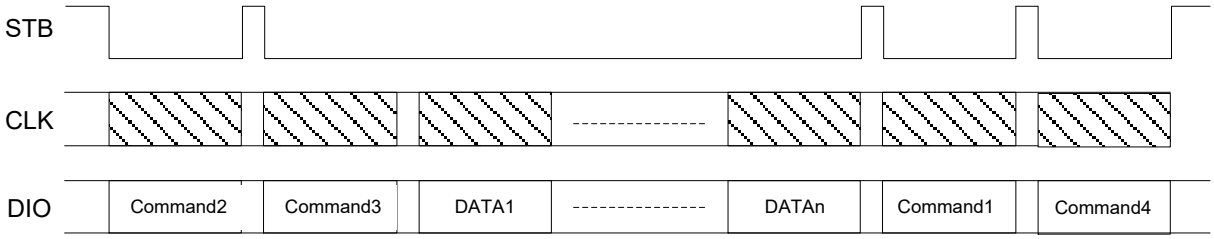


Figure 5.

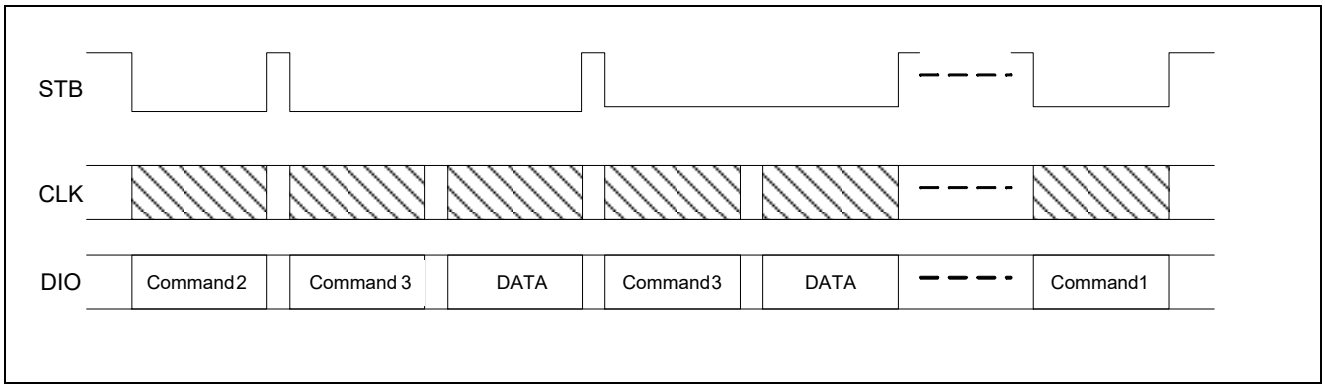
Communication application time series

Continuous display data writing (Automatic address increase)



- Command1：Display mode setting
- Command2：Data command setting
- Command3：Address command setting
- DATA1～n： Display data(MAX 14bytes)
- Command4：Display control command

Single display data writing (fixed address mode)



- Command1：Display mode setting
- Command2：Data command setting
- Command3：Address command setting
- DATA：Display data

Data transmission（Data read）

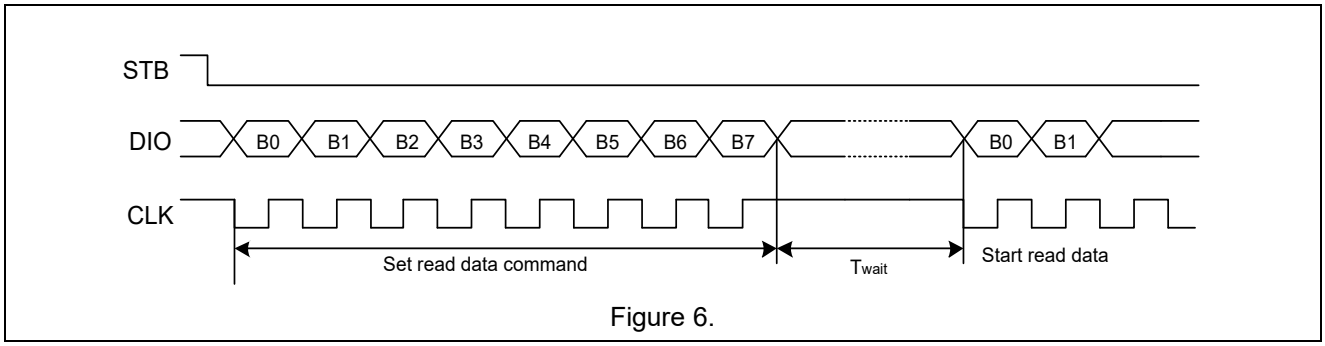


Figure 6.

Note: T_{wait}（waiting time）≥1μs.

It should be noted that when reading data, the rising edge is the eighth clock of the instruction to the falling edge of the first clock of the subsequent data reading must be longer than or equal to 1us waiting time(T_{wait}).

Conversion Characteristic Waveform

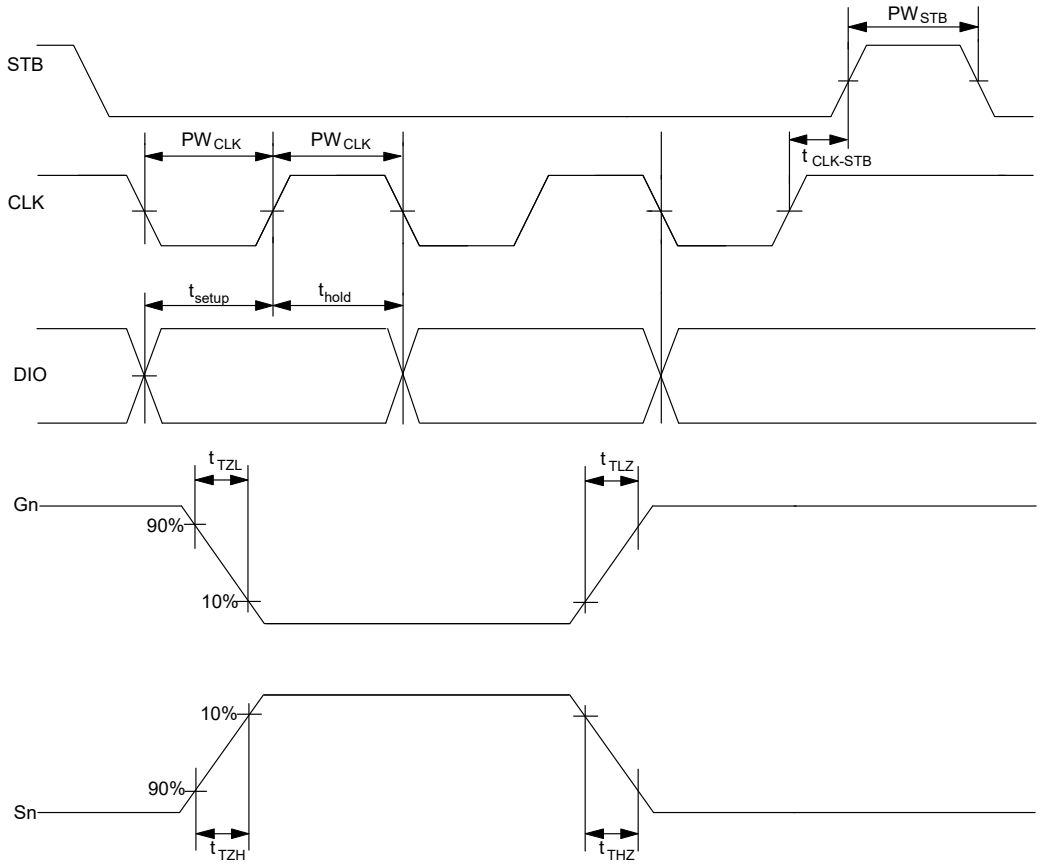


Figure 7.

Transformation Characteristic

Symbol	Descripiton	Range	Units
PW_{CLK}	CLK pulse width	≥400	ns
PW_{STB}	STB pulse width	≥1	us
t_{setup}	Data setup time	≥100	ns
t_{hold}	Date hold time	≥100	ns
$t_{CLK-STB}$	CLK-STB time	≥1	us
t_{THZ}	Falling time	≤10	us
t_{TZH}	Rising time	≤1	us
t_{TZL}		<1	us
t_{TLZ}		<10	us

Note: The test conditions :

t_{THZ} (pull-down resistance = 10kΩ, loading capacitance =300pF)

t_{TLZ} (pull-up resistance = 10kΩ, loading capacitance =300pF)

Software flow chart

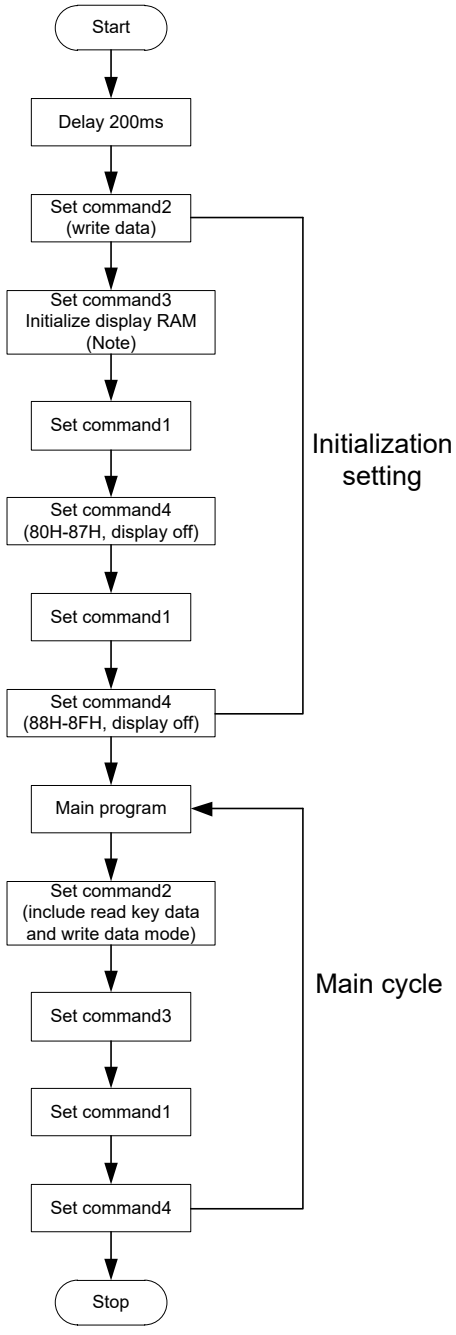


Figure 8.

Notes：

- Command1：Display mode setting
- Command2：Data command setting
- Command3：Address command setting
- Command4：Display control command

When the IC is powered on for the first time, the contents of the display RAM are not defined, so be sure to clear the contents of the display RAM in the initialization setting.

Absolute Maximum Ratings

(Unless otherwise noted ,T_A=25°C)

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.5～+7	V
Logic Input Voltage	V_I	-0.5～V_{DD}+0.5	V
Driver Output Current	I_{OLGR}	+250	mA
	I_{OHSG}	-50	mA
Max Output Driver current	I_{TOTAL}	400	mA

Recommended Operating Conditions

(Unless otherwise noted ,T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	5.0	5.5	V
Dynamic current	I_{DD_DYN}*	—	—	1	mA
High Level Input Voltage	V_{IH}	0.8V_{DD}	—	V_{DD}	V
Low Level Input Voltage	V_{IL}	0	—	0.3V_{DD}	V

Note*: Test condition Set display mode command = 80H (display off & no load).

Electrical Characteristics

(Unless otherwise noted, V_{DD}=5V ,T_A=25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Output Current	I_{OHSG1}	V_O=V_{DD}-2V SG1～SG7, SG14	-20	-25	-40	mA
	I_{OHSG2}	V_O=V_{DD}-3V SG1～SG7, SG14	-25	-30	-50	mA
Low Level Output Current	I_{OLGR}	V_O=0.3V, GR1～GR5,	100	140		mA
Low Level Output Current (DIO PIN)	I_{OLDOUT}	V_O=0.4V	4			mA
Percentage of high level output current at segment	I_{TOLSG}	V_O=V_{DD}-3V SG1～SG7, SG14			+5	%
High Level Input Voltage	V_{IH}		0.8V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}		0		0.3V_{DD}	V
Oscillation Frequency	F_{OSC}		350	500	650	kHz
K1 Pull-down Resistance	R_{KN}	K1	40	—	100	kΩ

Electrical Characteristics

(Unless otherwise noted, V_{DD}=3.3V ,T_A=25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Output Current	I_{OHSG1}	V_O = V_{DD} -2V，SG1～SG10, SG12～SG14	-15	-20	-35	mA
Low Level Output Current	I_{OLGR}	V_O =0.3V，GR1～GR7,	100	140	—	mA
Low Level Output Current (DIO PIN)	I_{OLDOUT}	V_O=0.4V	4	—	—	mA
High Level Input Voltage	V_{IH}	—	0.8V_{DD}	—	3.3	V
Low Level Input Voltage	V_{IL}	—	0	—	0.3V_{DD}	V
Oscillation Frequency	F_{OSC}		300	420	580	kHz
K1 Pull-down Resistance	R_{KN}	K1	40	—	100	kΩ

Application circuit

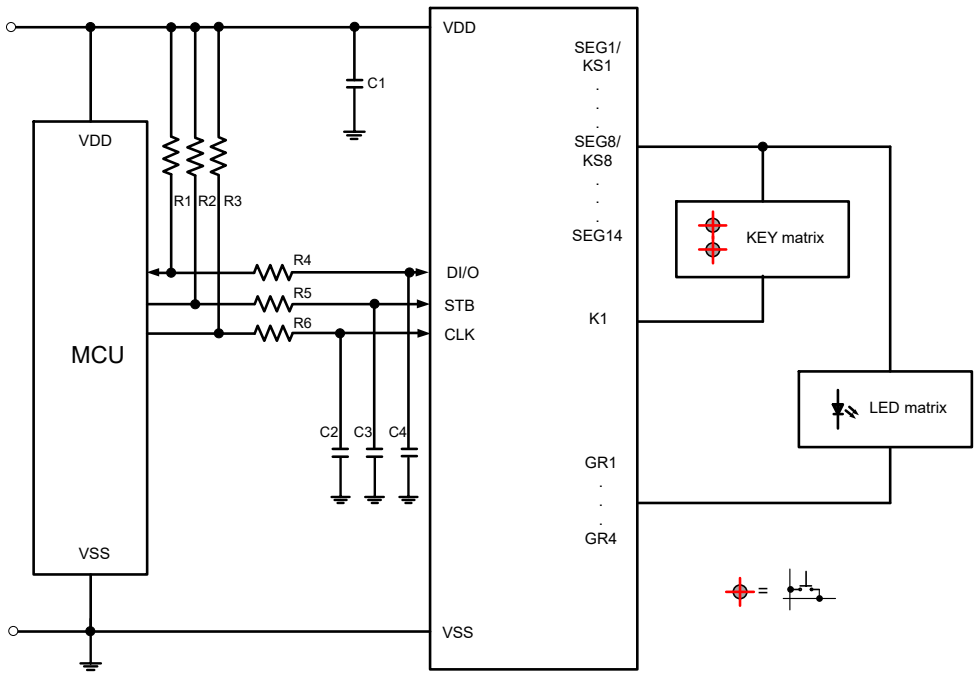


Figure 9.

Notes：

1. This application circuit is only for reference.

2. C1=1uF and should be placed as close as possible to the VDD.

3. R1~R3 = 4.7kΩ, R4~R6 = 100Ω, C2~C4 = 100pF.

4. The series resistance of the communication port and the capacitor for GND should be placed as close as possible to ET6218R, and the resistance value and capacitance value should be adjusted according to the actual anti-interference requirements and verification results.

Common cathode LED connection

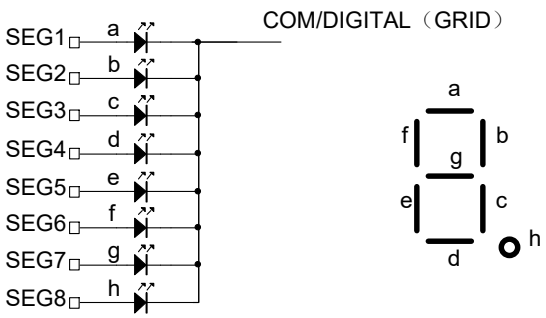
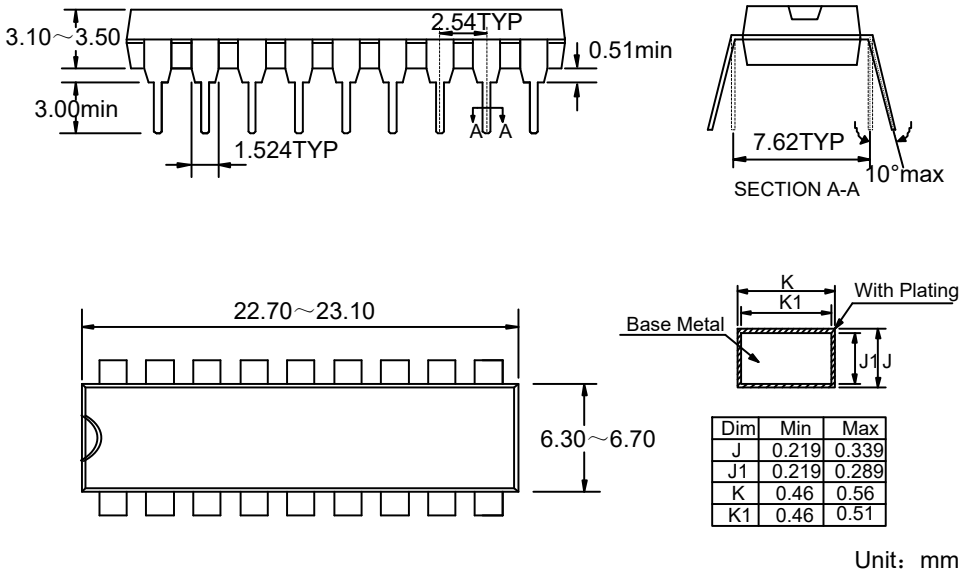


Figure 10.

Note： This application circuit is only for reference.

Package

DIP18



Dim	Min	Max
J	0.219	0.339
J1	0.219	0.289
K	0.46	0.56
K1	0.46	0.51

Unit：mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2018-1-23	Original Version	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.1	2022-11-22	Update form	Lv Yue Jin	Shi Bo	Shi Bo