12CH Constant Current LED Driver with I²C Control

General Description

The ET6312B are four constant current RGB LED drivers with I²C interface. The devices are ideally powered from 3.3V or 5V supplies. The independent programmable constant current sinks operate without external components.

By the nine internal registers programming, the each three LED channels can work in variety modes, a total of 192 current levels are available for each channel from 0.125mA to 24mA with a 0.125mA step or 0.25mA to 48mA with a 0.25mA step.

The device has design three kinds of interconnected threads, each channel can carry on any threads mode with an on-chip timing control unit, LED blink rate, fade-in(256 steps) and fade-out(256 steps) are user-adjustable resulting in unique color lighting patterns. The ET6312B have ADDR and SYN pin, it can realize four chips cascade with one group of I²C bus and one synchronous clock. In shutdown mode, the quiescent current is reduced to less than 1μA.

The driver is available in a QFN20 package. The package is Pb-free and RoHS compliant.

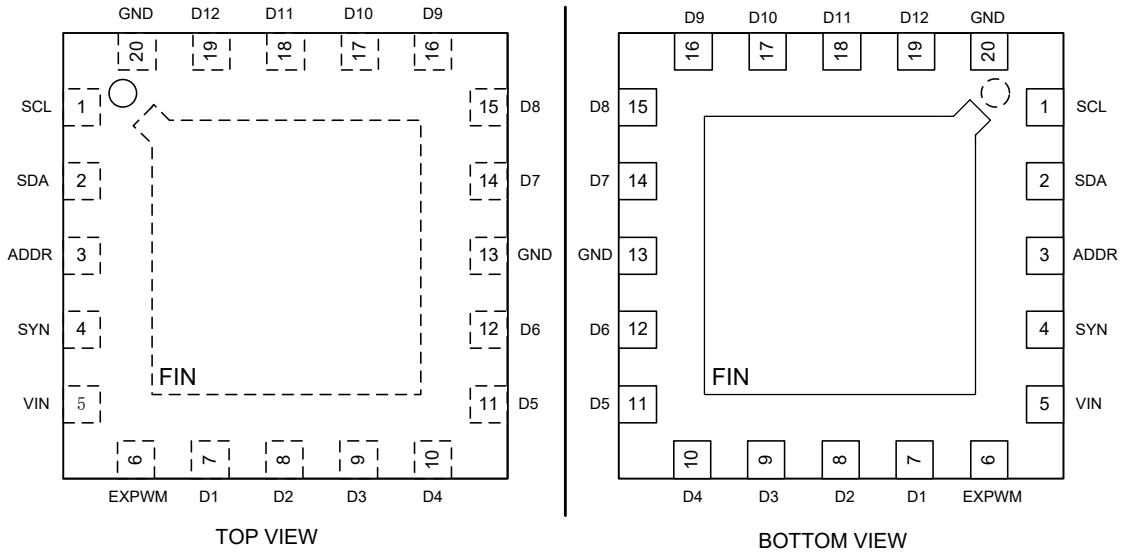
Features

- Ultra low dropout regulated current sinks, 75mV typical at 10mA per channel
- Each nine programmable LED setting registers are shared by each three LED
- I²C control, one ADDR pin realize four chip address selection
- SYN pin can supply chips cascade synchronous clock
- EXPWM pin for external PWM input, each LED can run external PWM when LED is working in “ON” state
- Individual channel control
  - On/Off Interval Time Control
  - Dimming Up/Down Time produced by 256 steps internal PWM
  - Current Level Setting
  - RGB LED Color Control
  - RGB Delay Time and FLASH Period Control
- 192 current levels: 24mA max@0.125mA step or 48mA max@0.25mA step
- ±5% current matching for max current, low supply current of 450μA typ
- No noise, non-pulsating LED current, Fast, smooth start-up
- VIN Range Voltage from 2.7V to 5.5V
- 0.1μA Low Shutdown Current
- Pb-free Package: QFN20 (3mm x 3mm x 0.75mm)
- Inside Temperature Protection

Application

- RGB indicator LEDs
- Flashing LEDs
- Handheld Devices
- Digital Cameras

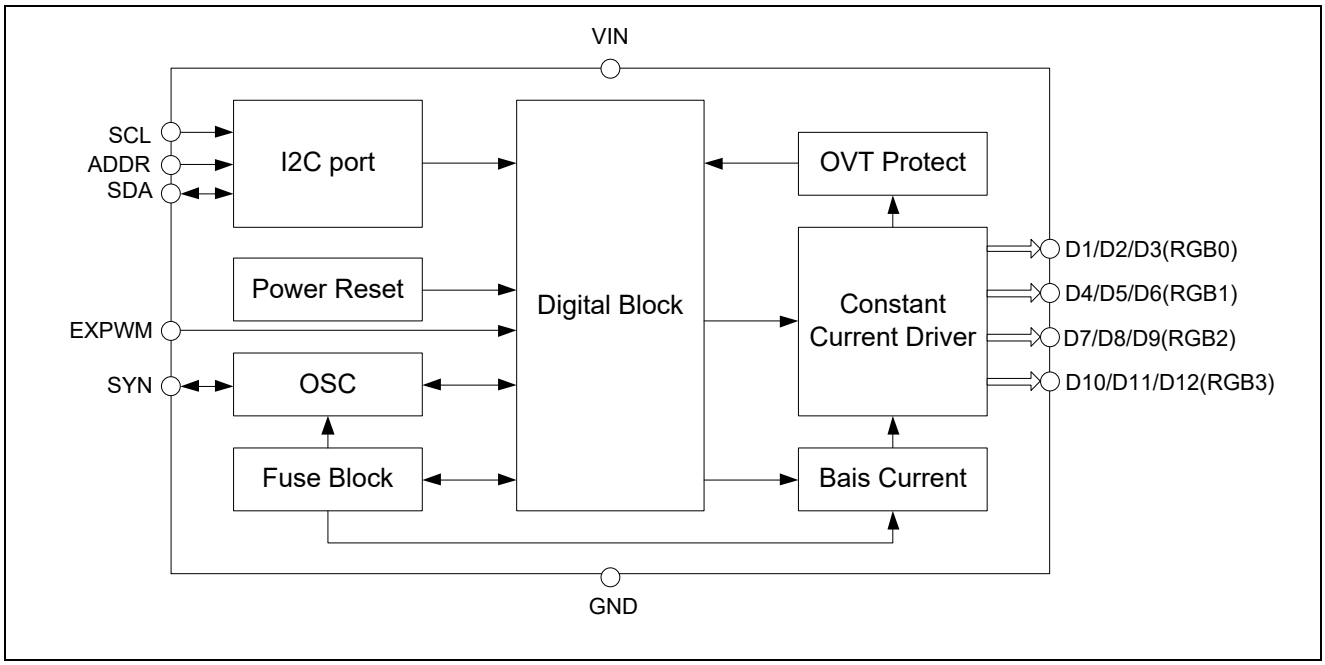
Pin Configuration



Pin Function

Name	Pin No	Type	Description
SCL	1	I	Clock of the I²C interface.
SDA	2	I/O	Data of the I²C interface.
ADDR	3	I	Chip address select, it can connect VDD/GND/SCL/SDA pins to select four chip address.
SYN	4	I/O	Synchronous clock input or output Pin.
VIN	5	-	Input power for the IC.
EXPWM	6	I	External PWM input pin with pull-down resistor.
D1~D6	7~12	O	Regulated output current sink D1~D6. Current level and ON/OFF selections are controlled by I²C interface.
GND	13/20	-	Ground pin.
FIN	-	-	Ground pin.
D7~D12	14~19	O	Regulated output current sink D7~D12. Current level and ON/OFF selections are controlled by I²C interface.

Block Diagram



Functional Description

The ET6312B is a 12-channel output current sink device, offering constant current regulation with high efficiency and ultralow internal voltage drop. High integration and small size makes it ideal for driving RGB LEDs from a one-cell lithium-ion/polymer battery. With a supply voltage range of 2.7V to 5.5V, the ET6312B is equally suitable for 3 or 4 cell NiCd/NiMH/Alkaline devices or systems with 3.3V or 5V supplies.

The ET6312B can be programmed by I^2C compatible interface. Each current sink can be configured independently to one of the 192-step current levels or turned off. Each RGB LED is composed by three LEDs, and its PWM waveform related registers are also shared by three LEDs.

LED current programming

Each channel's brightness is controlled by the LEDx Iout registers LED1_CURT(1AH) to LED12_CURT(25H). Each channel has a dedicated 8-bit register for setting the current value. The LED channel current is constant, non-pulsing, except when it is being ramped-up and down.

The ramp up and down are automatically generated using a PWM scheme where the duty cycle is continuously changing (either increasing or decreasing) to provide a smooth LED current transition between the ON and OFF states. Each RGB's ramp times, for rise and fall, are separately programmable through an internal Ramp register RAMP_RATE_RGBn(n=0~3) with 4 bits for rise and 4 bits for fall. The ramping can be configured to linear or quasi-logarithmic/s-curve by setting register FLASH_PERIOD_RGBn(n=0~3) bit 7.

The flashing LEDs can be performed by set register CHIPCTR bit 7(auto_brecon) and by programming the time period (Tepriod) and the delay time (Tdelay) between two consecutive flashes in the Flash Period register FLASH_PERIOD_RGBn(n=0~3) and the delay time register DELAY_TIEM_RGBn(n=0~3). Two Flash On Timer 1/2 registers, FLASH_TON1_RGBn(n=0~3) and FLASH_TON2_RGBn(n=0~3), allow to set the LED on time as a percentage of the Flash period. The on time (Ton), shown in Figure 1, includes the ramp-up

Trise and the full on time. Two timer registers for each RGB LED are available to support two or three LEDs to flash independently. Each channel can be configured to thread1 or thread2 or thread3 mode with the Channel Control register LEDXMD_RGBn(n=0~3).

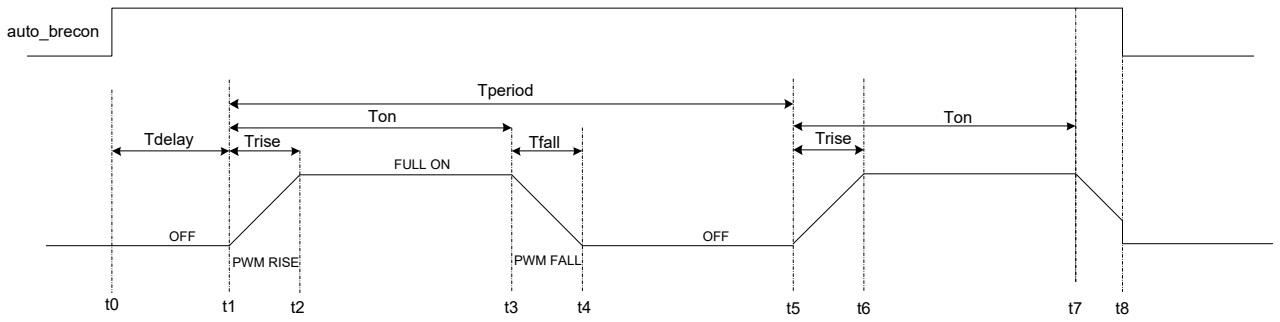


Figure 1. Channel Timing Diagram

Timer Mode Control

The timing diagrams for the four time modes are illustrated below.

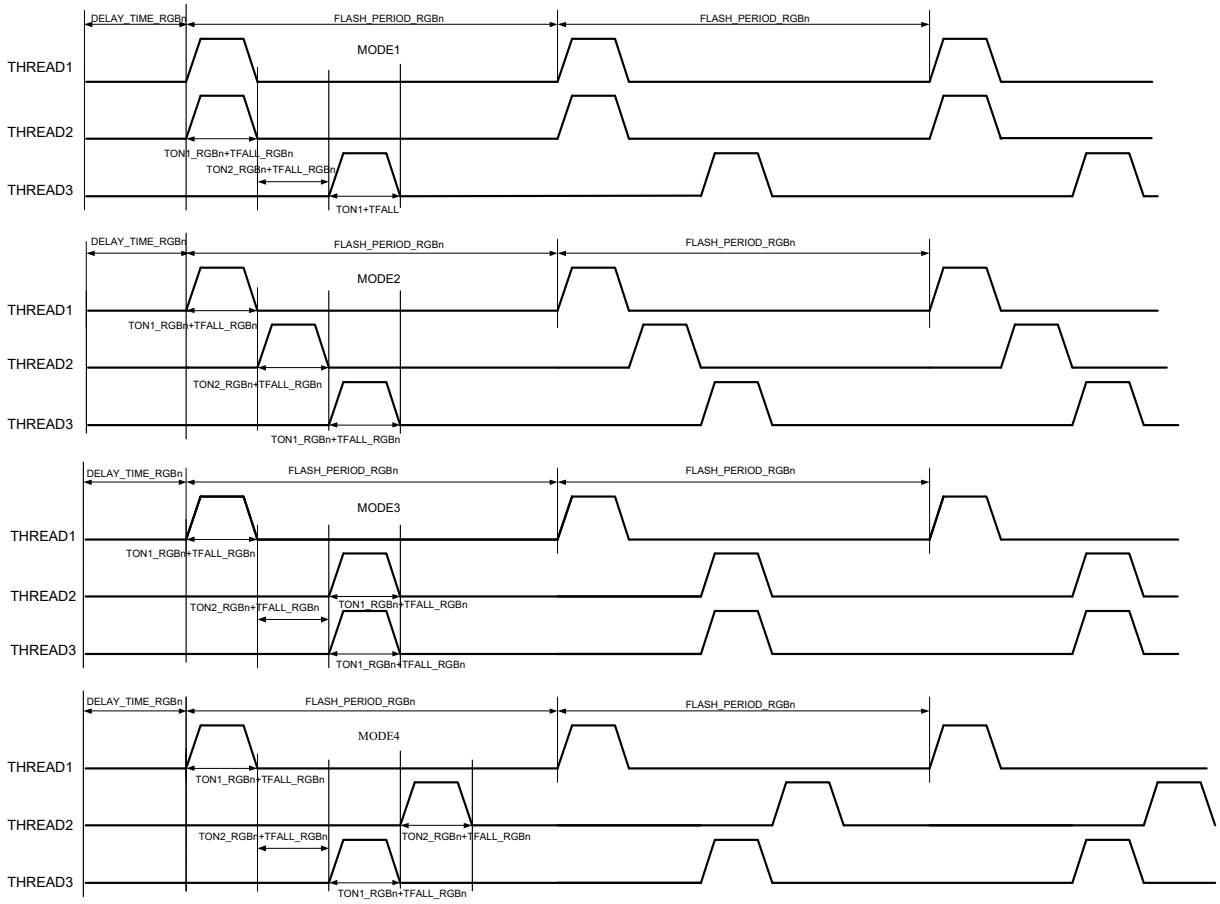


Figure 2. Four Mode Timing Diagram

Each channel can be assigned to one of the 3 time threads, or always OFF or always ON. The Timer Mode Control defines the timing as figure2.

The Duty Cycle of each flash waveform is set by the timer and can be set with 8-bit resolution (256 steps) between 0 and 100%. The period of the flash repetition rate can also be set with a 7-bit resolution up to 16 seconds. The Flash repetition period is the same for each three(RGBn,n=0~3) outputs. If the programmed total time of the Timers exceed the Flash repetition rate then the ThreadN(N=1~3) mode will be terminated and the Timers reset to start(t1,shown as figure 1) position. This may cause the ThreadN signal to be instantly reduced to zero. If TON<TRISE, the waveform fade-in will not reach maximum(FFH).

Rise/Fall Times

The Ramp-Up and Ramp-Down can be linear or S-shaped profile. The S-shape is the default. The ramp-up transitions from 0% to 100% of the Iset value (ON state) and ramp-down to 0% (OFF state).

LED Current Control

The brightness setting of each channel is internally controlled by 48 current units of 0.5mA. Output current resolution is increased to an effective 0.125mA steps by interpolation based time division multiplexing (similar to PWM) by a digital interpolator and works on the 2 LSB units of the current setting.

Register Map

Name	Addr	Description							Default
CHIPCTR	00H	auto_brecon	clkoen	clkdir	softdn_en	pden	imax_sel	tmd _sel[1:0]	x00
FLASH_PERIOD_RGB0	01H	rpline_rgb0	flash period_rgb0[6:0]						x00
FLASH_TON1_RGB0	02H	flash_ton1_rgb0[7:0]							x01
FLASH_TON2_RGB0	03H	flash_ton2_rgb0[7:0]							x01
RAMP_RATE_RGB0	04H	tfall_rgb0[3:0]				trise_rgb0[3:0]			x00
DELAY_TIME_RGB0	05H	delay_time_rgb0[7:0]							x00
FLASH_PERIOD_RGB1	06H	rpline_rgb1	flash period_rgb1[6:0]						x00
FLASH_TON1_RGB1	07H	flash_ton1_rgb1[7:0]							x01
FLASH_TON2_RGB1	08H	flash_ton2_rgb1[7:0]							x01
RAMP_RATE_RGB1	09H	tfall_rgb1[3:0]				trise_rgb1[3:0]			x00
DELAY_TIME_RGB1	0AH	delay_time_rgb1[7:0]							x00
FLASH_PERIOD_RGB2	0BH	rpline_rgb2	flash period_rgb2[6:0]						x00
FLASH_TON1_RGB2	0CH	flash_ton1_rgb2[7:0]							x01
FLASH_TON2_RGB2	0DH	flash_ton2_rgb2[7:0]							x01
RAMP_RATE_RGB2	0EH	tfall_rgb2[3:0]				trise_rgb2[3:0]			x00
DELAY_TIME_RGB2	0FH	delay_time_rgb2[7:0]							x00
FLASH_PERIOD_RGB3	10H	rpline_rgb3	flash period_rgb3[6:0]						x00
FLASH_TON1_RGB3	11H	flash_ton1_rgb3[7:0]							x01
FLASH_TON2_RGB3	12H	flash_ton2_rgb3[7:0]							x01
RAMP_RATE_RGB3	13H	tfall_rgb3[3:0]				trise_rgb3[3:0]			x00
DELAY_TIME_RGB3	14H	delay_time_rgb3[7:0]							x00

Register Map(Continued)

Name	Addr	Description				Default
RF_SCALE	15H	rfscale_rgb3[1:0]	rfscale_rgb2[1:0]	rfscale_rgb1[1:0]	rf_scale_rgb0[1:0]	x00
LEDXMD_RGB0	16H	led3_wkmd[2:0]	led2_wkmd[2:0]		led1_wkmd[1:0]	x00
LEDXMD_RGB1	17H	led6_wkmd[2:0]	led5_wkmd[2:0]		led4_wkmd[1:0]	x00
LEDXMD_RGB2	18H	led9_wkmd[2:0]	led8_wkmd[2:0]		led7_wkmd[1:0]	x00
LEDXMD_RGB3	19H	led12_wkmd[2:0]	led11_wkmd[2:0]		led10_wkmd[1:0]	x00
LED1_CURT	1AH	led1_curt[7:0]				x4F
LED2_CURT	1BH	led2_curt[7:0]				x4F
LED3_CURT	1CH	led3_curt[7:0]				x4F
LED4_CURT	1DH	led4_curt[7:0]				x4F
LED5_CURT	1EH	led5_curt[7:0]				x4F
LED6_CURT	1FH	led6_curt[7:0]				x4F
LED7_CURT	20H	led7_curt[7:0]				x4F
LED8_CURT	21H	led8_curt[7:0]				x4F
LED9_CURT	22H	led9_curt[7:0]				x4F
LED10_CURT	23H	led10_curt[7:0]				x4F
LED11_CURT	24H	led11_curt[7:0]				x4F
LED12_CURT	25H	led12_curt[7:0]				x4F

Register Map(continued)

Name	Addr	Description								Default
EXPWM_EN	26H	x	x	x	x	epen_rgb3	epen_rgb2	epen_rgb1	epen_rgb0	x00

Note: LEDx corresponding the port of device Dx.

Register CHIPCTR [7] Automatic Flash function enable signal

auto_brecon	Function
0	Stop all LED Flash function
1	Start all LED Flash function

Register CHIPCTR[6:5] CLK Input or Output select

clkoen	clkdir	Function
x	1	Inner clock from SYN Pin(SYN is a input pin)
0	0	Inner clock from inner OSC(SYN is a output pin and output “0”)
1	0	Inner clock from inner OSC(SYN is a output pin and output “inner oscillator clock”)

Register CHIPCTR [4] software Shutdown Enable

softdn_en	Function
0	Enable software shutdown, chip in standby mode
1	Disable software shutdown, chip go to work

Register CHIPCTR [3] SCL port shutdown enable

pden	Function
0	Disable SCL=0 shutdown function
1	Enable SCL=0 shutdown function

Note: if pden=1 and scl=0(low level time>350us), chip will go to shutdown mode.

Register CHIPCTR [2] Max output constant current Select

imax_sel	Function
0	24mA
1	48mA

Register CHIPCTR[1:0] Timer Mode Control

tmd _sel [1:0]	Function
00	mode1
01	mode2
10	mode3
11	mode4

Register FLASH_PERIOD_RGBn Flash Period and FLASH_TON1/2_RGBn Flash On Time

The each three registers FLASH_PERIOD_RGBn, FLASH_TON1_RGBn and FLASH_TON2_RGBn allow configuration of the blinking time for the two timers TON1 and TON2. FLASH_TON1_RGBn and FLASH_TON2_RGBn define the LED ON time as a percentage of the period defined in FLASH_PERIOD_RGBn. The ON time (Ton) includes the ramp rise time and ON hold time as shown in Figure 1. For example, for FLASH_PERIOD_RGBn=4 and FLASH_TON1_RGBn=5, ON timer 1 is equal to 2% of 0.64s = 12.8ms

FLASH_Period_RGBn[6:0] Flash Period		
Dec	**Binary**	**Period[s]**
0	0000000	0.128
1	0000001	0.256
2	0000010	0.384
3	0000011	0.512
4	0000100	0.640
5	0000101	0.768
6	0000110	0.896
7	0000111	1.024
8	0001000	1.152
9	0001001	1.28
10	0001010	1.408
11	0001011	1.536
12	0001100	1.664

(Continued)

FLASH_Period_RGBn[6:0] Flash Period		
Dec	**Binary**	**Period[s]**
13	0001101	1.792
……	……	……
112	1110000	14.46
113	1110001	14.59
114	1110010	14.72
115	1110011	14.85
116	1110100	14.98
117	1110101	15.10
118	1110110	15.23
119	1110111	15.36
120	1111000	15.49
121	1111001	15.62
122	1111010	15.74
123	1111011	15.87
124	1111100	16.0
125	1111101	16.13
126	1111110	16.26
127	1111111	16.38

Register FLASH_PERIOD_RGBn[7] Ramp Linear

The default setting, bit FLASH_PERIOD_RGBn[7](refer to rpline_rgbn)=0, provides with a logarithmic-like S ramp up and down curve. By setting this bit to 1, the ramp becomes a simple linear up and down waveform.

FLASH_TON1/2_RGBn[7:0] Flash ON Timer 1/2		
Dec	**Binary**	**Percentage of Period[%]**
0	00000000	0.0%
1	00000001	0.4%
2	00000010	0.8%
3	00000011	1.2%
4	00000100	1.6%
5	00000101	2.0%
6	00000110	2.3%
7	00000111	2.7%
8	00001000	3.1%
9	00001001	3.5%
10	00001010	3.9%
11	00001011	4.3%
12	00001100	4.7%

(Continued)

FLASH_TON1/2_RGBn[7:0] Flash ON Timer 1/2		
Dec	**Binary**	**Percentage of Period[%]**
13	00001101	5.1%
……	……	……
239	11101111	93.4%
240	11110000	93.8%
241	11110001	94.1%
242	11110010	94.5%
243	11110011	94.9%
244	11110100	95.3%
245	11110101	95.7%
246	11110110	96.1%
247	11110111	96.5%
248	11111000	96.9%
249	11111001	97.3%
250	11111010	97.7%
251	11111011	98.0%
252	11111100	98.4%
253	11111101	98.8%
254	11111110	99.2%
255	11111111	99.6%

Register RF_SCALE_RGBn Rise/Fall Time Scaling

These two bits allow to scale the rise and fall times defined in RF_SCALE_RGBn ramp rate register.

For example, RF_SCALE_RGBn [7:6] = 01b (2x slower scaling) and RAMP_RATE_RGB3=01H, then the rise time of RGB3=128ms x 2 = 256ms.

rfscale_rgbn[1:0]	Function
00	1x Normal
01	2x Slower
10	4x Slower
11	8x Faster

Register RAMP_RATE_RGBn Ramp Times

The register RAMP_RATE_RGBn sets the rise and fall time durations for the LED current ramp transitioning between 0mA and the nominal current. The rise and fall ramp times are defined by 4 bits RAMP_RATE_RGBn[3:0] and RAMP_RATE_RGBn[7:4] respectively.

For example, RAMP_RATE_RGBn=04H and RF_SACLE[7:0] = 00H (1x ramp scaling), then the rise time is equal to 512ms.

trise_rgbn[3:0]/ tfall_rgbn[3:0]		Ramp Time [ms]			
		Ramp Scaling rfscale_rgbn[1:0]			
Dec	Binary	00 1x	01 2x slower	10 4x slower	11 8x faster
0	0000	2	2	2	2
1	0001	128	256	512	16
2	0010	256	512	1024	32
3	0011	384	768	1536	48
4	0100	512	1024	2048	64
5	0101	640	1280	2560	80
6	0110	768	1536	3072	96
7	0111	896	1792	3584	112
8	1000	1024	2048	4096	128
9	1001	1152	2304	4608	144
10	1010	1280	2560	5120	160
11	1011	1408	2816	5632	176
12	1100	1536	3072	6144	192
13	1101	1664	3328	6656	208
14	1110	1792	3584	7168	224
15	1111	1920	3840	7680	240

Note: There is only one Tramp Scaling register for both the rise and fall times.

Register DELAY_TIME_RGBn Delay time

The register DELAY_TIME_RGBn sets the delay time of starting flash function for each three LED(One RGB). Through setting different delay time for each RGB, it can realize four RGB LEDs to display in turns.

DELAY_TIME_RGBn [7:0] Delay time		
Dec	Binary	Period[s]
0	00000000	0
1	00000001	0.128
2	00000010	0.256
3	00000011	0.384
4	00000100	0.512
5	00000101	0.640
6	00000110	0.768
7	00000111	0.896

(Continued)

DELAY_TIME_RGBn [7:0] Delay time		
Dec	**Binary**	**Period[s]**
8	00001000	1.024
9	00001001	1.152
10	00001010	1.28
11	00001011	1.408
12	00001100	1.536
13	00001101	1.664
……	……	……
112	01110000	14.33
113	01110001	14.46
114	01110010	14.59
115	01110011	14.72
116	01110100	14.85
117	01110101	14.98
118	01110110	15.10
119	01110111	15.23
120	01111000	15.36
121	01111001	15.49
122	01111010	15.62
……	……	……
250	11111010	32
251	11111011	32.13
252	11111100	32.26
253	11111101	32.28
254	11111110	32.51
255	11111111	32.64s

Register LEDXMD_RGBn LED Work Mode Control

Register LEDXMD_RGBn sets the mode of each LED channel to either always ON/OFF or Thread1/Thread2/Thread3.

For example LEDXMD_RGBn= 00000001(binary), sets LED1/4/7/10 ON and other channels OFF.

Note: LED1/4/7/10 can't carry on Thread3, and LEDXMD_RGBn [7] and LEDXMD_RGBn [4] become 1, LED2/5/8/11 and LED3/6/9/12 will carry on Thread3.

LEDXMD_RGBn LED Work Mode Control			
Bit	**Binary**	**LEDX**	**Function**
[7:5]	000	LED3/6/9/12	Always OFF
	001		Always ON
	010		Thread1
	011		Thread2
	1xx		Thread3
[4:2]	000	LED2/5/8/11	Always OFF
	001		Always ON
	010		Thread1
	011		Thread2
	1xx		Thread3
[1:0]	00	LED1/4/7/10	Always OFF
	01		Always ON
	10		Thread1
	11		Thread2

Note: RGB0 corresponding to LED1/2/3, RGB1 corresponding to LED4/5/6, RGB2 corresponding to LED7/8/9, RGB3 corresponding to LED10/11/12.

Register EXPWM_EN External PWM input Enable Control

epen_rgbn	Function
0	Disable External PWM input function for RGBn
1	Enable External PWM input function for RGBn

Note: The corresponding LED should be set to work in “Always ON” state in using external PWM function, refer to register LEDXMD_RGBn.(n=0~3)

Register LEDn_CURT LED Current Setting

Registers LEDn_CURT(n=1~12) define the LED current setting for the channels D1 to D12 respectively. The LED current can be programmed with 192 steps between 0.125mA(The CHPCTR register bit2 imax_sel=0) or 0.25mA(imax_sel=1) minimum and 24mA(imax_sel=0) or 48mA(imax_sel=1) maximum.

For example, 24mA or 48mA is set by the code BF hexadecimal (191 decimal, 1011 1111 binary) or any higher code value. 10mA or 20mA current is set by the code 4F hexadecimal (79 decimal, 0100 1111 binary)

Data Dec	Data Hex	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Iout(mA) imax_sel=0	Iout(mA) imax_sel=1
0	00h	0	0	0	0	0	0	0	0	0.125	0.25
1	01h	0	0	0	0	0	0	0	1	0.25	0.5
2	02h	0	0	0	0	0	0	1	0	0.375	0.75

(Continued)

Data Dec	Data Hex	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Iout(mA) imax_sel=0	Iout(mA) imax_sel=1
3	03h	0	0	0	0	0	0	1	1	0.50	1.0
……	……	……	……	……	……	……	……	……	……	……	……
79	4Fh	0	1	0	0	1	1	1	1	10.00	20.00
80	50h	0	1	0	1	0	0	0	0	10.13	20.25
……	……	……	……	……	……	……	……	……	……	……	……
159	9Fh	1	0	0	1	1	1	1	1	20.00	40.00
160	A0h	1	0	1	0	0	0	0	0	20.13	40.25
……	……	……	……	……	……	……	……	……	……	……	……
190	BEh	1	0	1	1	1	1	1	0	23.88	47.75
191	BFh	1	0	1	1	1	1	1	1	24.00	48.00
192	C0h	1	1	0	0	0	0	0	0	24.00	48.00
……	……	……	……	……	……	……	……	……	……	……	……
254	FEh	1	1	1	1	1	1	1	0	24.00	48.00
255	FFh	1	1	1	1	1	1	1	1	24.00	48.00

Note: The 2 LSB's are timed division multiplexed (similar to PWM) by a digital interpolator. Minimum Iout unit is 0.5mA (imax_sel=0) or 1mA (imax_sel=1).

Serial Port Interface (I^2C)

Bus Interface

Baseband Processor can transmit data with ET6312B each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET6312B will send a low level response signal with one period width to the SDA port. During the reading mode, ET6312B will not send response signal and the host will send a high response

signal one period width to the SDA.

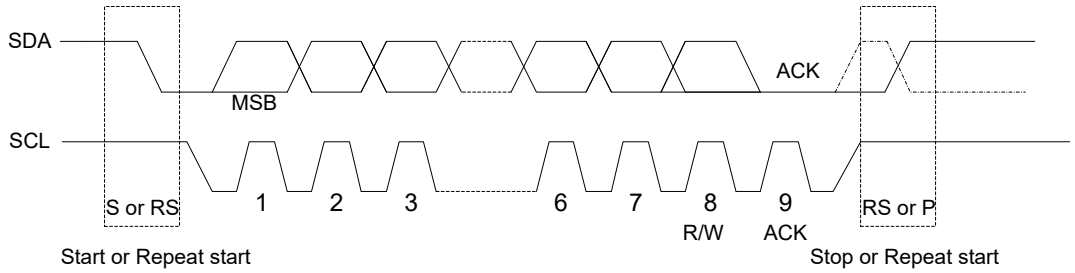


Figure3. I²C write mode

Note：ACK=Acknowledge

MSB=Most Significant Bit

S=Start Conditions RS=Restart Conditions P=Stop Conditions

Fastest Transmission Speed =400KBITS/S

Restart: SDA-level turnover as expressed by the dashed line waveform

Four I²C Chip Address with one ADDR pin

Four I²C Chip-Address		Description
ADDR Connect PIN	Chip address	W/R mode
GND	90H/91H	Writing/Reading Reg mode
SCL	92H/93H	Writing/Reading Reg mode
SDA	94H/95H	Writing/Reading Reg mode
VDD	96H/97H	Writing/Reading Reg mode

I²C Writing Command Register Interface Protocol (Continuous)：

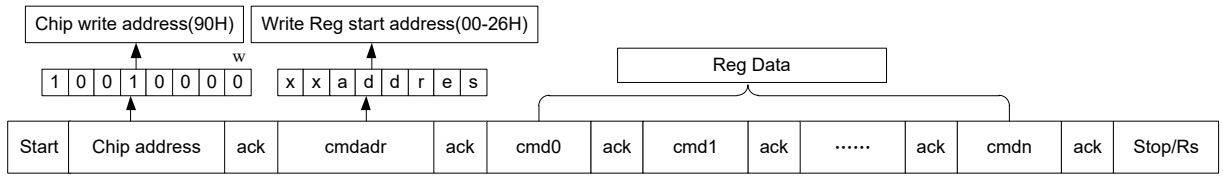


Figure4. I²C Writing Command Register(continuous)

- Start=Start Conditions
- Chip address=Write register address =1001000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(xx + REG's 6bit addres)
- ack=Acknowledge
- Reg data 0 = cmd0(Command data0)
- ack=Acknowledge

- ……
- Reg data n =cmdn(Command datan)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

I²C Writing Command Register Interface Protocol (single):

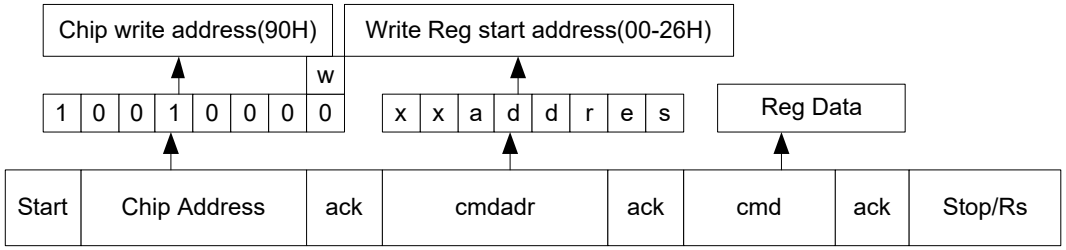


Figure5. I²C Writing Command Register(single)

- Start=Start Conditions
- Chip address =Write register address=1001000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(xx + REG's 6bit addres)
- ack=Acknowledge
- Reg data= cmd(Command data)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol

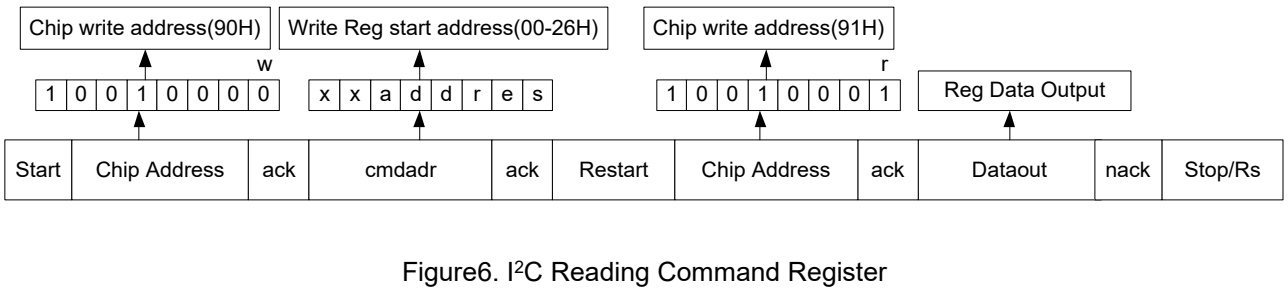


Figure6. I²C Reading Command Register

- Start=Start Conditions
- Chip address =Write register address=1001000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(xx + REG's 6bit addres)
- ack=Acknowledge
- Restart=Restart condition
- Chip address Read register address=1001000+1(r)b

- ack=Acknowledge
- Dataout=Register data output
- Nack=No Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

Voltage Headroom

The lowest headroom voltage is critical for systems with supply voltages nearing 3V, such as battery operated or regulated 3.3V systems. The advancement of LED technologies has made possible lower LED current and lower forward voltage drop (VF). For example, the majority of vendors' LED's VF at 5mA is 3.15V or below. With the cut-off voltage for most 1-cell Li+ powered systems set between 3.3V and 3.5V, it is possible to drive RGB LEDs without voltage step-up as long as the internal voltage drop for the driver circuit is specially designed for the lowest voltage possible.

Each current sink of the ET6312B is designed to allow the lowest operating input voltage without voltage step-up while maintaining current regulation, thus extending the battery run time. When input voltage is low, the internal low impedance current sink adds merely 75mV (typical) headroom on top of the LED forward voltage at 10mA per channel when CHIPCTR register bit2 imax_sel set to "0".

The formula is: $V_{IN(MIN)} = V_{F(MAX)} + V_{SINK(MIN)}$

When V_{IN} is the driving voltage applied to the anode of each LED, VF is the forward voltage drop of the LED, and V_{SINK} is the voltage at each Dx. When VIN is high (fully charged battery), VSINK is internally regulated to take the voltage difference between VIN and VF. For instance, if VIN is 4V and VF for LED1 is 3.1V, then VSINK at D1 pin is 0.9V.

When V_{IN} decreases (as the battery discharges), $V_{IN(MIN)}$ governs the lowest supply voltage for the LEDs without losing regulation. The design rule of thumb is to make sure the cut-off voltage is higher than VIN(MIN) for all conditions. It is important to emphasize the definition of "losing regulation"; in this datasheet it is defined as when the LED current drops to 90% of the nominal programmed current level.

At 10mA, the typical V_{SINK} can be as low as 75mV for each Dx pin. Since every LED has a slightly different VF at a given current, the minimum V_{IN} is determined by the highest VF plus 75mV typical. For the case of 10mA programmed current and highest VF of 3.2V, VIN in can go as low as 3.275V without losing LED current regulation. When V_{IN} drops further while the $V_{SINK(MIN)}$ remains constant, VF will be forced lower. As a result, the LED current will reduce according to each LED's V-I curve.

Absolute Maximum Ratings

Parameter	Range	Unit
VIN, D12~D1	-0.3 to 6.0	V
SCL, SDA	-0.3V to V_{IN}+0.3	V
Storage Temperature	-65 to 150	°C
Operating Temperature	-40 to 85	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Electrical Characteristics

D.C. Characteristics

V_{IN}=3.6V; T_A=25°C (Unless otherwise specified)

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
V_{IN}	Operating Voltage		2.7		5.5	V
V_{DPO}	Dx pin dropout voltage(90% Of nominal current)	All Channels set to 10mA LEDn_CURT=4FH,n=1~12 CHIPCTR bit2 imax_sel=0		75	120	mV
I_{SINK}	Out current accuracy	All Channels set to 20mA LEDn_CURT =9FH,n=1~12	-5		5	%
		All Channels set to 0.125mA LEDn_CURT=00H,n=1~12	-5		5	%
	Out current matching	All Channels set to 20mA LEDn_CURT=9FH,n=1~12	-5		5	%
I_{IN}	Supply Current	All 12 Channels set to 20mA LEDn_CURT=9FH,n=1~12		800		μA
		1 Channel set to 20mA Other channels OFF		450		μA
I_Q	IC quiescent Current	Device on,All LEDs OFF, LEDXMD_RGBn=00H,n=0~3		415		μA
I_{SHDN}	Shutdown Current	Shutdown Mode		0.1	1.0	uA
V_{IH}	Input high Voltage	SDA, SCL	1.2			V
V_{IL}	Input Low Voltage	SDA, SCL			0.4	V
T_{ST}	Thermal shutdown threshold			140		°C
T_{SH}	Thermal shutdown hysteresis			15		°C

I²C mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	0	-	400	KHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	1.3	-	-	μs
$t_{HD:STA}$	Hold Time(Repeated) START Condition	0.6	-	-	μs
t_{LOW}	Low Period of SCL Clock	1.3	-	-	μs
t_{HIGH}	HIGH Period of SCL Clock	0.6	-	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	0.6	-	-	μs
$t_{HD:DAT}$	Data Hold Time	0.1	-	0.9	μs
$t_{SU:DAT}$	Data Setup Time	100	-	-	ns
t_R	Data Hold Time2	-	20+0.1Cb(1)	300	ns
t_F	Data Hold Time2	-	20+0.1Cb(1)	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	0.6	-	-	μs

Note1: Cb=total capacitance of one bus line in PF.

I²C Mode Timing Diagram

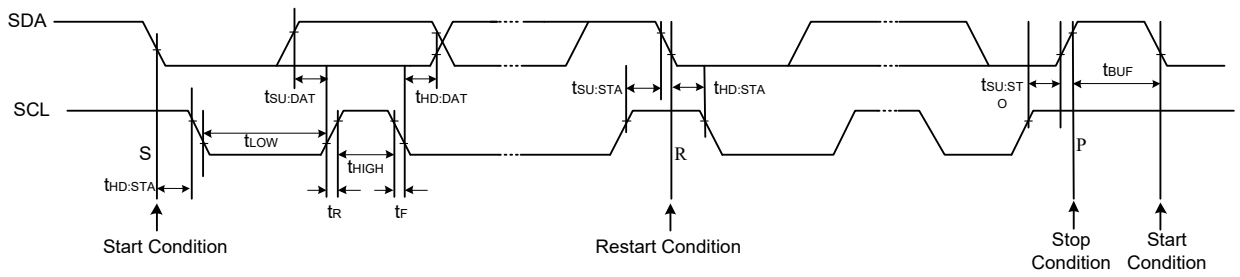
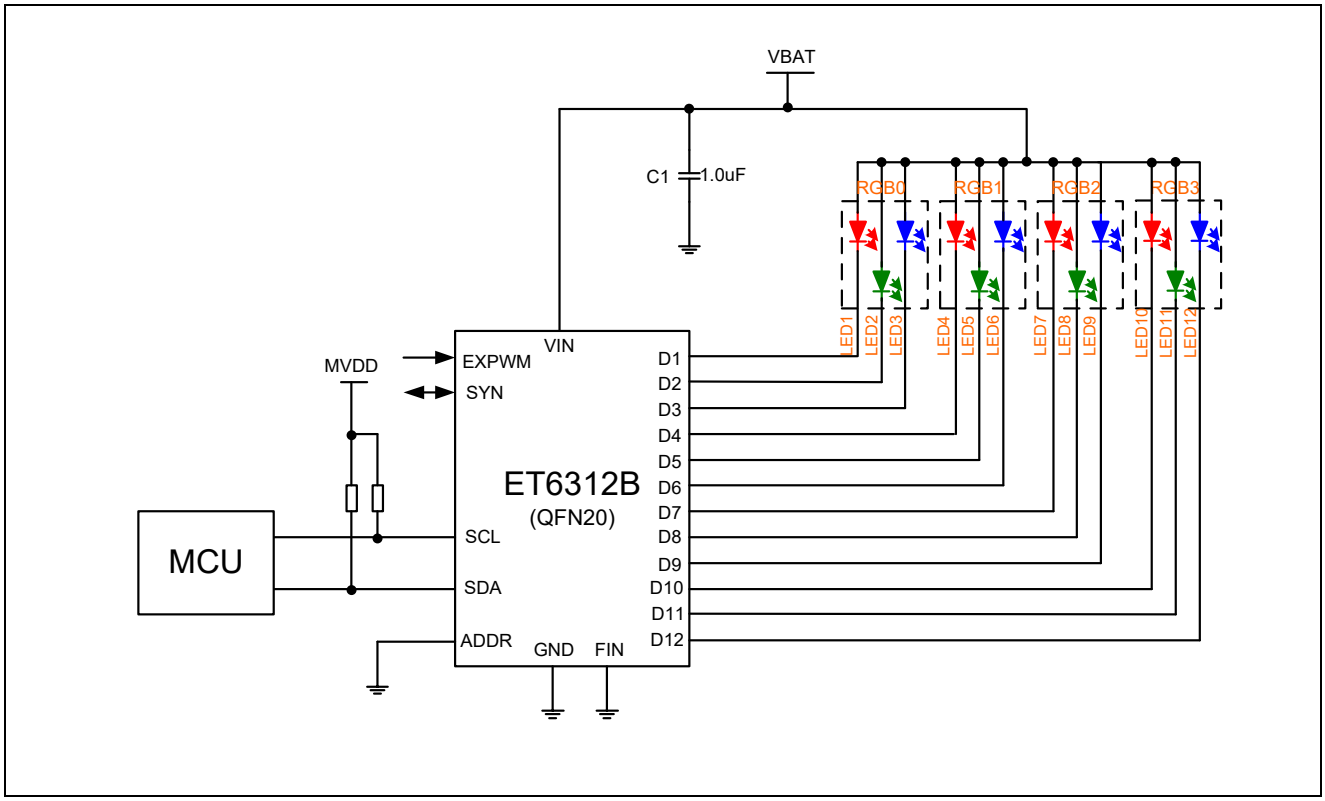


Figure7. I²C Timing Diagram

Application Circuits



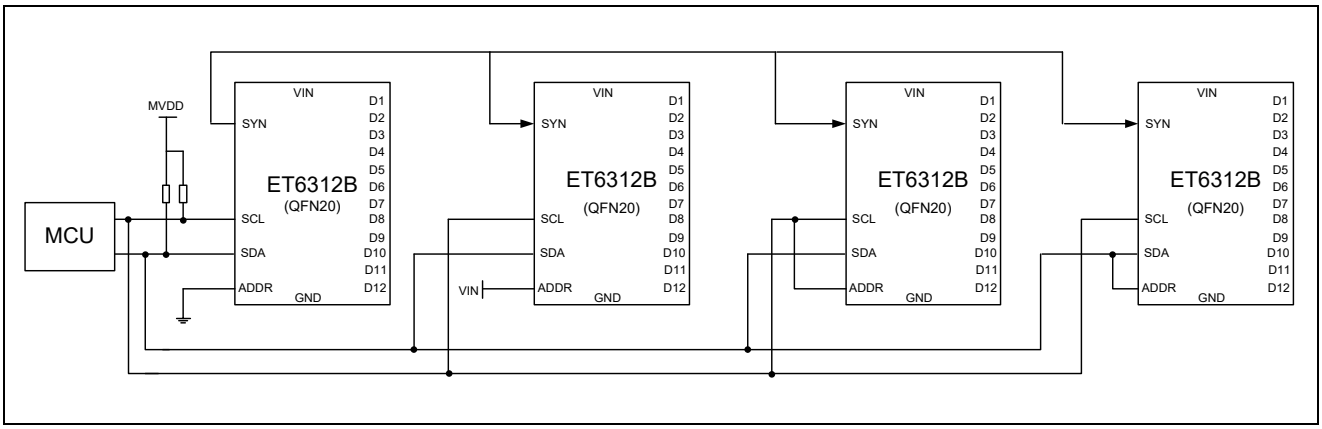
Notes: QFN20 package

(1) Chip Address is decided by ADDR pin connecting signal.

(2) SYN pin function is selected by CHIPCTR register bit6 and bit5.

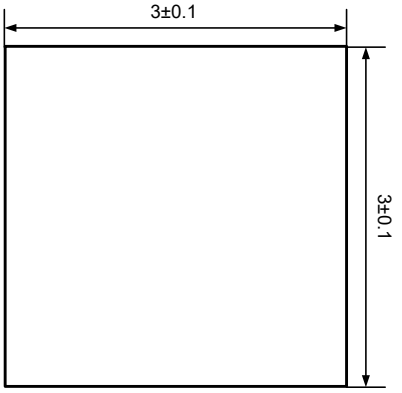
(3) EXPWM function is selected by EXPWM_EN register when LED is working in “ON” state.

Four chips cascade by a synchronous clock and a group of I²C bus

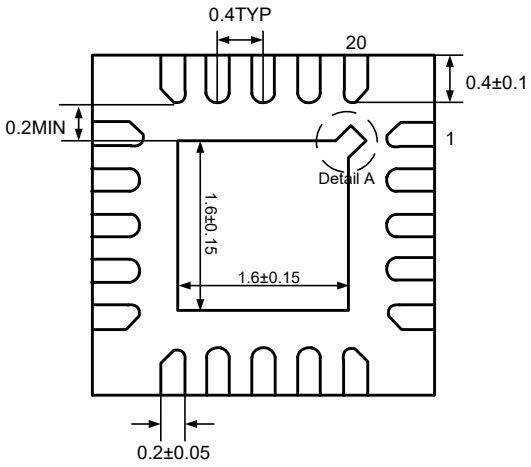


Package Dimension

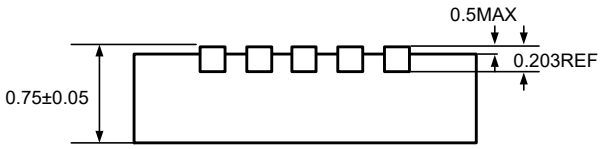
QFN20 (3mm×3mm×0.75mm)



TOP VIEW



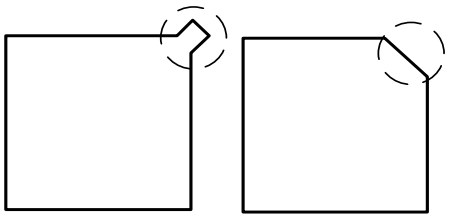
BOTTOM VIEW



SIDE VIEW

Unit: mm

Detail A(Thermal Pad shape):



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2016-09-12	Original Version	Sun Si Bing	Sun Si Bing	Zhu Jun Li
1.1	2016-09-21	Detailed the package dimension	Sun Si Bing	Sun Si Bing	Zhu Jun Li
1.2	2016-09-22	Update I_{IN}, I_Q value	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.3	2017-01-18	Updated AMR from 5.5V to 6.0V	Sun Si Bing	Sun Si Bing	Zhu Jun Li
1.4	2018-07-17	Correcting the Error(page8) FLASH_TON1_RGBn[7] to FLASH_PERIOD_RGBn[7]	Sun Si Bing	Sun Si Bing	Zhu Jun Li
1.5	2018-11-14	Correcting the Error(page2) SYN PIN Type from I to I/O	Sun Si Bing	Sun Si Bing	Zhu Jun Li
1.6	2021-6-30	Update Package Size	Sun Si Bing	Sun Si Bing	Zhu Jun Li
1.7	2023-8-30	Update Typeset	Zhuzq ,Shib	Sun Si Bing	Zhu Jun Li