Adjustable Voltage Monitor

General Description

The ET3896 low power voltage detector provides monitoring of battery, power-supply, and regulated system voltages. The devices is a very small supervisory circuits that monitor voltages greater than 500mV with a 0.25% (typical) threshold accuracy and offer adjustable delay time using external capacitors.

The ET3896 has a logic enable pin $\overline{EN}$ to power on and off the output, when the input voltage pin (IN) rises above the threshold, and the $\overline{EN}$ pin is high,then the output pin $\overline{OUT}$ goes high after the capacitor-adjustable delay time. When IN falls below the threshold or $\overline{EN}$ is low, then $\overline{OUT}$ goes low.

The ET3896 is available in ultra-small μDFN6 package and is fully specified over the temperature range of -40°C to 85°C.

Features

- Adjustable Threshold Down to 500mV
- Operate from V_{CC} of 1.7V to 6.5V
- Threshold Accuracy: 1% Over Temperature
- Capacitor-Adjustable Delay Time
- Low Quiescent Current is 6μA Typical
- External Enable Input
- Temperature Range from -40°C to 85°C
- Package Information:

Part No.	Package	MSL
ET3896	μDFN6(1.45 mm × 1.00 mm)	Level 1

Application

- Automotive
- DSPs, Microcontrollers and Microprocessors
- Notebook and Desktop Computers
- PDAs and Handheld Products
- Portable and Battery-Powered Products
- Medical Equipment
- FPGAs and ASICs

Pin Configuration

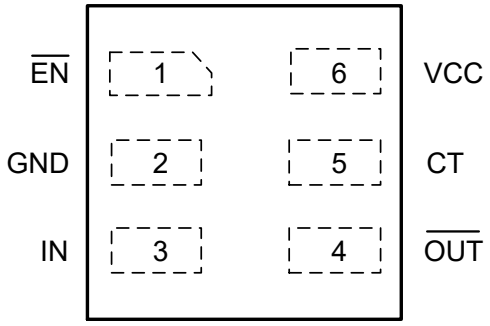


Figure1. TOP VIEW

Pin Function

Pin No.	Pin Name	I/O	Pin Function
1	$\overline{EN}$	I	Active low input. Driving $\overline{EN}$ high immediately makes $\overline{OUT}$ go high, independent of $V_{(IN)}$. With $V_{(IN)}$ already above V_{TH}, drive $\overline{EN}$ low to make $\overline{OUT}$ go low after the capacitor-adjustable delay time or 0.2μs (P version).
2	GND	-	Ground Pin.
3	IN	I	This pin is connected to the voltage that is monitored with the use of an external resistor. The output asserts after the capacitor-adjustable delay time when $V_{(IN)}$ rises above 0.5V and $\overline{EN}$ is asserted. The output deasserts after a minimal propagation delay (16μs) when $V_{(IN)}$ falls below $V_{TH} – V_{HYS}$.
4	$\overline{OUT}$	O	$\overline{OUT}$ is an push-pull output that is immediately driven high after $V_{(IN)}$ falls below ($V_{TH} – V_{HYS}$) or $\overline{EN}$ input is high. $\overline{OUT}$ goes low after the capacitor-adjustable delay time when $V_{(IN)}$ is greater than V_{TH} and the $\overline{EN}$ pin is low.
5	CT	I	Capacitor-adjustable delay. The CT pin offers a user-adjustable delay time. Connecting this pin to a ground referenced capacitor sets the delay time for IN rising above CT 0.5V to $\overline{OUT}$ asserting (or $\overline{EN}$ asserting to $\overline{OUT}$ asserting). $t_{pd(r)}$ (s) = [C_{CT} (μF) × 4] + 40μs
6	VCC	-	Power supply input. Connect a 1.7V to 6.5V supply to VCC to power the device. It is good analog design practice to place a 0.1μF ceramic capacitor close to this pin.

Block Diagram

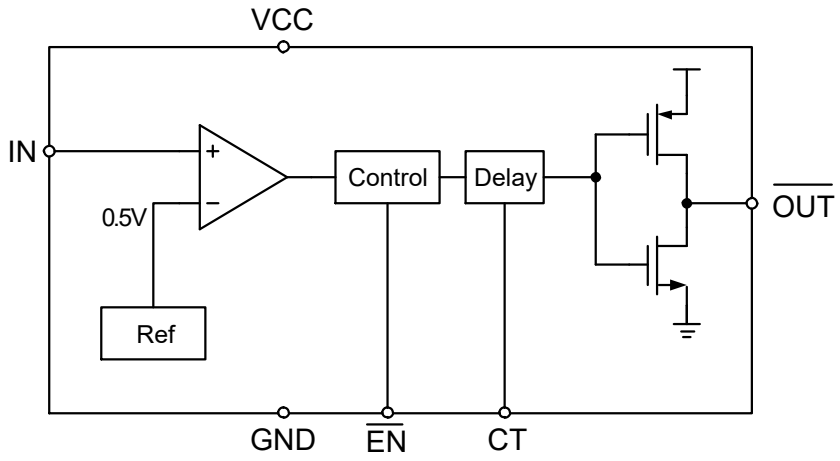


Figure2. ET3896 Block Diagram

Operation and Application Description

The ET3896 is a ultra-small supervisory circuits. When the IN pin rises above 0.5V and the enable input is asserted ($\overline{EN}$ = low), the output asserts ($\overline{OUT}$ goes low) after the capacitor-adjustable delay time. The IN pin can be set to any voltage threshold above 0.5V using an external resistor divider. A broad range of output delay times and voltage thresholds can be supported, allowing these devices to be used in wide array of applications.

Feature Description

The ET3896 provide push-pull outputs. The logic high level of the outputs is determined by the VCC pin voltage. With this configuration, pull-up resistors are not required and some board area can be saved. However, all the interface logic levels must be examined. All the $\overline{OUT}$ connections must be compatible with the VCC pin logic level.

The $\overline{OUT}$ outputs are defined for a V_{CC} voltage higher than $0.8V_{CC}$. Table 1 are truth tables that describe how the outputs are asserted or de-asserted. When the conditions are met, the device changes state from de-asserted to asserted after a preconfigured delay time. However, the transitions from asserted to de-asserted are performed almost immediately with minimal propagation delay of 16us (typical).

Conditions		Output	Status
$\overline{EN}$ = Low	IN < V_{TH}	$\overline{OUT}$ = High	Output not asserted
$\overline{EN}$ = High	IN < V_{TH}	$\overline{OUT}$ = High	Output not asserted
$\overline{EN}$ = High	IN > V_{TH}	$\overline{OUT}$ = High	Output not asserted
$\overline{EN}$ = Low	IN > V_{TH}	$\overline{OUT}$ = Low	Output asserted after delay

Table 1. ET3896 Truth Table

Input Pin (IN)

The IN input pin allows any system voltage above 0.5V to be monitored. If the voltage at the IN pin exceeds V_{TH}, and provided that the enable pin is asserted ($\overline{EN}$ =low), then the output is asserted after the capacitor-adjustable delay time elapses. When the voltage at the IN pin drops below (V_{TH} - V_{HYS}), then the output is de-asserted. The comparator has a built-in hysteresis to ensure smooth output assertions and de-assertions. Although not required in most cases, for extremely noisy applications, it is good analog design practice to place a 1nF to 10nF bypass capacitor at the IN input in order to reduce sensitivity to transients and layout parasitics.

The ET3896 monitor the voltage at IN with the use of external resistor divider, as shown in Figure 3.

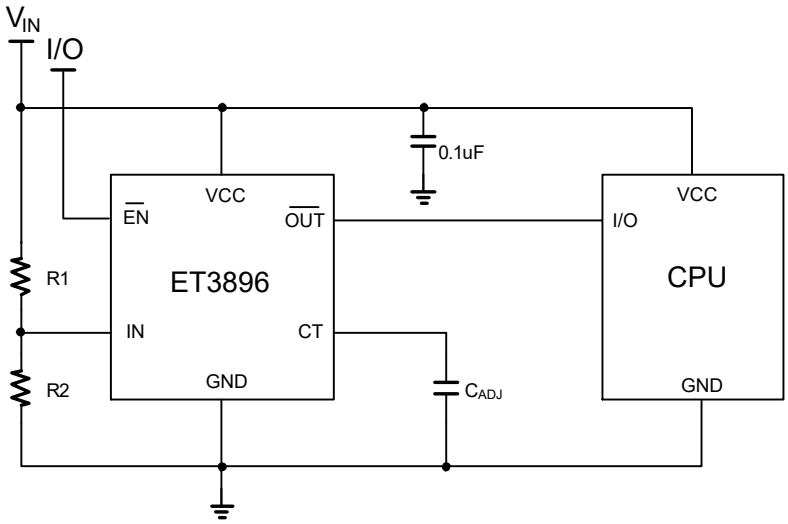


Figure 3. Using ET3896 to Monitor User-Defined Threshold Voltage

The target threshold voltage can be calculated by using Equation1:

$$V_{TARGET} = (1+R1/R2) \times 0.5\ (V) \quad (1)$$

When the input voltage (V_{IN}) is greater than V_{TARGET}, then the output is asserted, provided that the enable pin is asserted ($\overline{EN}$ = low). R1 and R2 can have high values (>100kΩ) to minimize current consumption as a result of a low IN input current without adding significant error to the resistive divider.

Enable Pin ($\overline{EN}$)

The enable input allows an external logic signal from other processors, logic circuits, and/or discrete sensors to turn on or turn off the output. Driving $\overline{EN}$ high forces $\overline{OUT}$ to go high. The 0.4V (maximum) low and 1.4V (minimum) high allow $\overline{EN}$ to be driven with a 1.5V or greater system supply.

ET3896 devices with V_{IN} > V_{TH}, driving $\overline{EN}$ low makes $\overline{OUT}$ go low after the capacitor-adjustable delay time.

Output Pin ($\overline{OUT}$)

In a typical ET3896 application, the $\overline{OUT}$ outputs are connected to a reset/enable input of the processor (DSP, CPU, FPGA, ASIC, and so on) or connected to the enable input of a voltage regulator.

Output Delay Time Pin (CT)

To program a user-defined, adjustable delay time, an external capacitor must be connected between the CT pin and GND. If the CT pin is left open, there will be a delay of 40us. The adjustable delay time can be calculated through Equation 2:

$$\mathbf{tpd(r)\ (s) = [C_{CT}(\mu F) \times 4] + 40\ (\mu s)} \quad \mathbf{(2)}$$

The reset delay time is determined by the time it takes an on-chip, precision 310nA current source to charge the external capacitor to 1.24V. When IN > V_{TH} and with $\overline{EN}$ low, the internal current sources are enabled and begin to charge the external capacitors. When the CTn voltage on a capacitor reaches 1.24V, the corresponding $\overline{OUT}$ is asserted. Note that a low-leakage type capacitor (such as ceramic) should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

The more precise of delay time can be calculated through Equation 3:

$$\mathbf{tpd(r)\ (s) = [C_{CT}(\mu F) \times 4] *(310nA/I_{CT})*(V_{CT}/1.24)+ 40\ (\mu s)} \quad \mathbf{(3)}$$

I_{CT} is the CT pin charge current;
V_{CT} is the CT pin comparator threshold voltage.

Immunity To IN Pin Voltage Transients

The ET3896 is relatively immune to short negative transients on the IN pin. Sensitivity to transients depends on threshold overdrive.

Device Functional Modes

- Normal Operation (V_{CC} > V_{CC}(min))

When the voltage on V_{CC} is greater than V_{CC}(min), the output corresponds to the voltages on the V_{CC} and $\overline{EN}$ pins relative to V_{TH}.

- Below V_{CC} (min) (V_{POR} < V_{CC} < $V_{CC(min)}$)

When the voltage on V_{CC} is less than V_{CC}(min) but greater than the power-on reset voltage (V_{POR}), the output is de-asserted ($\overline{OUT}$ is high).

- Below Power-On Reset (V_{CC} < V_{POR})

When the voltage on V_{CC} is lower than the power-on reset voltage (V_{POR}), the output is undefined. Do not rely on the output for proper device function under this condition.

PCB Layout Guide

Follow these guidelines to lay out the printed-circuit-board (PCB) that is used for the ET3896.
Place the V_{CC} decoupling capacitor close to the device.
Avoid using long traces for the V_{CC} supply node. The VCC capacitor (C_{VCC}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum V_{CC} voltage.

Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 1.7V to 6.5V. Though not required, it is good analog design practice to place a 0.1uF ceramic capacitor close to the VCC pin.

Single-Rail Monitoring

The ET3896 can be used to monitor the supply rail for devices such as digital signal processors (DSPs), central processing units (CPUs), or field-programmable gate arrays (FPGAs). The downstream device is enabled by the ET3896 once the voltage on the IN pin (V_{IN}) is above the threshold voltage ($V_{TH)}$ set by the resistor divider. The downstream device is disabled by the ET3896 when V_{IN} is falls below the threshold voltage minus the hysteresis voltage (V_{TH} - V_{HYS}).

Design Requirements

The ET3896 must drive the enable pin of devices using a logic-high signal to signify that the supply voltage is above the minimum operating voltage of the device.

Detailed Design Procedure

Select R1 and R2 so the voltage at IN (V_{IN}) is above the positive-going threshold voltage (V_{TH}) at the supply voltage required for proper device operation (that is, proper operation of the DSP, CPU, FPGA, and so on). Also, ensure that the current that flows from the supply voltage to ground through the resistor divider is at least 100 times larger than the input current (I_{IN}).

If an output delay time is required, connect a capacitor from CT to GND; see the Output Delay Time Pin (CT) section for more information. If no CT cap is connected, the delay time is 40us.

Absolute Maximum Ratings

Parameter	Rating	Unit
VCC, $\overline{EN}$ (push-pull) Voltage	-0.3 to 7.0	V
CT, $\overline{OUT}$ Voltage	-0.3 to V_{CC} + 0.3	V
$\overline{OUT}$ Current	-10 to 10	mA
Power Dissipation	200	mW
Package Thermal Resistance (θ_{JA})	250	°C/W
Operating Junction Temperature	-40 to 125	°C
Storage Temperature	-65 to 150	°C

Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Input supply voltage	V_{CC}	1.7	6.5	V
$\overline{EN}$ pin voltage	V_{EN}	0	6.5	V
IN pin voltage	V_{IN}	0	6.5	V
$\overline{OUT}$ pin voltage	V_{OUT}	0	V_{CC}	V
$\overline{OUT}$ pin current	I_{OUT}	0.0003	1	mA

Electrical Characteristics

V_{CC}=1.7V to 6.5V, T_A= -40°C to +85°C, unless otherwise specified.

Typical values are at V_{CC} = 3.3V and T_A = +25°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Operating voltage range	T_A= 0°C to 85°C	1.65		6.5	V
V_{POR}	Power-on reset voltage	$V_{OH\ (MIN)}$ =V_{CC}-0.2V, I_{OUT}=15μA			1	V
I_{CC}	Supply current (into VCC pin)	V_{CC} = 3.3V , no load		5.5	11	uA
		V_{CC} = 6.5V , no load		6.5	11	
V_{TH}	Positive-going input threshold voltage	V_{IN} rising	0.495	0.500	0.505	V
V_{HYS}	Hysteresis voltage	V_{IN} falling		3		mV
I_{IN}	Input current	V_{IN} = 0V or V_{CC}	-15		15	nA
I_{CT}	CT pin charge current		260	310	350	nA
V_{CT}	CT pin comparator threshold voltage		1.18	1.23	1.28	V
R_{CT}	CT pin pull-down resistance			200		Ω
V_{IL}	$\overline{EN}$ Low-level input voltage				0.4	V
V_{IH}	$\overline{EN}$ High-level input voltage		1.4			V
V_{UVLO}	Under-voltage Lockout	V_{CC} falling	1.3		1.7	V
I_{LEAK}	Leakage current	$\overline{EN}$ = GND	-100		100	nA
V_{OL}	Low-level output voltage	V_{CC} ≥ 2.25V, Isink = 0.5mA			0.3	V
		V_{CC} ≥ 4.5V, Isink = 1mA			0.4	
V_{OH}	High-level output voltage	V_{CC} ≥ 2.25V, Isource = 0.5mA	0.8V_{CC}			V
		V_{CC} ≥ 4.5V, Isource = 1mA	0.8V_{CC}			

Timing Requirements

V_{CC}=1.7V to 6.5V, T_A= -40°C to +85°C, unless otherwise specified.

Typical values are at V_{CC} = 3.3V and T_A = +25°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{pd(r)}$	IN (rising) to IN- $\overline{OUT}$ propagation delay	$V_{(IN)}$ rising, $C_{(CT)}$=open		40		us
		$V_{(IN)}$ rising, $C_{(CT)}$=0.047uF		190		ms
$t_{pd(f)}$	IN (falling) to IN- $\overline{OUT}$ propagation delay	$V_{(IN)}$ falling		16		us
t_{star}	Start-up delay(1)			50		us
t_w	$\overline{EN}$ pin minimum pulse duration		1			us
	EN pin glitch rejection			100		ns
$t_{d(OFF)}$	$\overline{EN}$ to IN- $\overline{OUT}$ delay time (output disabled)	$\overline{EN}$ de-asserted to output de-asserted		200		ns
$t_{d(A)}$	$\overline{EN}$ to IN- $\overline{OUT}$ delay time	$\overline{EN}$ asserted to output asserted delay , $C_{(CT)}$ = open		20		us
		$\overline{EN}$ asserted to output asserted delay, $C_{(CT)}$ = 0.047uF		190		ms

Notes:

1. During power on,V_{CC} must exceed 1.7V for at least 50us (plus propagation delay time, $t_{pd(r)}$) before output is in the correct state.

2. tpd(r) decreases with the increase of V_{CC}, the typical characteristics are shown in the following table 2:

(T_A= +25°C ,C_{CT}=0.1uF)

V_{CC}	1.7V	2V	2.5V	3V	3.5V	4V	4.5V	5V	5.5V	6V	6.5V
$t_{pd(r)}$	407ms	406ms	405ms	405ms	405ms	405ms	404ms	402ms	397ms	386ms	370ms

Table 2. ET3896 $t_{pd(r)}$ vs V_{CC}

Timing Diagram

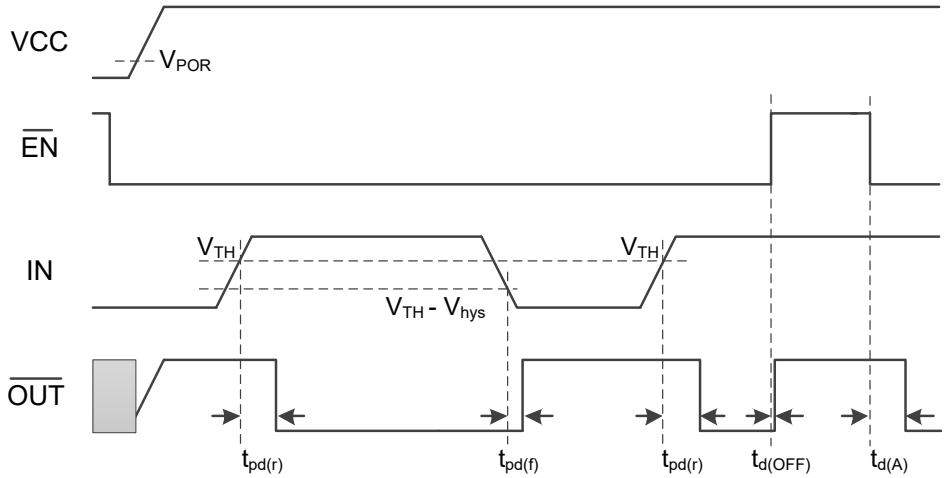


Figure 4. ET3896 Timing

Application Circuits

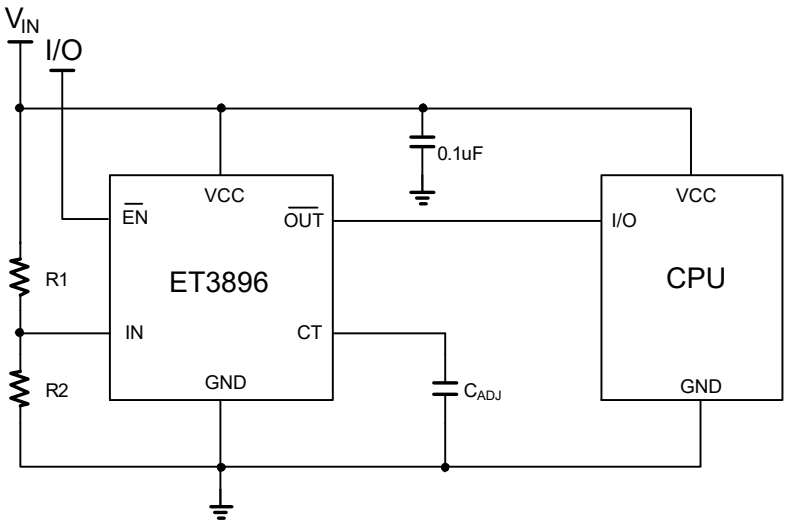
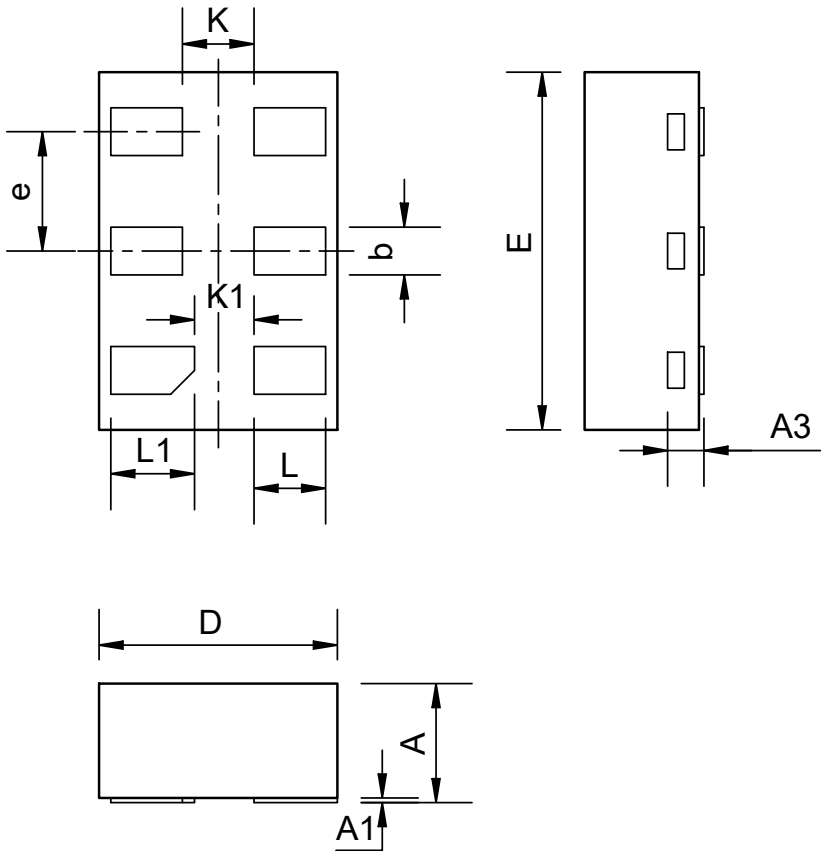


Figure 5. ET3896 Typical Application

Package Dimension



COMMON DIMENSIONS

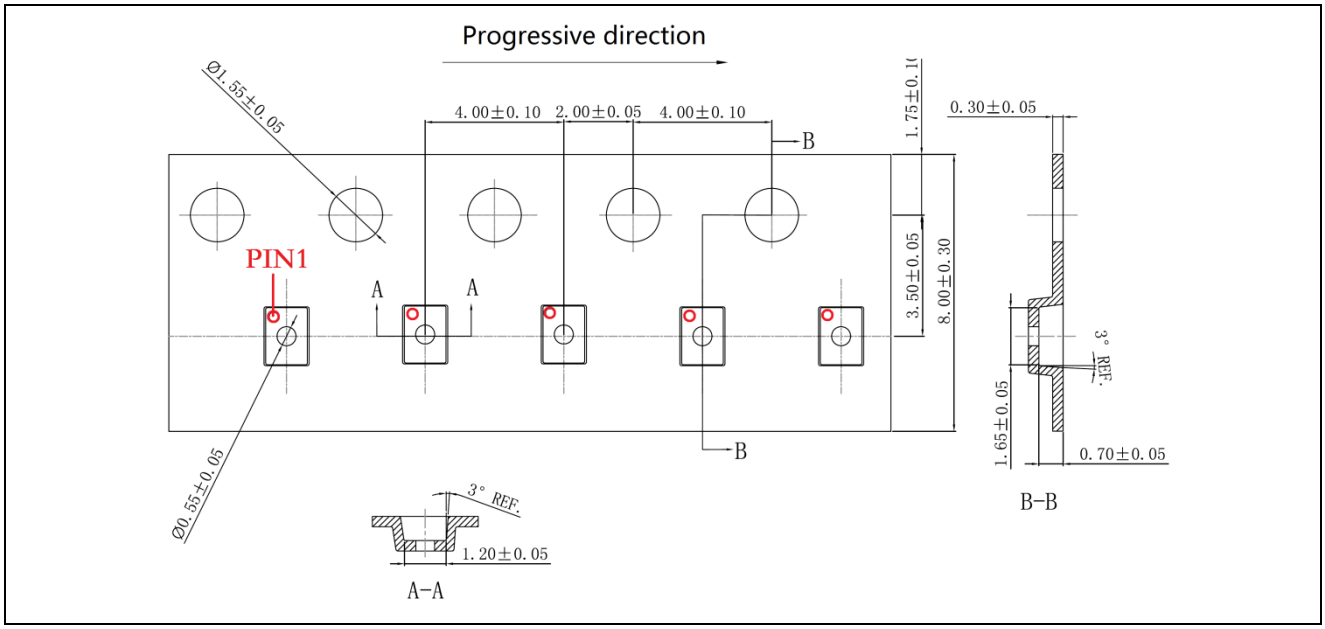
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.45	0.5	0.55
A1	0.02REF		
A3	0.152REF		
b	0.15	0.2	0.25
D	0.9	1	1.1
E	1.35	1.45	1.55
e	0.5BSC		
K	0.3REF		
K1	0.25REF		
L	0.224	0.3	0.376
L1	0.274	0.35	0.426

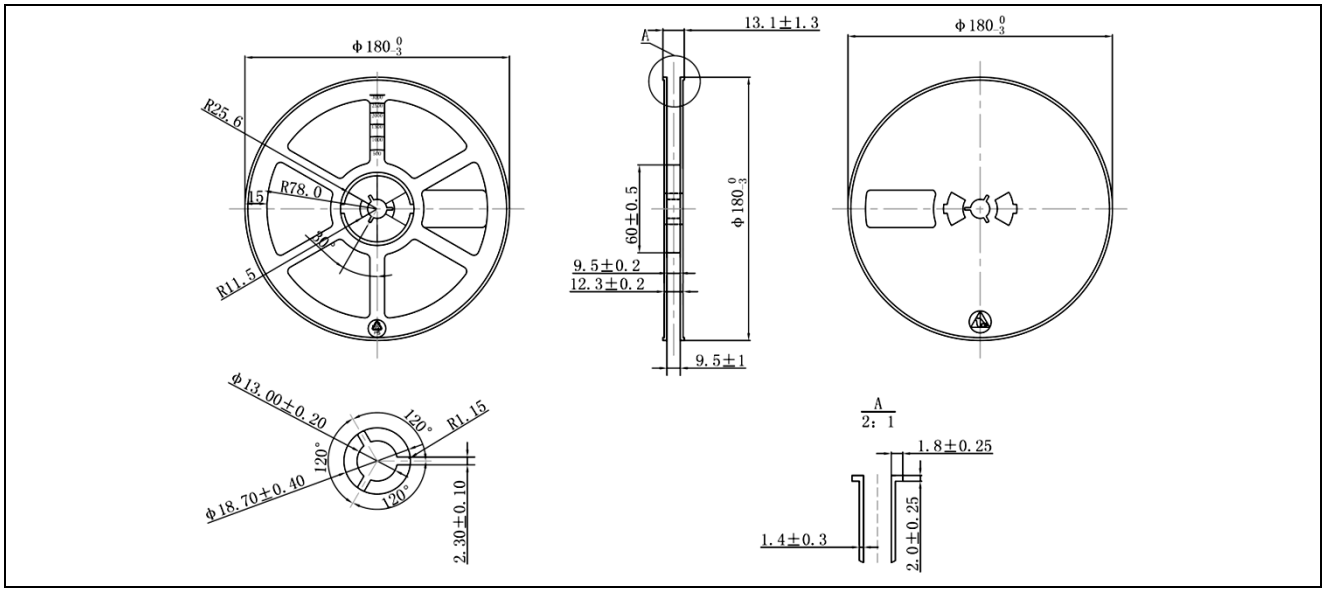
Packing Information

Package Type	Reel Dimension	Units/ Reel	Inner Box Dimension (mm^3)	Reel /Inner Box	Units/ Inner Box	Outer Box Dimension (mm^3)	Inner Boxes/ Outer Box	Units/ Outer Box
DFN6	Listed Below	3000	210×208×203	10	30k	440×440×230	4	120K

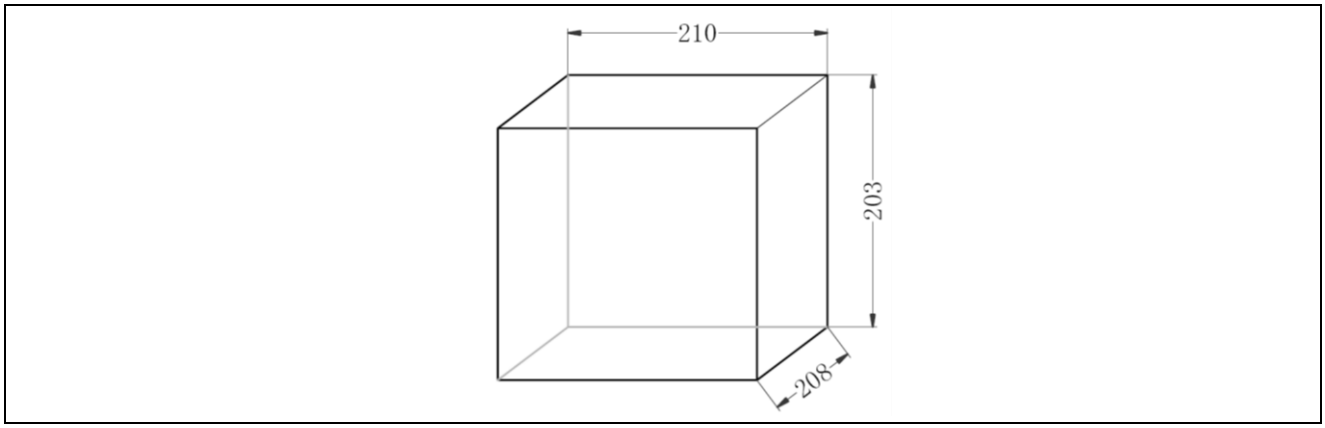
Tape



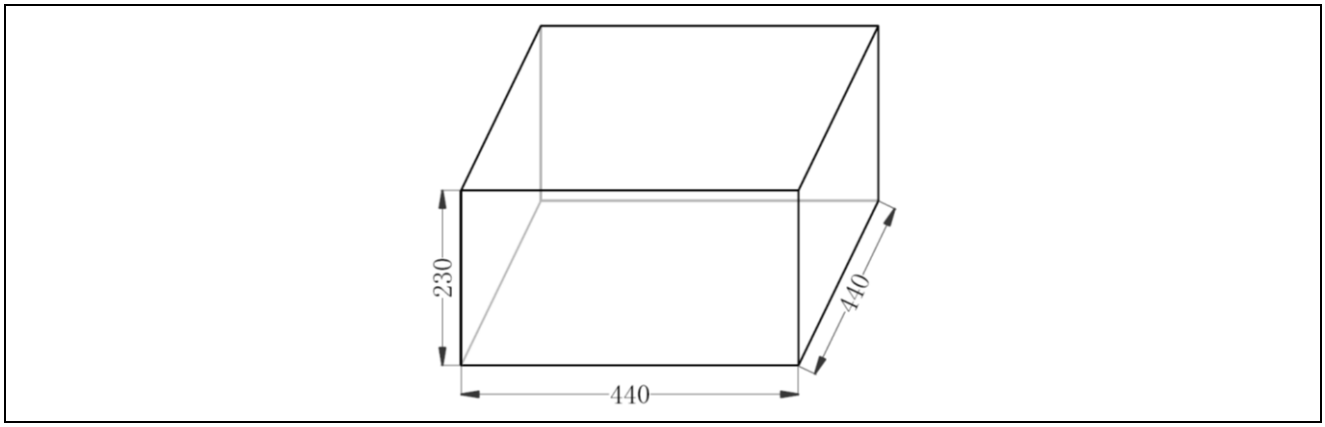
Reel



Inner Box



Outer Carton



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2016-03-15	Original Version	Liu Yi Guo	Liu Yi Guo	Zhu Jun Li
1.1	2016-08-25	Make dimension package with ±tolerance	Liu Yi Guo	Liu Yi Guo	Zhu Jun Li
1.2	2017-03-16	Add packing information	Liu Yi Guo	Liu Yi Guo	Zhu Jun Li
1.3	2017-03-21	1.Remove preliminary 2. Updated V(POR) Released Version	Liu Yi Guo	Liu Yi Guo	Zhu Jun Li
1.4	2017-04-19	Add tpd(r) decreases with the increase of VCC and Equation 3	Liu Yi Guo	Liu Yi Guo	Zhu Jun Li
1.5	2020.3.13	Document check and formalize	Shibo	Shibo	Shibo
1.6	2022.12.9	Update Typeset	Hu Yun Tao	Hu Yun Tao	Zhu Jun Li