ET64C16 - 16 bit I²C-bus/SMBus I/O Expander

General description

The ET64C16 is a 16-bit general purpose I/O expander that provides remote I/O expansion for most micro-controller families via the I²C-bus interface.

ET64C16 provides a simple solution for I/O port expansion, which can be realized with little interconnection. In addition to providing a set of flexible GPIO ports, it also supports the level conversion between different voltage devices, so that it can be flexibly applied in multi voltage mixed signal environment.

ET64C16 has four pairs of 8-bits registers: configuration register, input register, output register and polarity reversal register.

When power-on, all I/O ports are configured to input status. By configuring the I/O ports' configuration register, the system can determine the input and output status of each I/O port. Each input or output data is stored in the corresponding input or output register. The polarity of input registers can be flipped by configuring polarity reversal registers to save external logic gates.

When any input state is different from its corresponding input register state, the ET64C16 open drain interrupt ($\overline{INT}$) output is active to indicate to the host that the input state has changed.

The $\overline{INT}$ can be connected to the interrupt input of the micro-controller. By sending the interrupt signal, the micro-controller port is informed that there is data entering, instead of passing through I²C BUS.

The Port P output of ET64C16 can provide 25mA perfusion current, which can directly drive LED.

The hardware address pin (A2、A1、A0) can be used to program and change the I²C BUS address.

Features

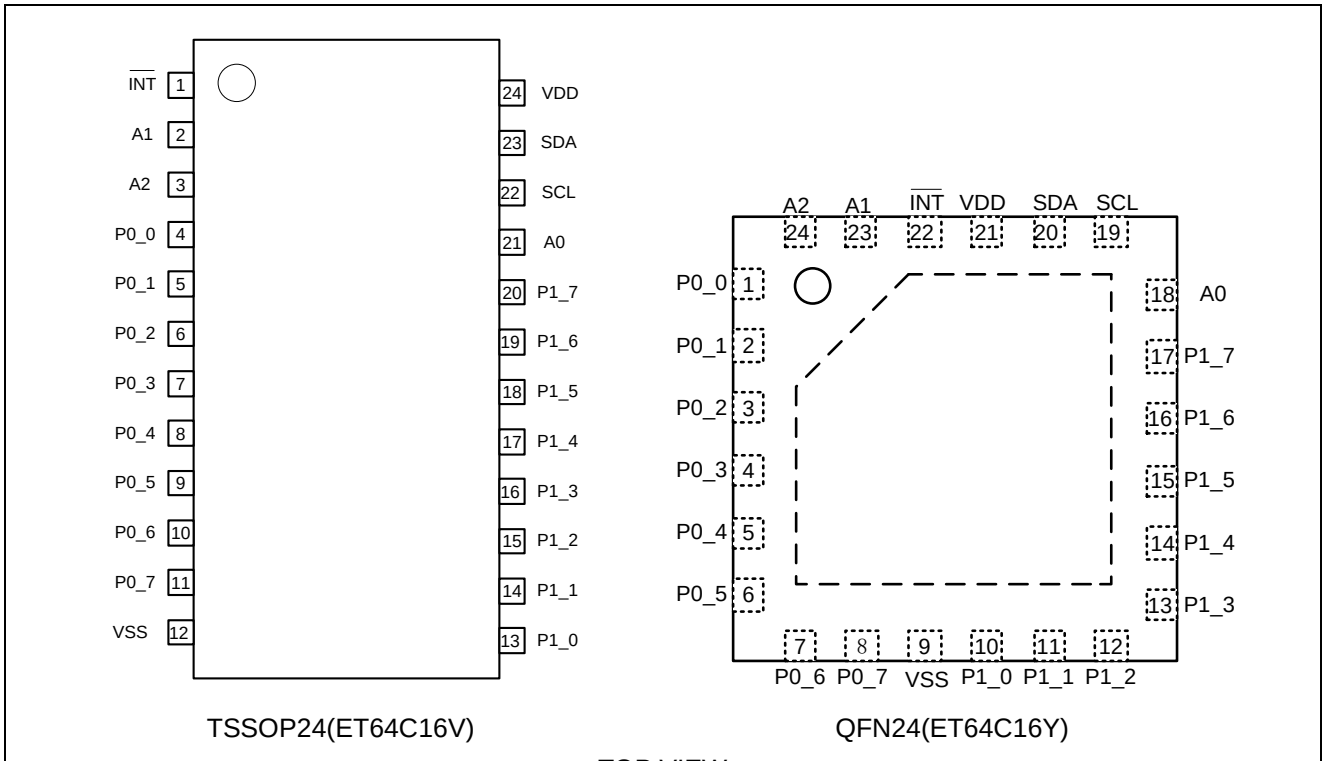
- 16 bit I²C-BUS to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption
  - 1.5 uA typical at V_{DD}=5 V
  - 1.0 uA typical at V_{DD}=3.3 V
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - V_{HYS} = 0.15 V (typical) at 1.8 V
  - V_{HYS} = 0.20 V (typical) at 2.5 V
  - V_{HYS} = 0.26 V (typical) at 3.3 V
  - V_{HYS} = 0.45 V (typical) at 5.0 V
- 5 V tolerant I/O ports
- Open-drain active LOW interrupt output ($\overline{INT}$)

- 400 kHz Fast-mode I²C-BUS
- Input/Output Configuration register
- Polarity Inversion register
- Internal power-on reset
- Power-up with all channels configured as inputs
- No glitch on power-up
- Noise filter on SCL/SDA inputs
- Outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA
- ESD protection exceeds
  - ±2000 V Human-Body Model Pass
  - ±1000 V Charged-Device Model Pass

Device Information

Part No.	Package	Size
ET64C16Y	QFN24	4mm × 4mm × 0.75mm
ET64C16V	TSSOP24	4.4mm ×7.8mm

Pin Assignments



TSSOP24(ET64C16V) QFN24(ET64C16Y)

TOP VIEW

Figure 1. Pin Assignments

Pin. Function

Pin No.	Pin Name		Description
	TSSOP24	QFN24	
$\overline{INT}$	1	22	Interrupt output. Connect to VDD through a pull-up resistor.
A1	2	23	Address input1. Connect directly to VDD or GND.
A2	3	24	Address input2. Connect directly to VDD or GND.
P0_0	4	1	Port 0 input/output 0.
P0_1	5	2	Port 0 input/output 1.
P0_2	6	3	Port 0 input/output 2.
P0_3	7	4	Port 0 input/output 3.
P0_4	8	5	Port 0 input/output 4.
P0_5	9	6	Port 0 input/output 5.
P0_6	10	7	Port 0 input/output 6.
P0_7	11	8	Port 0 input/output 7.
VSS	12	9	GND port
P1_0	13	10	Port 1 input/output 0.
P1_1	14	11	Port 1 input/output 1.
P1_2	15	12	Port 1 input/output 2.
P1_3	16	13	Port 1 input/output 3.
P1_4	17	14	Port 1 input/output 4.
P1_5	18	15	Port 1 input/output 5.
P1_6	19	16	Port 1 input/output 6.
P1_7	20	17	Port 1 input/output 7.
A0	21	18	Address input0. Connect directly to VDD or GND.
SCL	22	19	Serial clock bus. Connect to VDD through a pull-up resistor.
SDA	23	20	Serial data bus. Connect to VDD through a pull-up resistor.
VDD	24	21	Supply voltage of ET64C16.

Block Diagram

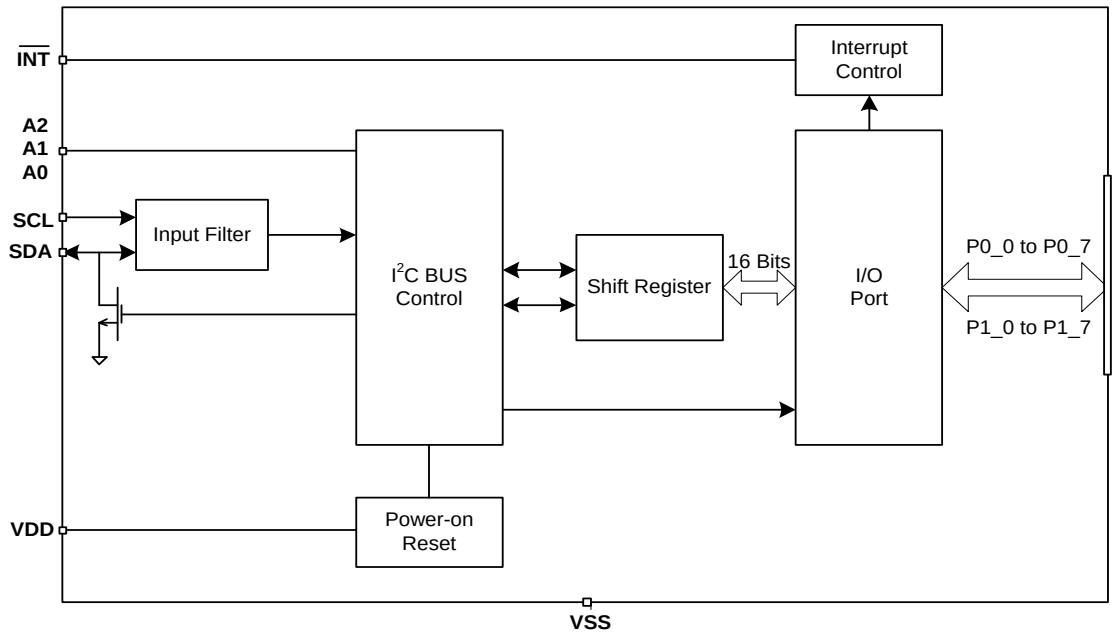


Figure 2. Block Diagram

Functions Description

BUS Transactions

The ET64C16 is an I²C-bus slave device. Data is exchanged between the master and ET64C16 through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Chip Address

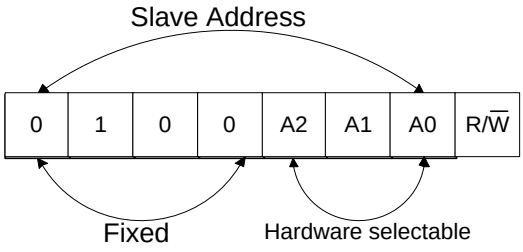


Figure 3. Chip address

ADDR (A0,A1,A2) is the hardware address package pin and is held to either HIGH (logic 1) or LOW (logic 0) to assign one of the two possible slave addresses. The last bit of the slave address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

Write Commands

Data is transmitted to the ET64C16 by sending the device address and setting the Least Significant Bit (LSB) to a logic ‘0’. The command byte is sent after the address and determines which register receives the data that follows the command byte.

The eight registers within the ET64C16 are configured to operate as four register pairs. The four pairs are input Resisters, output Resisters, polarity inversion and configuration Registers. After sending data to one register, the next data byte is sent to the other register in the pair. For example, if the first byte is sent to Output Resisters1 (register 3), the next byte is stored in Output Resisters0 (register 2).

There is no limit on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register pair independently of the other registers or the host can simply update a single register.

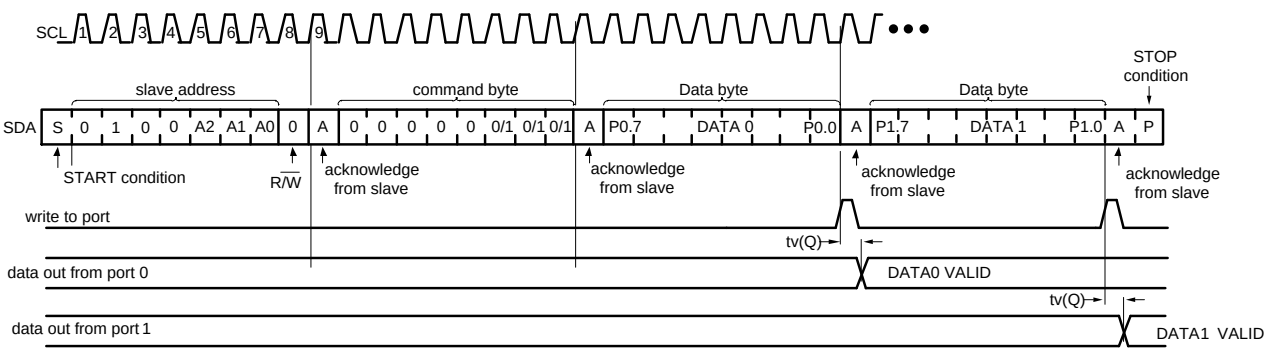


Figure 4. Write Commands

Read Commands

To read data from the ET64C16, the bus master must first send the ET64C16 address with the least significant bit set to a logic ‘0’. The command byte is sent after the address and determines which register is to be accessed.

After a restart, the device address is sent again, but this time the least significant bit is set to a logic ‘1’. Data from the register defined by the command byte is sent by the ET64C16. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflects the information in the other register in the pair. For example, if Input Resisters 1 is read, the next byte read is Input Resisters 0.There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

After a subsequent restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Resisters 1 was read last before the restart, the register that is read after the restart is the Input Resisters 0.

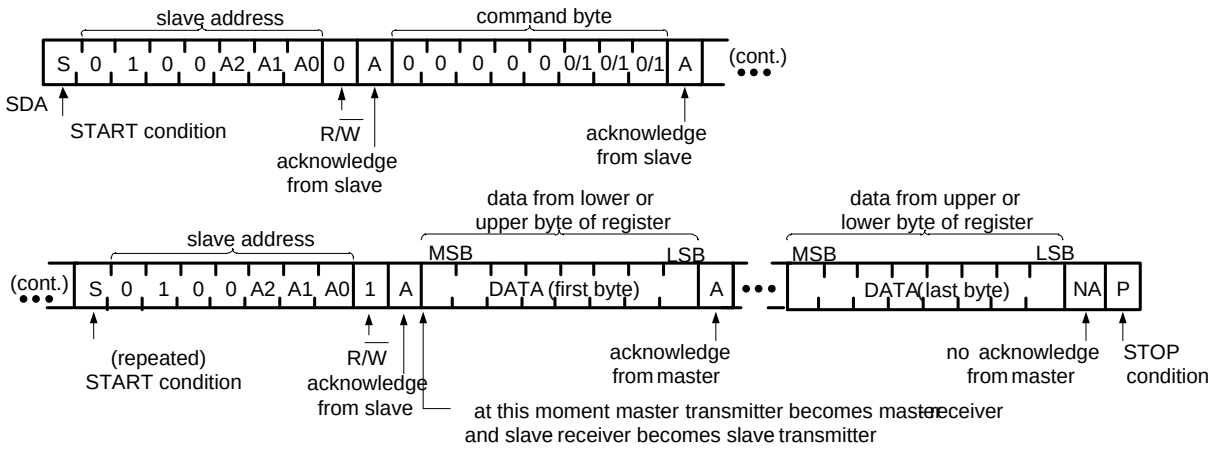


Figure 5. Read Commands

I/O Port

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either VDD or VSS . The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

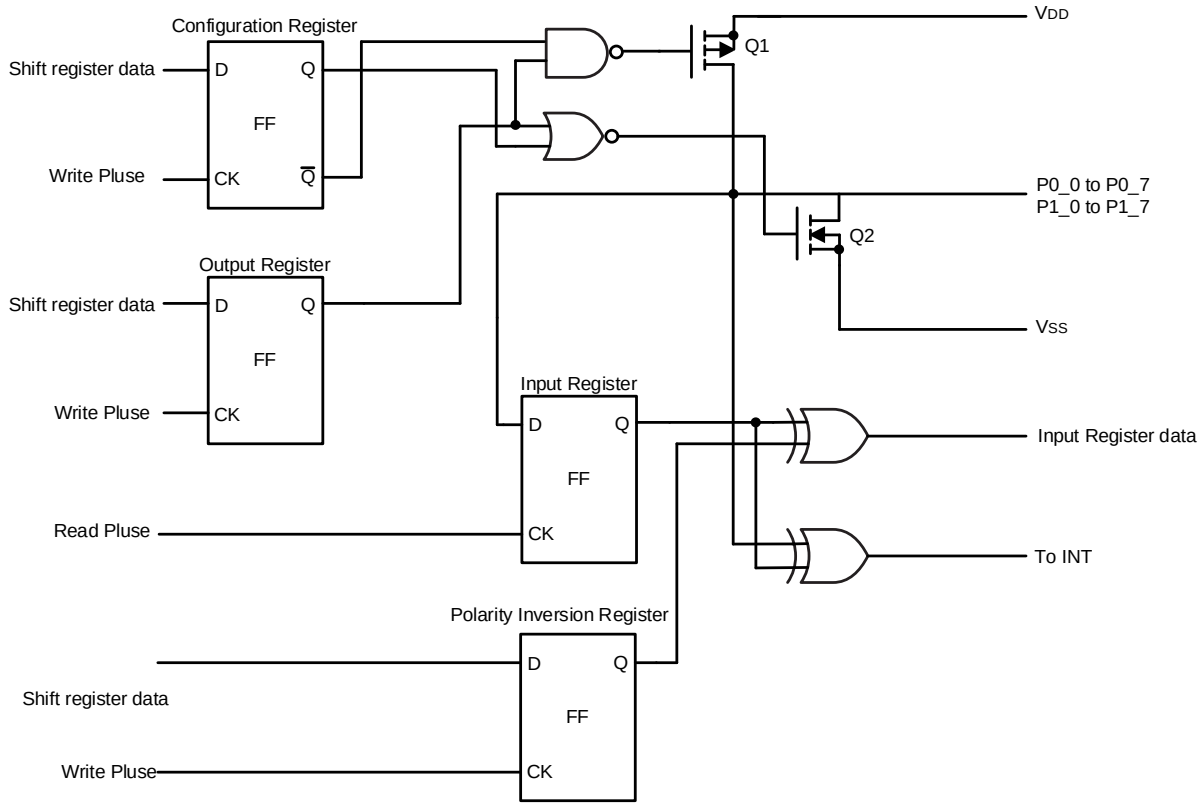


Figure 6. I/O Ports

Power-on Reset

When power (from 0 V) is applied to VDD , an internal power-on reset holds the ET64C16 in a reset condition until VDD has reached VPOR. At that time, the reset condition is released and the ET64C16 registers and I²C-bus/SMBus state machine initializes to their default states. After that, VDD must be lowered to below VPOR and back up to the operating voltage for a power-reset cycle.

Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time tv($\overline{INT}$) , the signal $\overline{INT}$ is valid. The interrupt is reset when data on the port changes back to the original value or when data is read from the port that generated the interrupt. Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to VDD depending on the application. $\overline{INT}$ should be connected to the voltage source of the device that requires the interrupt information.

Interface definition

Byte	Bit							
	7(MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0(LSB)**
I²C-BUS slave address	L	H	L	L	A2	A1	A0	R/W
I/O data bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Pointer register and Command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the ET64C16. The lower three bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register is write only.

While a new command has been sent, the register that was last addressed continues to be accessed by reads until a new command byte is sent.

Pointer Register Bits	Command Byte	Register	Protocol	Default Value
0000 0000	00h	Input Registers 0	Read only	xxxx xxxx
0000 0001	01h	Input Registers 1	Read only	xxxx xxxx
0000 0010	02h	Output Registers 0	Read/Write	1111 1111
0000 0011	03h	Output Registers 1	Read/Write	1111 1111
0000 0100	04h	Polarity inversion Registers 0	Read/Write	0000 0000

Pointer Register Bits	Command byte	Register	Protocol	Default Value
0000 0101	05h	Polarity inversion Registers 1	Read/Write	0000 0000
0000 0110	06h	Configuration Registers 0	Read/Write	1111 1111
0000 0111	07h	Configuration Registers 1	Read/Write	1111 1111

Register descriptions

Register	Bits	7	6	5	4	3	2	1	0
00h	Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
	Default	X	X	X	X	X	X	X	X
01h	Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
	Default	X	X	X	X	X	X	X	X
02h	Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
	Default	1	1	1	1	1	1	1	1
03h	Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
	Default	1	1	1	1	1	1	1	1
04h	Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
	Default	0	0	0	0	0	0	0	0
05h	Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
	Default	0	0	0	0	0	0	0	0
06h	Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
	Default	1	1	1	1	1	1	1	1
07h	Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
	Default	1	1	1	1	1	1	1	1

Input Registers（00h、01h）

The Input registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect.

The default value ‘X’ is determined by the externally applied logic level.

Output Registers（02h、03h）

The Output registers (registers 2 and 3) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, not the actual pin value.

Polarity inversion Registers（04h、05h）

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with ‘1’), the corresponding port pin’s polarity is inverted in the input register. If a bit in this register is cleared (written with a ‘0’), the corresponding port pin’s polarity is retained.

Configuration Registers（06h、07h）

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output.

Note： When the P port is suspended, configure it to the output state please.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		-0.5	+6.5	V
V_I	Input voltage		-0.5	+6.5	V
V_O	Output voltage		-0.5	+6.5	V
I_{IK}	Input clamping current	A2, A1, A0, SCL; V_I < 0V		±20	mA
I_{OK}	Output clamping current	$\overline{INT}$; V_O < 0V		±20	mA
I_{IOK}	Input/output clamping current	P port, SDA; V_O < 0V or V_O > V_{DD},		±20	mA
I_{OL}	LOW-level output current	P port, SDA, $\overline{INT}$; V_O = 0V to V_{DD}		50	mA
		SDA, $\overline{INT}$; V_O = 0V to V_{DD}		25	mA
I_{OH}	HIGH-level output current	P port; V_O = 0V to V_{DD}		25	mA
I_{DD}	Supply current	through V_{SS}		200	mA
T_{STG}	Storage temperature		-65	+150	˚C
T_{JMAX}	Maximum junction temperature			+150	˚C
$R_{\theta JA}$	Transient thermal impedance from junction to ambient	QFN24		66	˚C/W
		TSSOP24		88	

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA, A2~A0, P1_7 to P0_0	0.7×V_{DD}	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA, A2~A0, P1_7 to P0_0	-0.5	0.3×V_{DD}	V
I_{OH}	HIGH-level output current	P1_7 to P0_0	-	10	mA
I_{OL}	LOW-level output current	P1_7 to P0_0	-	23	mA
T_A	Ambient temperature	Operating in free air	-40	+85	˚C

Electrical Characteristics

D.C. Characteristics

T_A = 25˚C;V_{DD} = 1.65V to 5.5V; (Unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IK}	Input clamping voltage	I_I = -18mA	-1.2	-	-	V
V_{POR}	Power-on reset voltage	V_I = V_{DD} or V_{SS}; I_O = 0mA	-		1.5	V
V_{OH}	HIGH-level output voltage	P port				
		I_{OH} = -8mA; V_{DD} = 1.65V	1.2	-	-	V
		I_{OH} = -10mA; V_{DD} = 1.65V	1.1	-	-	V
		I_{OH} = -8mA; V_{DD} = 2.3V	1.8	-	-	V
		I_{OH} = -10mA; V_{DD} = 2.3V	1.7	-	-	V
		I_{OH} = -8mA; V_{DD} = 3.0V	2.6	-	-	V
		I_{OH} = -10mA; V_{DD} = 3.0V	2.5	-	-	V
		I_{OH} = -8mA; V_{DD} = 4.5V	4.1	-	-	V
		I_{OH} = -10mA; V_{DD} = 4.5V	4.0	-	-	V
V_{OL}	LOW-level output voltage	P port; I_{OL} = 8 mA				
		V_{DD} = 1.65V	-	-	0.45	V
		V_{DD} = 2.3V	-	-	0.25	V
		V_{DD} = 3.0V	-	-	0.25	V
		V_{DD} = 4.5V	-	-	0.2	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V; V_{DD} = 1.65V to 5.5V				
		SDA	3	-	-	mA
		$\overline{INT}$	3	15	-	mA
		P port				
		V_{OL} = 0.5V; V_{DD} = 1.65V	8	10	-	mA
		V_{OL} = 0.7V; V_{DD} = 1.65V	10	13	-	mA
		V_{OL} = 0.5V; V_{DD} = 2.3V	8	10	-	mA
		V_{OL} = 0.7V; V_{DD} = 2.3V	10	13	-	mA
		V_{OL} = 0.5V; V_{DD} = 3.0V	8	14	-	mA
		V_{OL} = 0.7V; V_{DD} = 3.0V	10	19	-	mA
		V_{OL} = 0.5V; V_{DD} = 4.5V	8	17	-	mA
		V_{OL} = 0.7V; V_{DD} = 4.5V	10	24	-	mA
I_I	Input current	V_{DD} = 1.65V to 5.5V				
		SCL, SDA,A2~A0; V_I = V_{DD} or V_{SS}	-	-	±1	uA
I_{IH}	HIGH-level input current	P port; V_I = V_{DD}; V_{DD} = 1.65V to 5.5V	-	-	1	uA
I_{IL}	LOW-level input current	P port; V_I = V_{SS}; V_{DD} = 1.65V to 5.5V	-	-	1	uA

D.C. Characteristics (Continued)

T_A = 25°C;V_{DD} = 1.65V to 5.5V; (Unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	I_{DD}; SDA, P port, A2~A0; V_I on SDA = V_{DD} or V_{SS}; V_I on P port and A2~A0= V_{DD}; I_O = 0mA; I/O = inputs; f_{SCL} = 400kHz				
		V_{DD} = 3.6V to 5.5V	-	10	25	uA
		V_{DD} = 2.3V to 3.6V	-	6.5	15	uA
		V_{DD} = 1.65V to 2.3V	-	4	9	uA
		I_{DD}; SCL, SDA, P port, A2~A0; V_I on SCL, SDA = V_{DD} or V_{SS}; V_I on P port and A2~A0 = V_{DD}; I_O = 0mA; I/O = inputs; f_{SCL} = 0kHz				
		V_{DD} = 3.6V to 5.5V	-	1.5	7	uA
		V_{DD} = 2.3V to 3.6V	-	1	3.2	uA
		V_{DD} = 1.65V to 2.3V	-	0.5	1.7	uA
		Active mode; I_{DD}; P port, A2~A0; V_I on P port and A2~A0 = V_{DD}; I_O = 0mA; I/O = inputs; f_{SCL} = 400kHz, continuous register read				
		V_{DD} = 3.6V to 5.5V	-	60	125	uA
		V_{DD} = 2.3V to 3.6V	-	40	75	uA
		V_{DD} = 1.65V to 2.3V	-	20	45	uA
ΔI_{DD}	Additional quiescent supply current	SCL, SDA; one input at V_{DD} - 0.6V, other inputs at V_{DD} or V_{SS};	-	-	25	uA
		P port,A2~A0; one input at V_{DD} - 0.6V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65V to 5.5V	-	-	80	uA
C_I	Input capacitance	V_I = V_{DD} or V_{SS} ; V_{DD} = 1.65V to 5.5V	-	4.2	7	pF
C_{IO}	Input/output capacitance	V_{IO} = V_{DD} or V_{SS} ; V_{DD} = 1.65V to 5.5V	-	4.5	8	pF
		V_{IO} = V_{DD} or V_{SS} ; V_{DD} = 1.65V to 5.5V	-	4.5	8.5	pF

A.C. Characteristics

T_A = 25°C;V_{DD} = 1.65V to 5.5V; (Unless otherwise specified.)

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	KHz
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	us
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	us
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{SU;DAT}$	Data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	Data hold time		0	-	0	-	ns
t_r	Rise time of both SDA and SCL signals		-	1000	-	300	ns
t_f	Fall time of both SDA and SCL signals			300	-	300	ns
t_{BUF}	Bus free time between a STOP and START condition		4.7	-	1.3	-	us
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7	-	0.6	-	us
$t_{HD;STA}$	Hold time (repeated) START condition		4	-	0.6	-	us
$t_{SU;STO}$	Set-up time for STOP condition		4	-	0.6	-	us
$t_{VD;DAT}$	Data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	us
$t_{VD;ACK}$	Data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	us
t_{wrst}	Reset pulse width		30	-	30	-	ns
t_{recrst}	Reset recovery time		200	-	200	-	ns
t_{rst}	Reset time		600	-	600	-	ns
t_{vINT}	Valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	-	1	us
t_{rstINT}	Reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	1	-	1	us
t_{vQ}	Data output valid time	from SCL to P port	-	400	-	400	ns
t_{suD}	Data input set-up time	from P port to SCL	0	-	0	-	ns
t_{hD}	Data input hold time	from P port to SCL	300	-	300	-	ns

Load Configuration

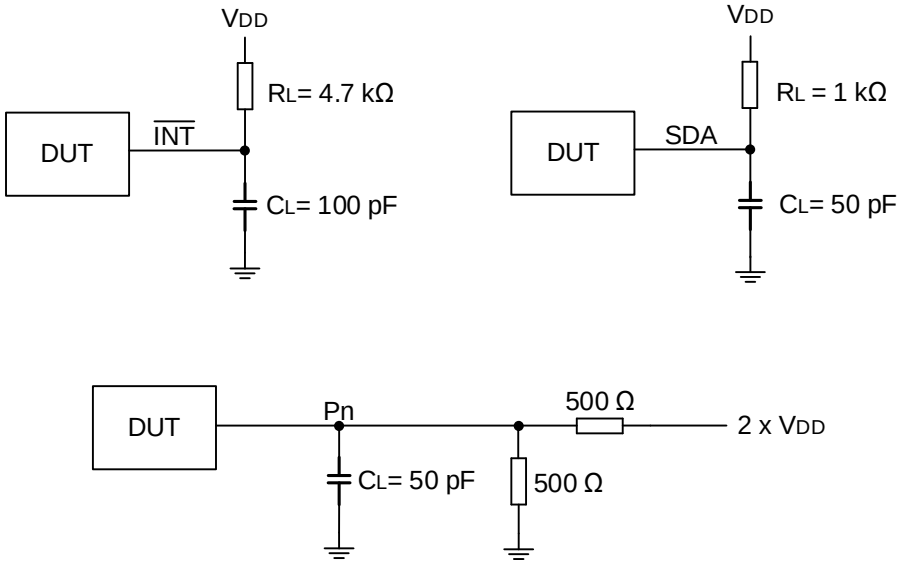


Figure 7. $\overline{INT}$、SDA、Port P Load Configuration

Note: C_L includes probe and clamp capacitance.

I²C Timing Waveform

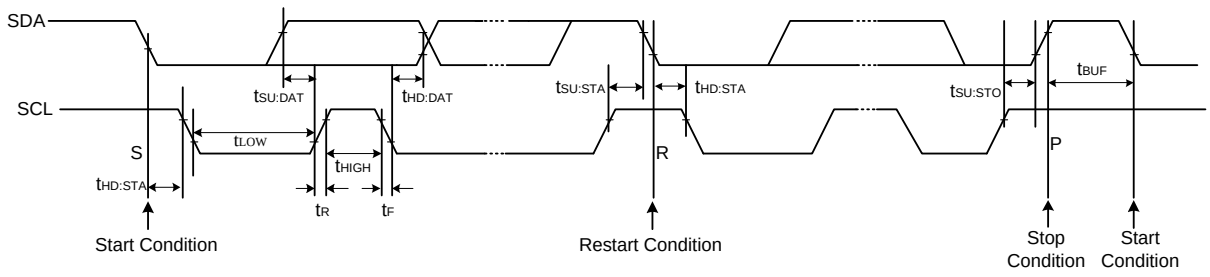


Figure 8. SDA Waveform

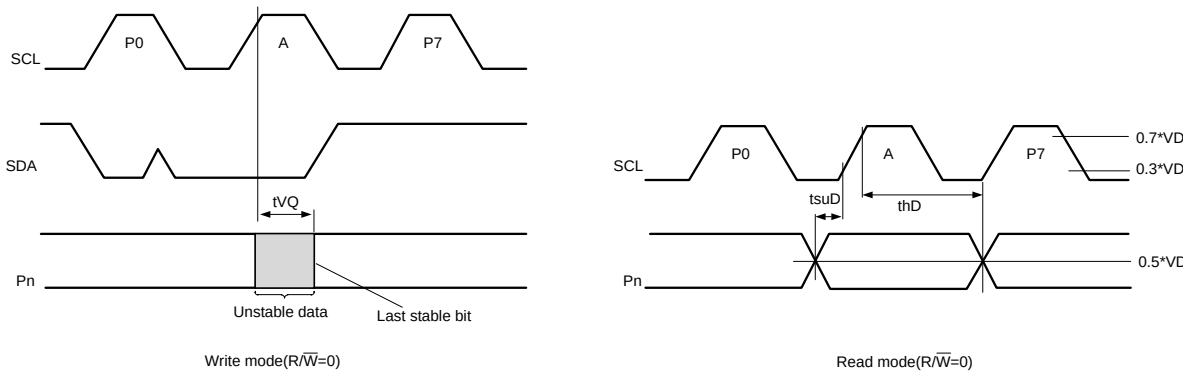


Figure 9. SDA Read/Write Mode Waveform

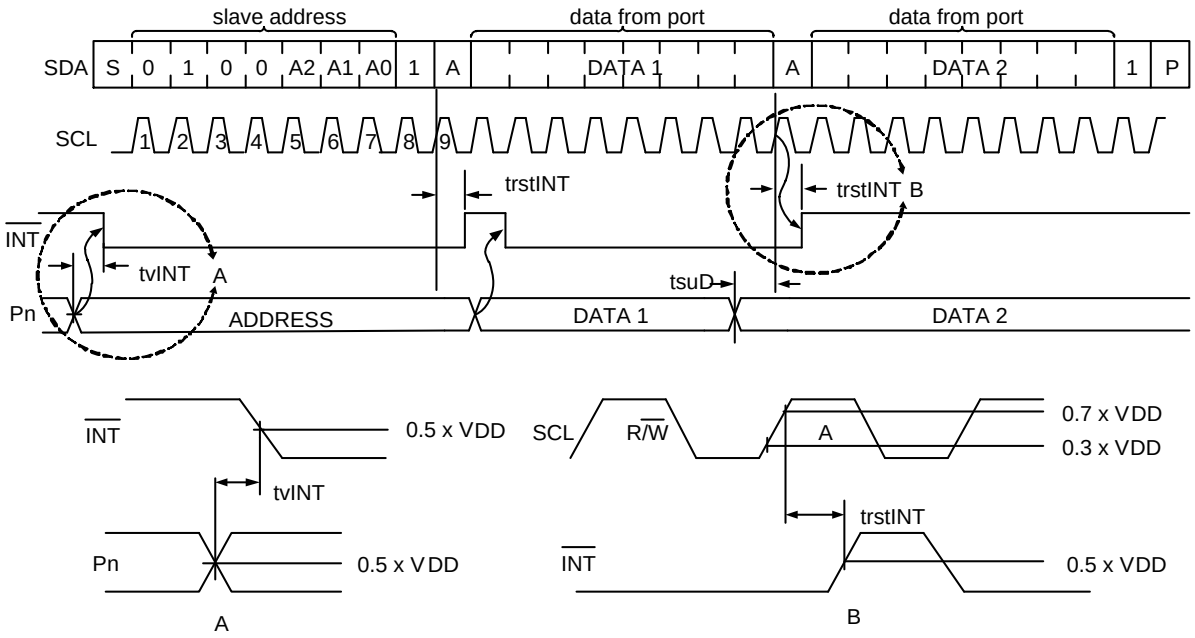


Figure 10. $\overline{INT}$、SDA、Port P waveform

Application Circuits

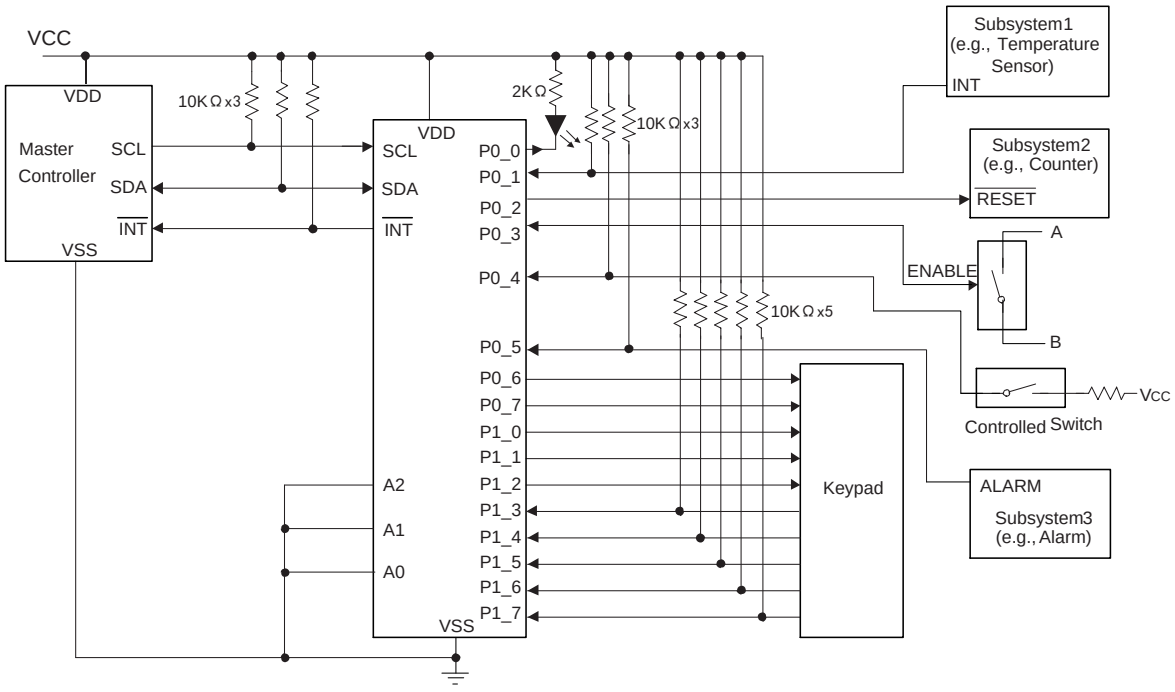


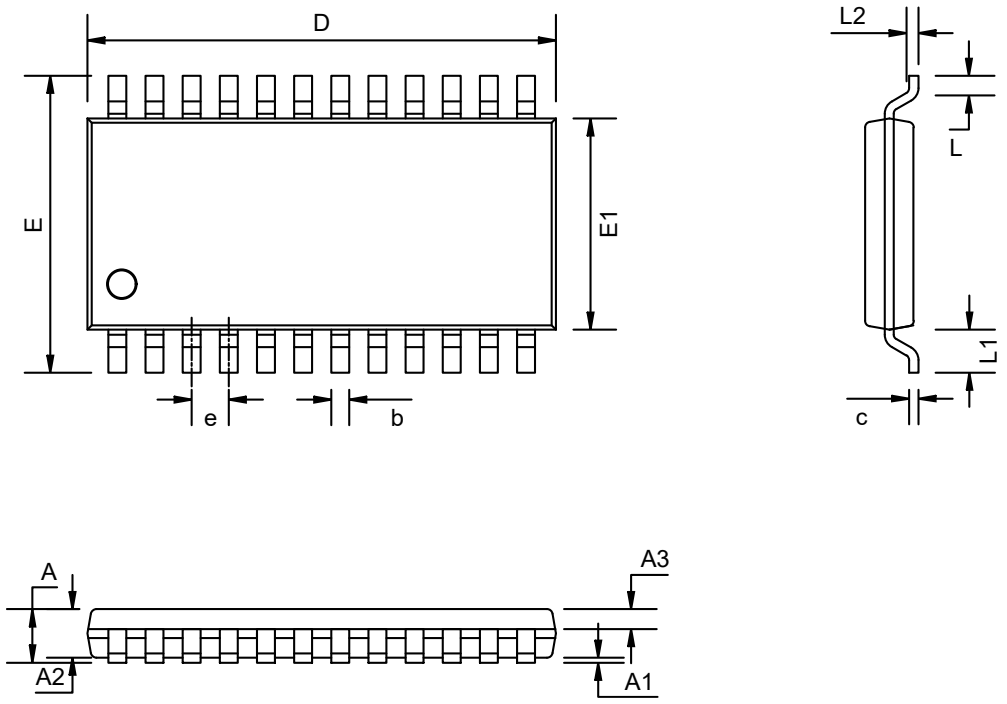
Figure 11. Application circuit

Notes： This application circuits is for reference only.

When the P port is suspended, configure it to the output state please.

Package

TSSOP24

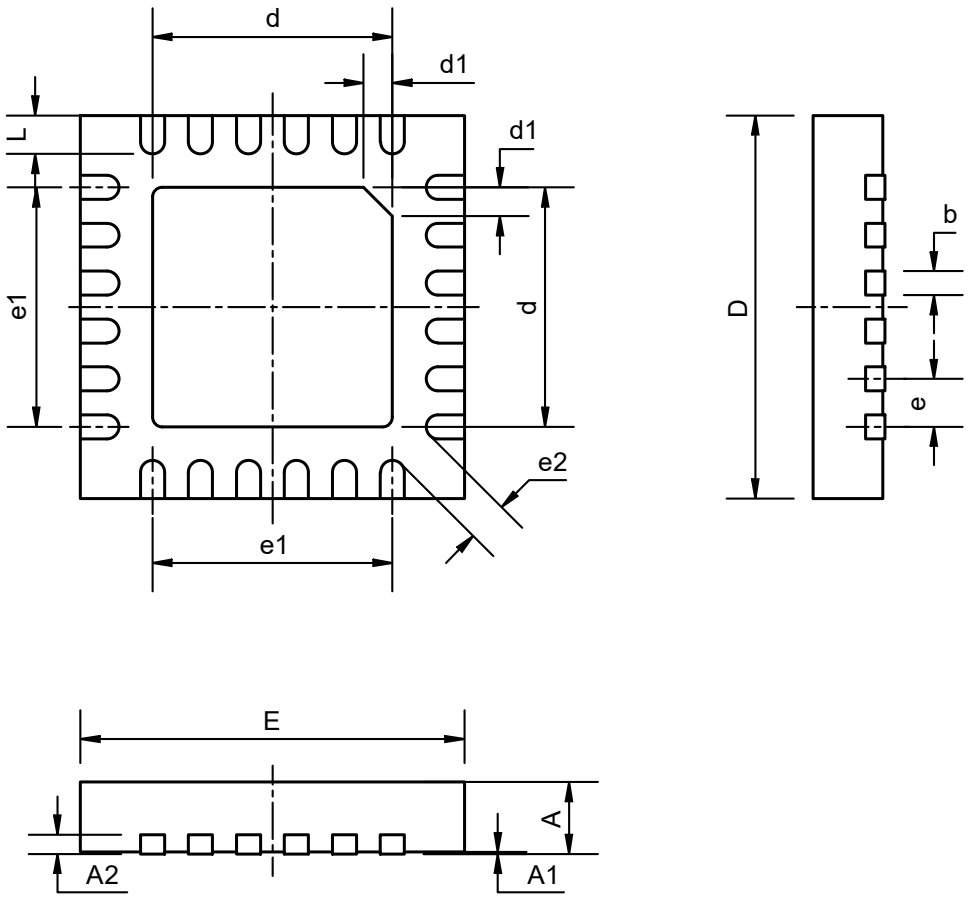


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	0.90	1.00
A3	0.34	0.39	0.44
b	0.20	-	0.29
c	0.10	-	0.19
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
L2	0.25BSC		

QFN24



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.18	0.20	0.25
b	0.18	0.25	0.30
D	3.90	4.00	4.10
d	2.40	2.60	2.80
d1	0.30	0.35	0.40
E	3.90	4.00	4.10
e		0.50	
e1	2.40	2.60	2.80
e2	0.40	0.45	0.50
L	0.35	0.40	0.45

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2022-04-29	Preliminary Version	Shilj	Shilj	Liujy
1.0	2022-05-11	Released Version	Shib	Shilj	Liujy
1.1	2022-05-27	Released Version	Shilj	Shilj	Liujy
1.2	2022-07-24	Typeset Version	Shib	Shilj	Liujy
1.3	2023-6-4	Pen error update	Shib	Shilj	Liujy
1.4	2024-1-26	Update picture	Shib	Shib	Liujy