SD3.0-SDR104 Compliant Integrated Auto-direction Control Memory Card Voltage Level Translator

General Description

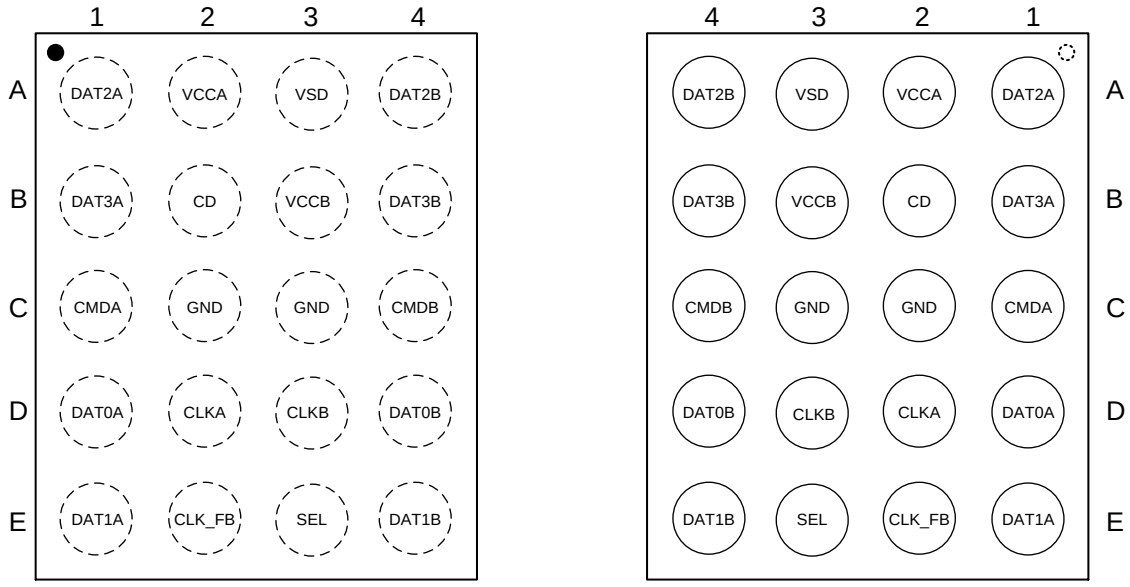
The ET4857 is a SD 3.0-compliant bidirectional dual voltage level translator with auto-direction control. It is designed to interface between a memory card operating at 1.8V or 3.0V signal levels and a host with a nominal supply voltage of 1.2V to 1.8V. The IC supports SD3.0 SDR104、SDR50、DDR50、SDR25、SDR12 and SD2.0 High-Speed (50MHz) and Default-Speed (25MHz) modes. The device has an integrated voltage select-able low dropout regulator to supply the card-side I/Os, an auto-enable/disable function connected to the VSD supply pin.

Features

- Supports up to 208MHz clock rate
- SD3.0 specification-compliant voltage translation to support SDR104, SDR50, DDR50, SDR25, SDR12, High-Speed and Default-Speed modes
- 1.2V to 1.8V host side interface voltage support
- Feedback channel for clock synchronization
- 100mA Low dropout voltage regulator to supply the card-side I/Os
- Low power consumption by push-pull output stage with break-before-make architecture
- Automatic enable and disable through V_{SD}
- Integrated pull-up and pull-down resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Integrated 8kV ESD protection according to IEC 61000-4-2, level 4 on card side
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- Package information:

Part No.	Package	MSL
ET4857	WLCSP20 (0.4pitch)	1

Pin Configuration



TOP VIEW BOTTOM VIEW

Pin Function

Pin No.	Pin Name	Pin Function
A1	DAT2A	Data 2 input or output on host side
A2	VCCA	Supply Voltage from host side
A3	VSD	Supply Voltage
A4	DAT2B	Data 2 input or output on memory card side
B1	DAT3A	Data 2 input or output on host side
B2	CD	Card detect switch basing output
B3	VCCB	Internal supply decoupling(V_{LDO})
B4	DAT3B	Data 3 input or output on memory card side
C1	CMDA	Command input or output on host side
C2	GND	Supply Ground
C3	GND	Supply Ground
C4	CMDB	Command input or output on memory card side
D1	DAT0A	Data 0 input or output on host side
D2	CLKA	Clock signal input on host side
D3	CLKB	Clock signal output on memory card side
D4	DAT0B	Data 0 input or output on memory card side
E1	DAT1A	Data 1 input or output on host side
E2	CLK_FB	Clock feedback output on host side
E3	SEL	Card side I/O voltage level select
E4	DAT1B	Data 1 input or output on memory card side

SD Card side voltage level control signal truth table

INPUT	OUTPUT		
SEL	**V_{CCB}**	**Pin**	**Pin Function**
H	1.8V	DATA0B to DATA3B, CLKB	Low supply voltage level (1.8V typ)
L	Tracking V_{SD}	DATA0B to DATA3B, CLKB	High supply voltage level (tracking V_{SD})

Note:

If the OE pin is driven LOW, the ET4857 is disabled and the A0, A1, B0, and B1 pins (including dynamic drivers) are forced into 3-state and all four 10KΩ internal pull-up resisters are decoupled from their respective V_{CC}.

Block Diagram

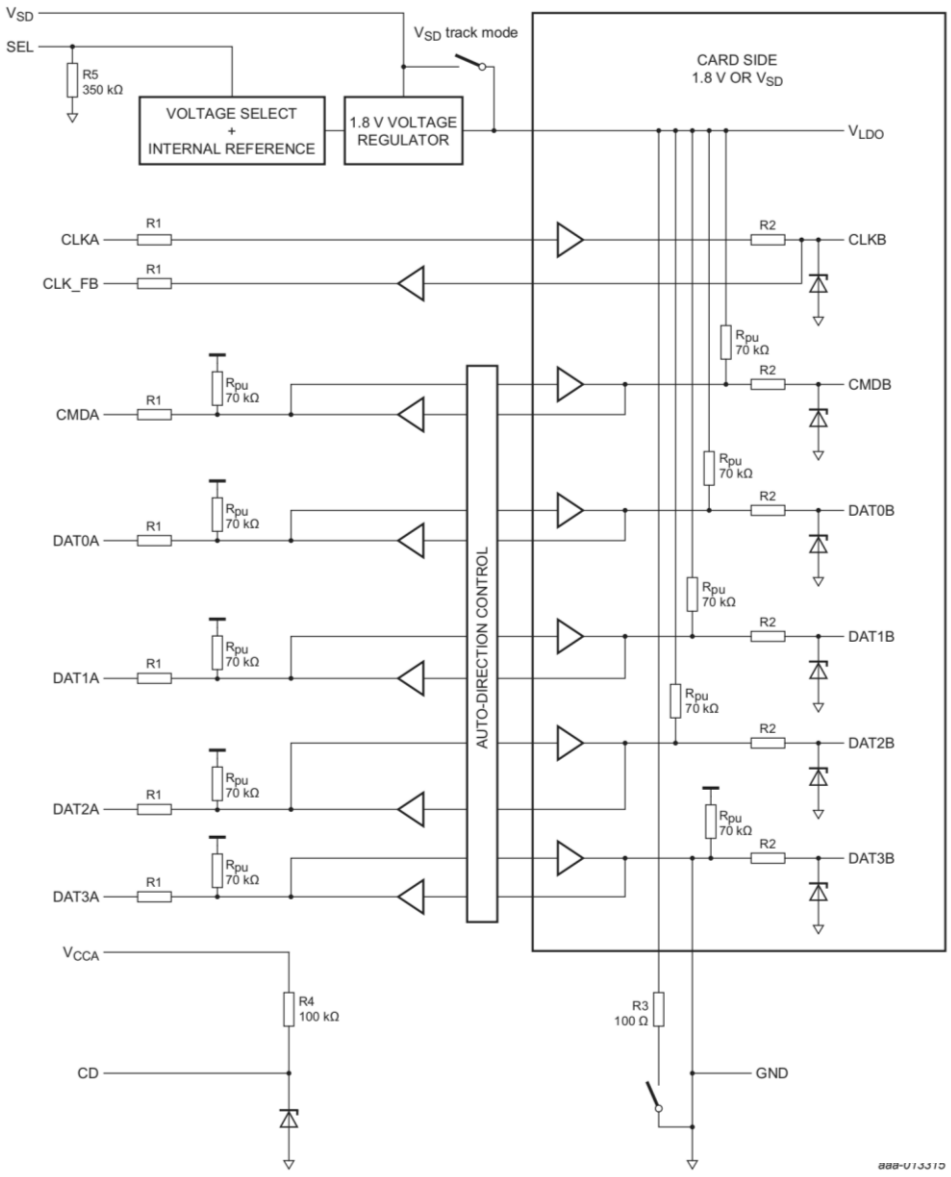


Figure1. Block Diagram

Functional Description

Level Translate

The bidirectional level translator shifts the data between the I/O supply levels of the host and the memory card. The voltage translator has to support several clock and data transfer rates at the signaling levels specified in the SD 3.0 standard specification.

Enable and direction control

ET4857 contains an auto-enable feature. If V_{SD} rises above 2.65V, the LDO and the level translator logic is enabled automatically. As soon as V_{SD} drops below the V_{SD} disable (typ 2.45V), the LDO and the card side drivers and the level translator logic is disabled. All host side pins excluding CLKA 1 are configured as inputs with a 70k resistor pulled up to V_{CCA}.

Integrated voltage regulator

The low dropout voltage regulator delivers supply voltage for the voltage translators and the card-side input/output stages. It has to support 1.8V and 3V signaling modes as stipulated in the SD3.0 specification. The switching time between the two output voltage modes is compliant with SD3.0 specification. Depending on the signaling level at pin SEL, the regulator delivers 1.8V (SEL = high) or 3.0V (SEL = low).

Supported Modes table+

Bus Speed Mode	Signal Level (V)	Clock Rate (MHz)	Data Rate (MB/s)
Default Speed	3.3	25	12.5
High-Speed	3.3	50	25
SDR12	1.8	25	12.5
SDR25	1.8	50	25
SDR50	1.8	100	50
SDR104	1.8	208	104
DDR50	1.8	50	50

An external capacitor (typ 2.2μF) is needed between the regulator output pin V_{CCB} and ground for proper operation of the integrated voltage regulator. It is recommended to place the capacitor close to the V_{SD} and V_{CCB} pin and maintain short connections of both to ground.

Feedback clock channel

The clock is transmitted from the host to the memory card side. The voltage translator and the Printed-Circuit Board (PCB) tracks introduce some amount of delay. It reduces timing margin for data read back from memory card, especially at higher data rates. Therefore, a feedback path is provided to compensate the delay. The reasoning behind this approach is the fact that the clock is always delivered by the host, while the data in the timing critical read mode comes from the card.

EMI filter

ET4857's all input/output ports are equipped with EMI filters to reduce interferences towards sensitive mobile-communication.

ESD protection

ET4857 has robust ESD protections on all memory card pins as well as on the VSD pin. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground. Pin Card Detection (CD) might be pulled down by the memory card which has to be detected by the host. The pin is equipped with International Electrotechnical Commission (IEC) system-level ESD protection and pull-up resistor connected to the host supply V_{CCA}.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters		Condition	Rating	Unit
V_{CC}	Supply Voltage		VSD pins (4ms transient)	-0.5 ~ 4.6	V
			VCCA pins (4ms transient)	-0.5 ~ 4.6	
V_{IN}	Input Voltage		I/O pins (4ms transient)	V_{SS}-0.3 ~ V_{DD}+0.3	V
P_D	Power Dissipation		T_A = 25°C	2000	mW
T_J	Junction Temperature Range		-	-40 ~ +150	°C
T_{STG}	Storage Temperature Range		-	-65 ~ +150	°C
V_{ESD}(1)	(IEC 61000-4-2)	Contact discharge	All memory card side pins, VSD and CD pins to ground	±8	kV
		Air discharge		±15	
	HBM (JESD22-A114)		All Pins	±2	
	CDM (JESD22-C101)		All Pins	±0.5	
I_{LU}	Max Latch-up Current (JESD78B)		I/O port : -0.5V_{CC} < V_I <1.5V_{CC}	±100	mA

Note(1): ESD test, All system level tests are performed with the application-specific capacitors connected to the supply pins V_{SUPPLY}, V_{LDO} and V_{CCA}.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. We does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameters	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	V_{SD}	2.9(2)	-	3.6	V
		V_{CCA}	1.1	-	2.0	
V_{IN}	Input Voltage	Host side	-0.3(3)	-	V_{CCA}+0.3	V
		Memory card side	-0.3	-	V_{LDO}+0.3	
C_{EXT}	Recommended External Capacitance	Capacitor connect to V_{CCB}		2.2		µF
		Capacitor connect to V_{SD}		0.1		µF
		Capacitor connect to V_{CCA}		0.1		µF
ESR	Equivalent series resistance	At pin V_{LDO}	0	-	50	mΩ
T_A	Operate Temperature Range		-40		+85	°C

Note(2): By minimum value the device is still fully functional, but the voltage on pin V_{LDO} might drop below the recommended memory card supply voltage.

Note(3): The voltage must not exceed 3.6V.

Integrated Resistors in Block Diagram (T_A=25°C)

Symbol	Parameters	Condition	Min	Typ	Max	Unit
R_{PD}	Pull-down Resistance	R3 , tolerance±30%	70	100	130	Ω
		R5	200	350	500	KΩ
R_{PU}	Pull-up Resistance	All data lines and CMDx	49	70	91	KΩ
		R4	70	100	130	KΩ
R_S	Series Resistance	Host side, R1, tolerance ±30%	-(4)	22.5		Ω
		Card side, R2, tolerance ±30%	-(4)	15		Ω

Note(4): Guaranteed by design.

Electrical Characteristics

Recommended operating conditions: T_A= -40 ~ 85°C

Symbol	Parameter	Conditions	Min	Typ(5)	Max	Unit
Automatic enable feature:V_{SD}						
V_{SD_EN}	IC enable voltage	V_{CCA}≥1V, V_{SD} rising edge	2.25	2.45	2.65	V
V_{SD_DIS}	IC disable voltage	V_{CCA}≥1V, V_{SD} falling edge	2.2	2.4	2.6	V
ΔV_{SD_EN}	V_{SD_EN} hysteresis voltage		-	50		mV
Supply voltage regulator for card-side I/O Pin: V_{CCB}						
$V_{O(LDO)}$	Regulator/switch output voltage	SEL=Low, 3V≤ V_{SD} ≤3.6V, I_O<100mA	V_{SD}-0.2	V_{SD}-0.1	V_{SD}	V
		SEL=High;V_{SD} ≥ 2.9V, I_O<100mA	1.7	1.8	1.95	V
$I_{O(LDO)}$	Regulator/switch output current		-	-	100	mA
Host-side input signals:CMDA and DAT0A to DAT3A,CLKA;host-side control singnal;1.1V≤V_{CCA}≤2.0V						
V_{IH}	Input voltage high level		0.75×V_{CCA}	-	V_{CCA}+0.3	V
V_{IL}	Input voltage low level		-0.3	-	0.25×V_{CCA}	V
Host-side output signals: CLK_FB, CMDA, DATA0A to DATA3A; 1.1V≤V_{CCA}≤2.0V						
V_{OH}	Output voltage high level for CLK_FB	I_O=2mA, V_I=V_{IH}(card side)	0.8×V_{CCA}	-	-	V
	Output voltage high level for CMDA, DATxA	I_O=2μA, V_I=V_{IH}(card side)	0.8×V_{CCA}	-	-	V
V_{OL}	Output voltage low level	I_O=-2mA, V_I=V_{IL}(card side)	-	-	0.15×V_{CCA}	V

Electrical Characteristics (Continued)

Recommended operating conditions: T_A= -40 ~ 85°C

Symbol	Parameter	Conditions	Min	Typ[5]	Max	Unit
Card-side input singals: CMDB and DAT0B to DAT3B						
V_{IH}	Input voltage high level	SEL=Low (3.0V card interface)	0.625× $V_{O(LDO)}$	-	$V_{O(LDO)}$ +0.3	V
		SEL=High (1.8V card interface)	0.625× $V_{O(LDO)}$	-	$V_{O(LDO)}$ +0.3	V
V_{IL}	Input voltage low level	SEL=Low (3.0V card interface)	-0.3	-	0.3× $V_{O(LDO)}$	V
		SEL=High (1.8V card interface)	-0.3	-	0.3× $V_{O(LDO)}$	V
Card-side output signal (CMDB and DAT0B to DAT3B,CLKB)						
V_{OH}	Output voltage high level for CLKB only	I_O=4mA, V_I=V_{IH}(host side); SEL=Low(3.0V card interface)	0.85× $V_{O(LDO)}$	-	$V_{O(LDO)}$ +0.3	V
		I_O=2mA, V_I=V_{IH}(host side); SEL=High(1.8V card interface)	0.85× $V_{O(LDO)}$	-	2.0	V
	Output voltage high level for CMDB,DATxB	I_O=2μA, V_I=V_{IH}(host side); SEL=High(1.8V card interface)	0.85× $V_{O(LDO)}$	-	2.0	V
V_{OL}	Output voltage low level	I_O= -4mA, V_I=V_{IL}(host side); SEL=Low(2.9 V card interface)	-0.3	-	0.125× $V_{O(LDO)}$	V
		I_O= -2mA, V_I=$V_{I\ card\ L}$(host side); SEL= High(1.8V card interface)	-0.3	-	0.125× $V_{O(LDO)}$	V
Bus signal equivalent capacitance						
C_{ch}	Channel capacitance (V_I=0 V, f_i=1MHz, V_{SD}=3 V, V_{CCA}=1.8 V)	Host side	-[6]	7	-	pF
		Card side	-	15	-	pF
Current consumption						
$I_{CC(start)}$	Static supply current (V_{SD} ≥ V_{SD_EN} (active mode); all input = high)	SEL=Low (3.0V card interface)	-	-	100	μA
		SEL=High (1.8 V card interface)	-	-	100	μA
$I_{CC(stb)}$	Standby supply current	V_{SD} ≤ V_{SD_EN} and V_{CCA} ≥ 1.0V (inactive mode), All host side input = High	-	-	7	μA

Note(5): Typical values are measured at T_A = 25°C.

Note(6): EMI filter line capacitance per data channel from I/O driver to pin; C_{ch} is guaranteed by design.

Voltage Regular (T_A=25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage regulator output Pin: V_{CCB}						
$t_{startup(LDO)}$	Regulator start-up time	V_{CCA}=1.8V; V_{SD}=3.0V, C_{EXT}=2.2μF (Figure3.)	-	-	400	μs
$t_{f(O)}$	Output fall time	$V_{O(LDO)}$=3.0V to 1.8V, SEL = Low to High (Figure2.)			1	ms
$t_{f(O)}$	Output rise time	$V_{O(LDO)}$=3.0V to 1.8V, SEL = High to Low (Figure2.)			100	μs

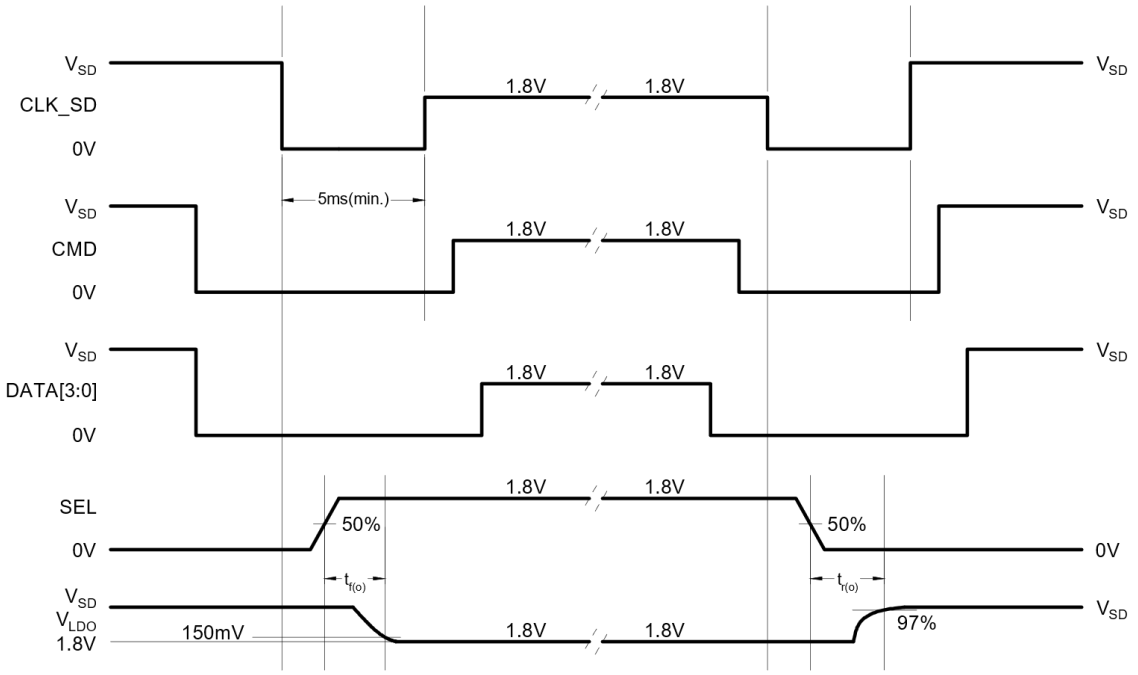


Figure2. Regulator mode change timing

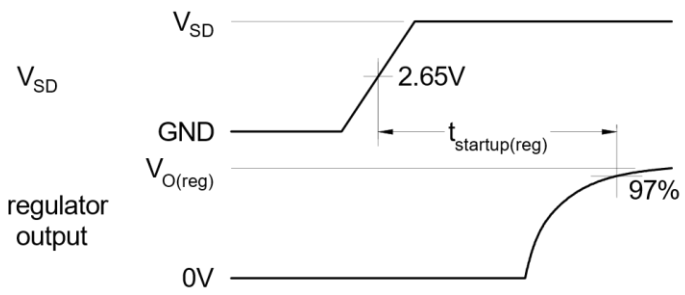


Figure3. Regulator start-up time

Test point: V_{SD} signal is at 2.65V, and regulate output signal at 0.97×$V_{O(LDO)}$

Level Translator(T_A=25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Host side transition times[7]						
t_r	Rise time	SEL=High(1.8V card interface); V_{CCA}=1.8V	-	0.4	1.0	ns
t_f	Fall time		-	0.4	1.0	ns
t_r	Rise time	SEL=High(1.8V card interface); V_{CCA}=1.2V	-	0.4	1.0	ns
t_f	Fall time		-	0.4	1.0	ns
Card side transition times[8]						
t_r	Rise time	SEL=High(1.8V card interface); -40°C ≤T_A≤ 85°C	0.4	0.88	1.32	ns
t_f	Fall time		0.4	0.88	1.32	ns
Card input transition times[9]						
t_r	Rise time	SEL=High(1.8V card interface); -40°C ≤T_A≤ 85°C	0.2	0.5	0.96	ns
t_f	Fall time		0.2	0.45	0.96	ns
Host to card propagation delay						
DATAxA to DATAxB, CMDA to CMDB, CLKA to CLKB						
t_{pd}	Propagation delay	SEL=High(1.8V card interface); V_{CCA}=1.2V	-	3.0	5.5	ns
CLKA to CLK_FB						
t_{pd}	Propagation delay	SEL=High(1.8V card interface); V_{CCA}=1.2V	-	5.5	10.0	ns
Card to host propagation delay						
DATxB to DATxA, CMDB to CMDA						
t_{pd}	Propagation delay	SEL=High(1.8V card interface); V_{CCA}=1.2V	-	2.5	4.5	ns

Note(7): Transition between V_{OL}=0.35×V_{CCA} and V_{OH}=0.65×V_{CCA}.

Note(8): Transition between V_{OL}=0.45V and V_{OH}=1.4V.

Note(9): Guaranteed by design; transition between V_{IL}=0.58V and V_{IH}=1.27V with C_{trace}=3.5pF and C_{card}+C_{RADLE} =12pF, trace length=11mm.

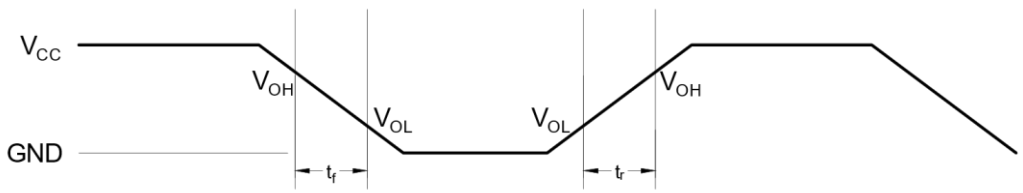


Figure4. Output rise and fall times

Test point: V_{OH} and V_{OL} are specified as ***Note(7)*** and ***Note(8)***

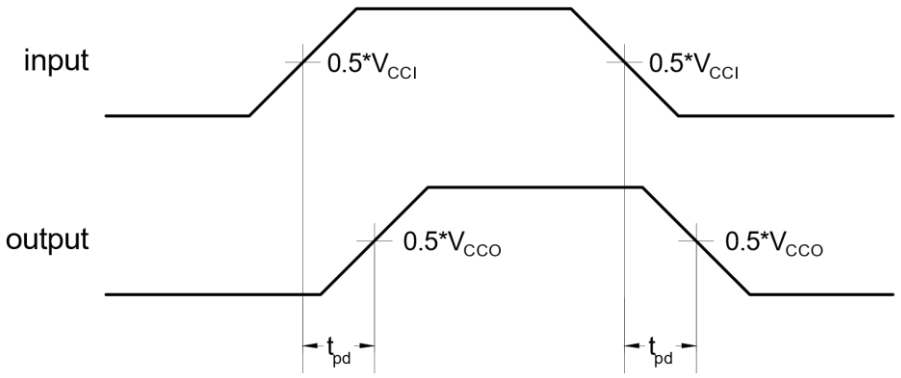


Figure5. Output delay timing

Test point: Output delay is for every single channel, from input to output, 0.5×V_{CCI} to 0.5×V_{CCO}, in which V_{CCI} and V_{CCO} are the input and output voltage domain.

Test Information

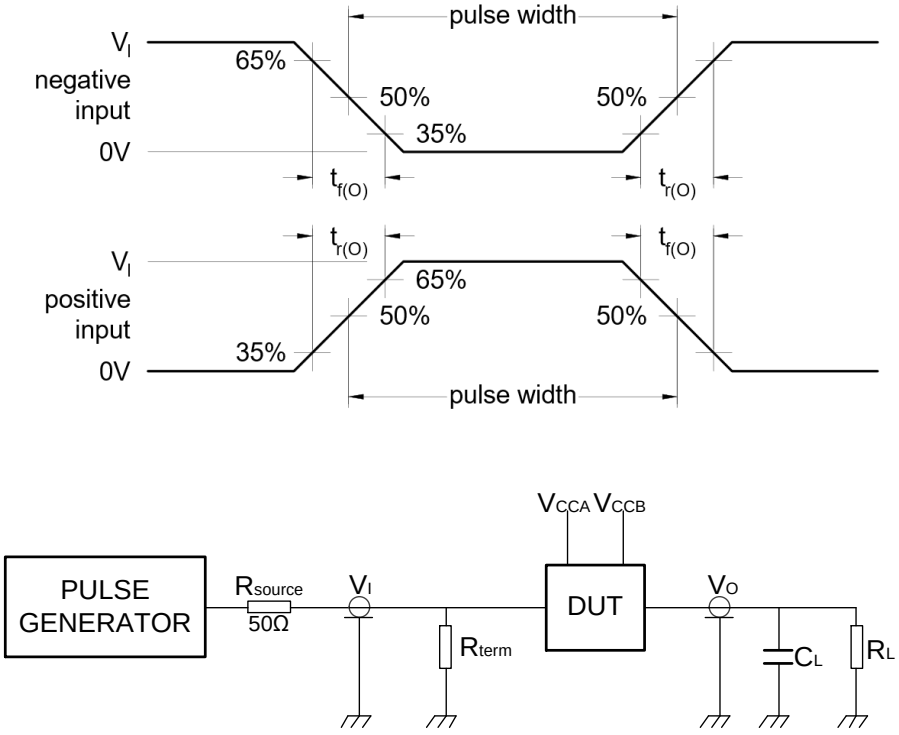


Figure6. Load circuitry for measuring switching time

Definitions test circuit:

R_{source} = source resistance of pulse generator.

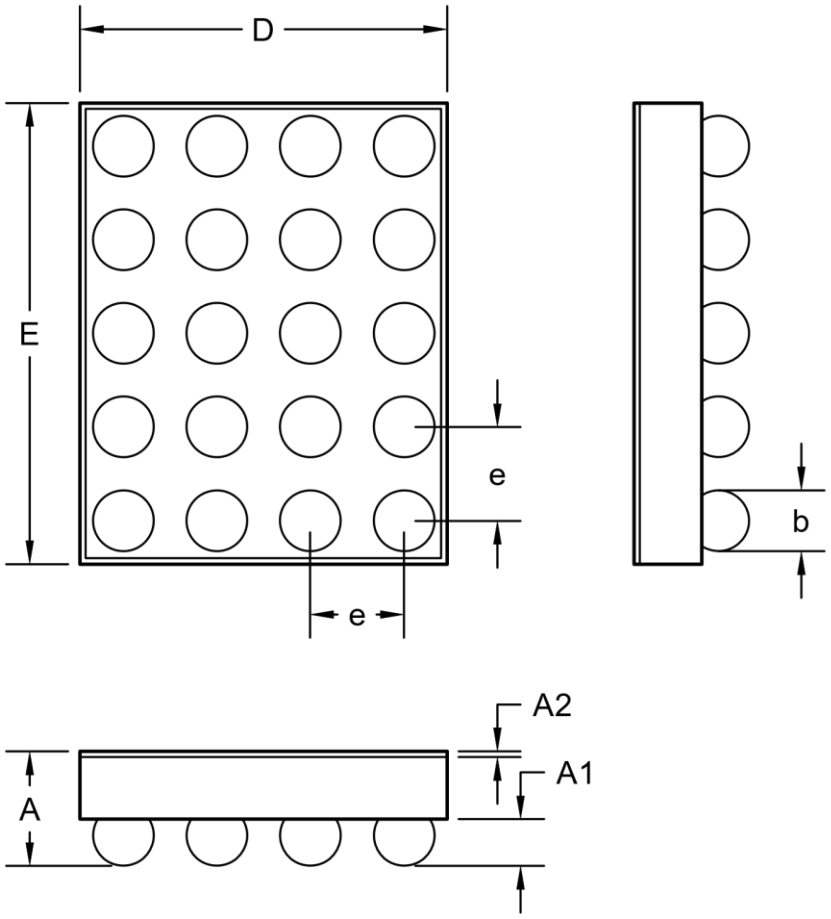
R_{term} = termination resistance should be equal to output impedance Zo of pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

Package Dimension

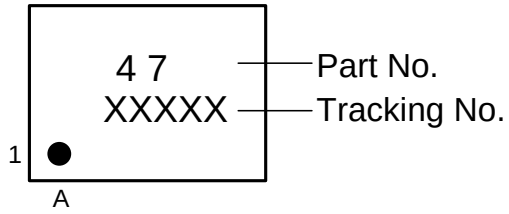
WLCSP20



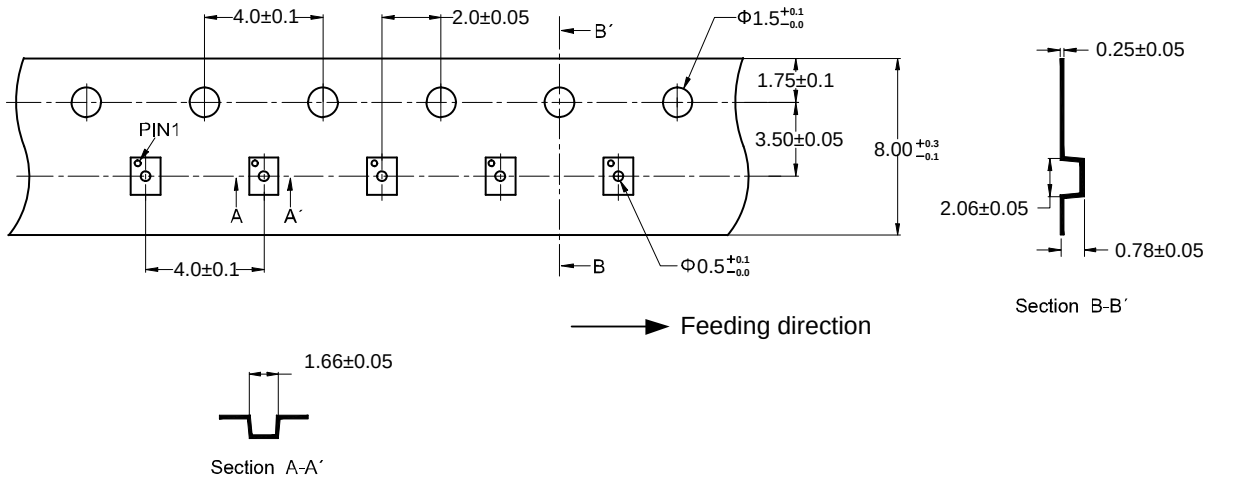
Dimensions Table (Units:mm)

SYMBOL	MIN	NOM	MAX
A	0.46	0.49	0.52
A1	0.18	0.20	0.22
A2	0.025 TYP		
b	0.24	0.26	0.28
D	1.55	1.57	1.59
E	1.95	1.97	1.99
e	0.40 BSC		

Marking



Tape Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2022.8.11	Preliminary Version	LiuCong	Shi Bo	Shi Bo
0.1	2023.11.29	Update Pin picture	Shibo	Luh	Liujy
1.0	2024.12.25	Offered Version	Shibo	Luh	Liujy