ET4559 - SIM Card Interface Level Translator With EMI Filter and ESD Protection

General Description

The ET4559 device is built for interfacing a SIM card with a single low-voltage 1.08V to 1.98V host side interface. The ET4559 contains three 1.62V to 3.6V level translators to convert the data, RST and CLK signals between a SIM card and a host micro controller.
The ET4559 is compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements.

Features

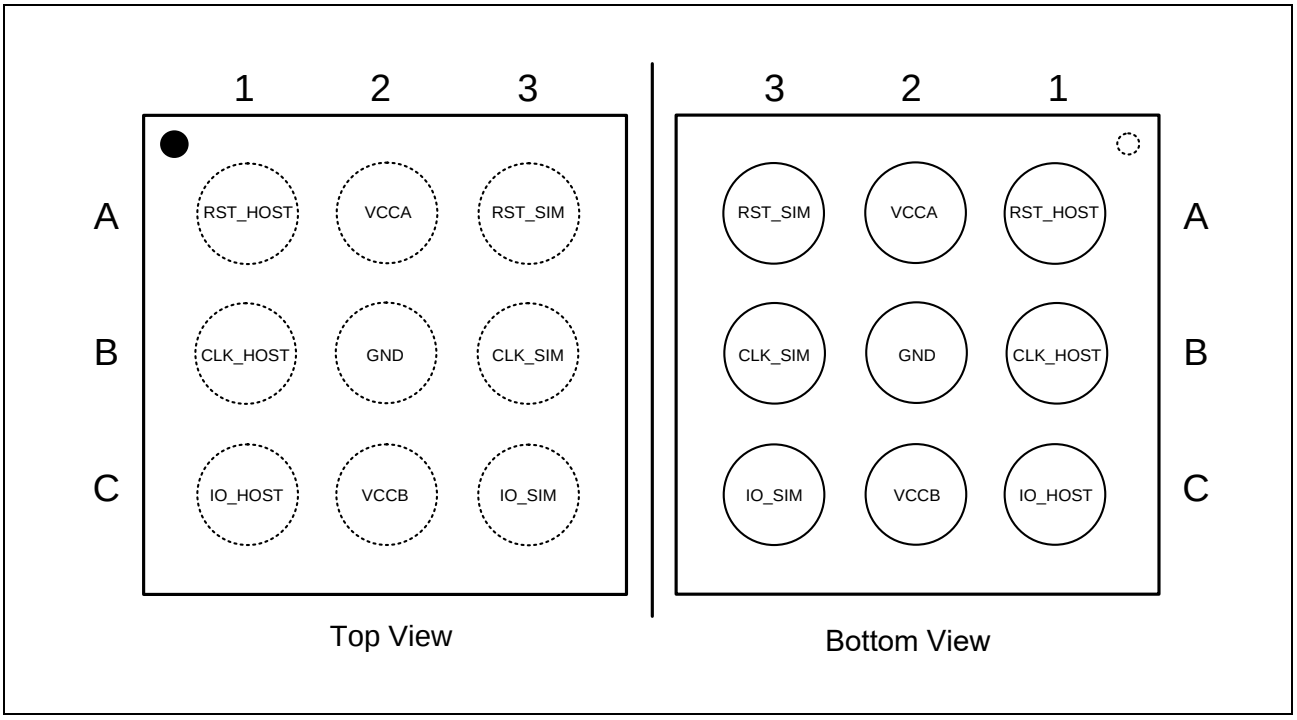
- Supports clock speed up to 10MHz clock
- Compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements
- Support SIM card supply voltages with range of 1.62V to 3.6V
- Host micro controller operating voltage range: 1.08V to 1.98V
- Automatic level translation of I/O, RST and CLK between SIM card and host side interface with capacitance isolation
- Incorporates shutdown feature for the SIM card signals according to ISO-7816-3
- Automatic enable and disable through VCCB
- Integrated pull-up and pull-down resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Integrated 8kV ESD protection according to IEC 61000-4-2, level 4 on all SIM card contact pins
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Part No. and Package

Part No.	Package	MSL
ET4559	FOWLP9 (1.06 mm × 1.06 mm × 0.43 mm; 0.35 mm pitch)	Level 1

Applications

- Mobile and personal phones
- Wireless modems
- SIM card terminals

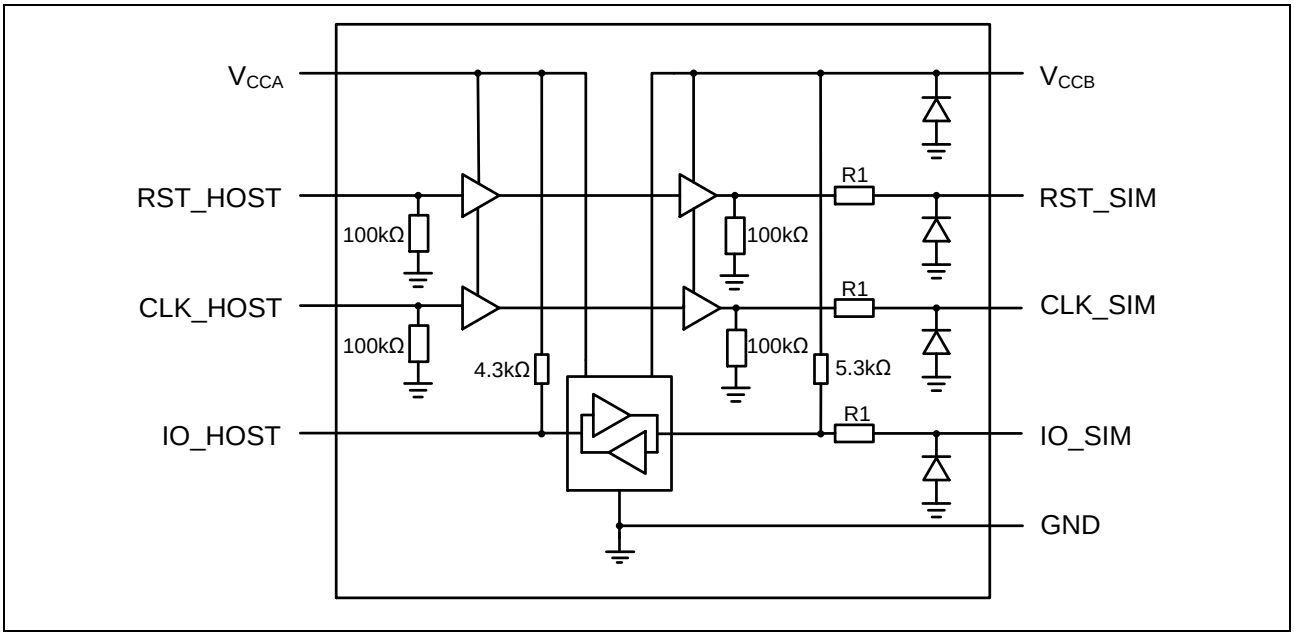
Pin Configuration



Pin Function

Pin	Pin No.	Type	Description
RST_HOST	A1	I	Reset input from host controller.
V_{CCA}	A2	Supply	Supply voltage for the host controller side input/output pins (CLK_HOST, RST_HOST, IO_HOST). This pin should be bypassed with a 1μF ceramic capacitor close to the pin.
RST_SIM	A3	O	Reset output pin for the SIM card.
CLK_HOST	B1	I	Clock input from host controller.
GND	B2	Ground	Ground for the SIM card and host controller. Proper grounding and bypassing are required to meet ESD specifications.
CLK_SIM	B3	O	Clock output pin for the SIM card.
IO_HOST	C1	I/O	Host controller bidirectional data input/output. The host output must be on an open-drain driver.
V_{CCB}	C2	Supply	SIM card supply voltage. When V_{CCB} is below the V_{CCB} disable, the device is disabled. This pin should be bypassed with a 1μF ceramic capacitor close to the pin.
IO_SIM	C3	I/O	SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver.

Block Diagram



Operation

The ISO 7816-3 specification specifies the shutdown sequence for the SIM card signals to ensure that the card is properly disabled for power savings. Also during hot swap, the orderly shutdown of these signals helps to avoid any improper write and corruption of data.

When the V_{CCB} disable, V_{CCB_DIS}, the shutdown sequence is initiated by powering down the RST_SIM channel. Once the RST_SIM channel is powered down, CLK_SIM and IO_SIM are powered down sequentially one-by-one. An internal pull-down resistor on the SIM pins is used to pull these channels LOW. The shutdown sequence is completed in a few microseconds.

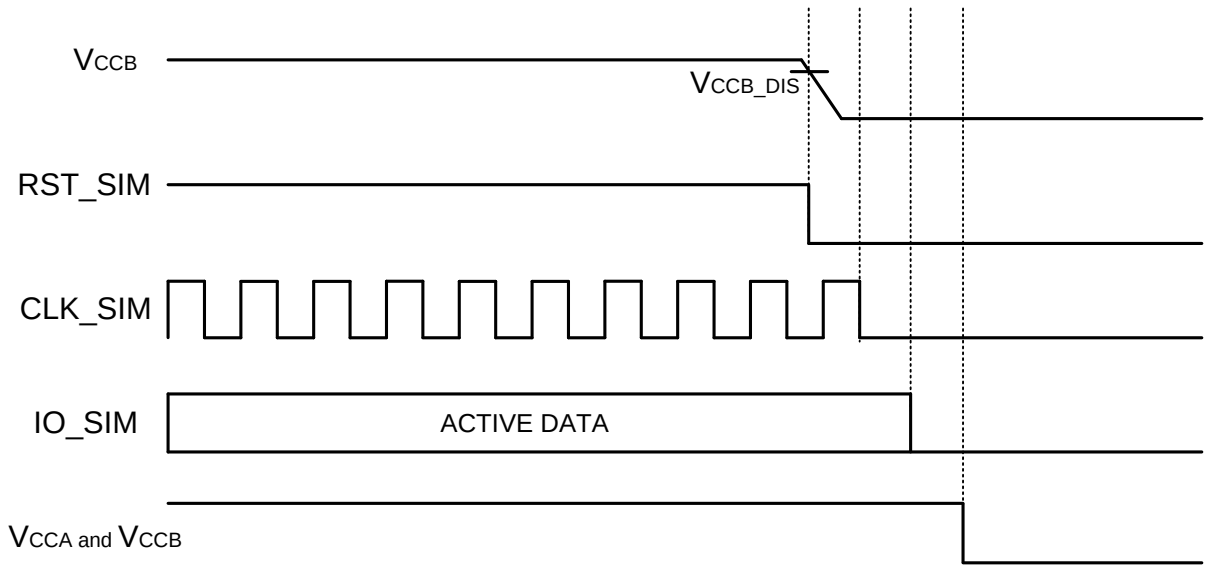


Figure1.Shutdown sequence for RST_SIM, CLK_SIM, IO_SIM and V_{CCA}/V_{CCB} of SIM card translator

VCCB enable

The device contains an auto-enable feature. If V_{CCB} rises above V_{CCB_EN}, the level translator logic is enabled automatically. As soon as V_{CCB} drops below the V_{CCB_DIS}, the SIM card side drivers and the level translator logic is disabled. Host side IO pin is configured as input with a 4.3kΩ resistor pulled up to V_{CCA}.

When the V_{CCB} drops below V_{CCB} disable voltage but is still higher than a MOS threshold (e.g. 0.8V) the pull-down NMOS in the one-directional drive will be off and NMOS controlled by CTL will be on, and the 400Ω resistor will keep the card side CLK/RST/IO low. Additionally the CLK/RST pins on both the Host and Card side have a 400Ω pull down resistor. The 400Ω resistor is used for discharge at power off and the 100kΩ resister is used for keep RST_SIM/CLK_SIM low when V_{CCB} below V_{TH}.

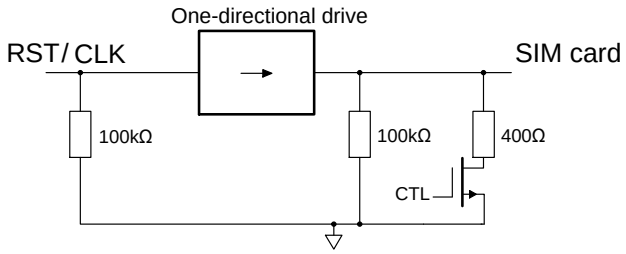


Figure 2.RST/CLK voltage level translation architecture

When V_{CCB_EN} = 0 then CTL = V_{CCB} and line is high-Z.
When V_{CCB_EN} = 1 then CTL = GND and line is active.

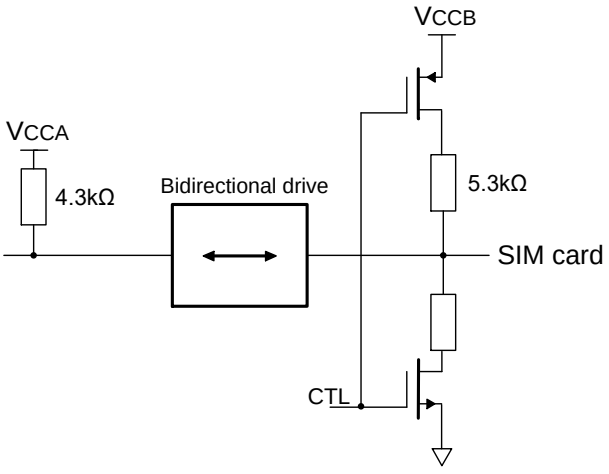


Figure3.IO voltage level translation architecture

When V_{CCB_EN} = 0 then CTL = VCCB and line is high-Z.
When V_{CCB_EN} = 1 then CTL = GND and line is active.

EMI filter

All input/output driver stages are equipped with EMI filters to reduce interferences towards sensitive mobile communication.

ESD protection

The device has robust ESD protections on all SIM card pins as well as on the V_{CCB} pin. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions		Min.	Max.	Unit
V_{CCA}	Host supply voltage			GND - 0.5	2.4	V
V_{CCB}	SIM supply voltage			GND - 0.5	4.0	V
V_I (CLK_HOST)	Input voltage on pin CLK_HOST	Input signal voltage, HOST side		GND - 0.5	V_{CCA} + 0.3	V
V_I (RST_HOST)	Input voltage on pin RST_HOST	Input signal voltage, HOST side		GND - 0.5	V_{CCA} + 0.3	V
V_I (IO_HOST)	Input voltage on pin IO_HOST	Input signal voltage, HOST side		GND - 0.5	V_{CCA} + 0.3	V
V_I (CLK_SIM)	Input voltage on pin CLK_SIM	Input signal voltage, SIM side		GND - 0.5	V_{CCB} + 0.3	V
V_I (RST_SIM)	Input voltage on pin RST_SIM	Input signal voltage, SIM side		GND - 0.5	V_{CCB} + 0.3	V
V_I (IO_SIM)	Input voltage on pin IO_SIM	Input signal voltage, SIM side		GND - 0.5	V_{CCB} + 0.3	V
T_{STG}	Storage temperature			-65	+150	°C
T_J	Junction temperature			-40	+150	°C
T_A	Ambient temperature			-40	+85	°C
V_{ESD}	Electrostatic discharge voltage	IEC 61000-4-2, level 4, all memory card- side pins, V_{CCB} and GND	Contact discharge	-8	+8	kV
			Air discharge	-15	+15	kV
		Human Body Model (HBM) JEDEC JESD22-A114F; all pins		-2000	+2000	V
		Charge Device Model (CDM) JEDEC JESD22-C101E; all pins		-1000	+1000	V
I_{LU} (IO)	Input/output latch-up current	JESD 78B: $-0.5xV_{CC}<V_I<1.5xV_{CC}$; $T_J<85°C$		-200	+200	mA

Note：All system level tests are performed with the application-specific capacitors connected to the supply pins V_{SUPPLY}, V_{LDO} and V_{CCA}.

Electrical Characteristics

($1.62V \le V_{CCB} \le 3.6V$, $1.08V \le V_{CCA} \le 1.98V$, T_A = -40°C to +85°C.)

Symbol	Parameter	Conditions	Min.	Typ.(1)	Max.	Unit
Basic Operation						
V_{CCA}	Supply voltage(2)		1.08		1.98	V
I_{CCA}	Supply current	Operating mode; IO_HOST = IO_SIM=HIGH f_{CLK_HOST} = 1MHz,		5	10	μA
		Quiescent current; IO_HOST = V_{CCA}, CLK_HOST = GND		0.01	1	μA
		Shutdown mode; IO_HOST=HIGH			1	μA
V_{CCB}	SIM supply voltage		1.62		3.6	V
I_{CCB}	SIM supply current	Operating mode; IO_HOST = IO_SIM=HIGH CLK/RST_HOST =LOW		3.7	8	μA
		Shutdown mode;			1	μA
V_I	Input voltage	host side	-0.3		V_{CCA}+0.3	V
		Sim card side	-0.3		V_{CCB}+0.3	
Automatic Enable Feature: V_{CCB}						
V_{CCB_EN}	Device enable voltage level	V_{CCA} ≥ 1.0V, V_{CCB} rising edge	1.62			V
V_{CCB_DIS}	Device disable voltage level	V_{CCA} ≥ 1.0V, V_{CCB} falling edge			0.80	V
Level Shifter						
V_{IH}(4)	HIGH-level input voltage	IO_HOST, RST_HOST, CLK_HOST 1.08V ≤ V_{CCA} < 1.98V	0.65× V_{CCA}		V_{CCA}+0.3	V
		IO_SIM	0.65× V_{CCB}		V_{CCB}+0.3	V
V_{IL}(4)	LOW-level input voltage	IO_HOST, RST_HOST, CLK_HOST	-0.15		0.35× V_{CCA}	V
		IO_SIM	-0.15		0.35× V_{CCB}	V

Electrical Characteristics(Continued)

(1.62V ≤ V_{CCB} ≤ 3.6V, 1.08V ≤ V_{CCA} ≤ 1.98V, T_A = -40°C to +85°C.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{PU}	Pull-up resistance	IO_SIM connected to V_{CCB},	4	5.3	7	kΩ
		IO_HOST connected to V_{CCA}	3.3	4.3	6	kΩ
R_{PD}	Pull-down resistance	CLK_HOST/SIM, RST_HOST/SIM;	70	100	130	kΩ
V_{OH}	HIGH-level output voltage	RST_SIM, CLK_SIM; I_{OH} = -1mA	0.85× V_{CCB}		V_{CCB}	V
		IO_SIM; I_{OH} = -20μA	0.85× V_{CCB}		V_{CCB}	V
		IO_HOST; I_{OH} = -20μA	0.85× V_{CCA}		V_{CCA}	V
V_{OL}	LOW-level output voltage	RST_SIM, CLK_SIM; I_{OL} = 1mA	0		0.115× V_{CCB}	mV
		IO_SIM; I_{OL} = 1mA	0		0.125× V_{CCB}	mV
		IO_HOST; I_{OL} = 1mA	0		0.25× V_{CCA}	mV
EMI Filter						
Rs	Series resistance[5]	IO_SIM; R1 tolerance ± 30%	-	30	-	Ω
		RST_SIM; R1 tolerance ± 30%	-	30	-	Ω
		CLK_SIM; R1 tolerance ± 30%	-	30	-	Ω
Cio	Input/Output/ Capacitance[5]	IO_SIM	-	8.5	-	pF
		RST_SIM	-	8.5	-	pF
		CLK_SIM	-	8.5	-	pF
Dynamic characteristics **F_{CLK} = F_{IO} = 1MHz; unless otherwise specified. Refer to Figure 4; V_{CCA} = 1.8V; V_{CCB} = 3.0V; SIM card C_L ≤ 30pF; host C_L ≤10 pF**						
t_{PD}	t_{PHL} and t_{PLH} are t_{PD} propagation delay[5]	I/O channel; SIM card side to host side		8	15	ns
		all channels; host side to SIM card side		8	15	ns
t_T	t_{THL} and t_{TLH} are the transition time.[5]				10	ns

Electrical Characteristics(Continued)

(1.62V ≤ V_{CCB} ≤ 3.6V, 1.08V ≤ V_{CCA} ≤ 1.98V, T_A = -40°C to +85°C.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{SK}(o)$	Output skew time[3] [5]	between channels; IO_SIM and CLK_SIM		2		ns
F_{CLK}	Clock frequency[5]	CLK_SIM			10	MHz
V_{CCA} = 1.2V; V_{CCB} = 1.8V; SIM card C_L ≤ 30pF; host C_L ≤ 10pF						
t_{PD}	t_{PHL} and t_{PLH} are t_{PD} propagation delay[5]	I/O channel; SIM card side to host side		15	25	ns
		all channels; host side to SIM card side		15	25	ns
t_T	t_{THL} and t_{TLH} are the transition time.[5]				10	ns
$t_{SK}(o)$	Output skew time[3][5]	between channels; IO_SIM and CLK_SIM		2		ns
F_{CLK}	Clock frequency[5]	CLK_SIM			10	MHz

Note1: Typical values measured at 25 °C

Note2: The voltage must not exceed 1.98 V steady state.

Note3: Skew between any two outputs of the same package switching in the same direction with same C_L.

Note4: V_{IL}, V_{IH} depend on the individual supply voltage per interface

Note5: Guaranteed by design Note: This parameter is guaranteed by design and characterization.

Timing Waveform

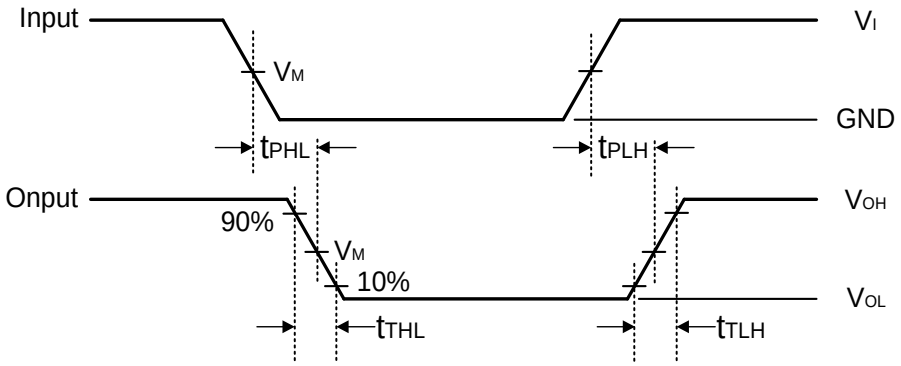


Figure 4. Data Input to Data Output Propagation Delay Times

Measurement points are given in EC table.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

t_{PHL} and t_{PLH} are t_{PD} propagation delay; t_{THL} and t_{TLH} are the transition time.

Note:This electric circuit only supplies for reference.

Application Circuits

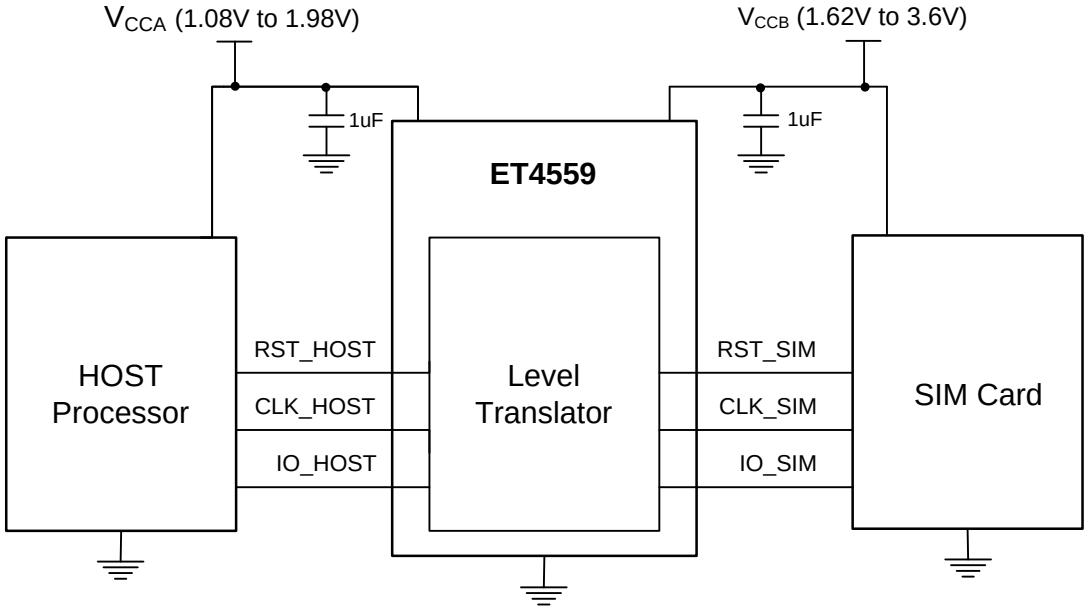


Figure 5. ET4559 application circuit interfacing with typical SIM card

Input/output capacitor considerations

It is recommended that a 1μF and 100nF capacitors having low Equivalent Series Resistance (ESR) are used respectively at V_{CCA} and V_{CCB} input terminals of the device. X5R and X7R type multi-layer ceramic capacitors (MLCC) are preferred because they have minimal variation in value and ESR over temperature. The maximum ESR should be < 500mΩ (50mΩ typical).

Layout consideration

The capacitors should be placed directly at the terminals and ground plane. It is recommended to design the PCB so that the V_{CCA} and V_{CCB} pins are bypassed with a capacitor with each ground returning to a common node at the GND pin of the device such that ground loops are minimized.

Level translator stage

The architecture of the device I/O channel is shown in Figure 6. The device does not require an extra input signal to control the direction of data flow from host to SIM or from SIM to host.

As a change of driving direction is just possible when both sides are in HIGH state, the control logic is recognizing the first falling edge granting it control about the other signal side.

During a rising edge signal, the non-driving output is driven by a one- shot circuit to accelerate the rising edge. In case of a communication error or some other unforeseen incident that would drive both connected sides to be drivers at the same time, the internal logic automatically prevents stuck-at situation, so both I/Os will return to HIGH level once released from being driven LOW.

The channels RST and CLK just contain single direction drivers without the holding mechanism of the I/O channel, as these are just driven from the host to the card side.

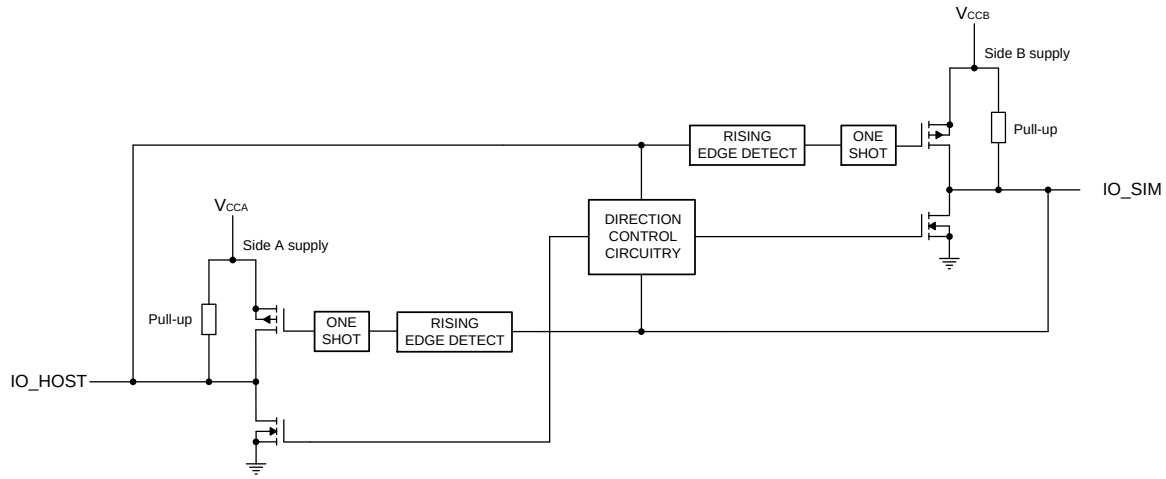
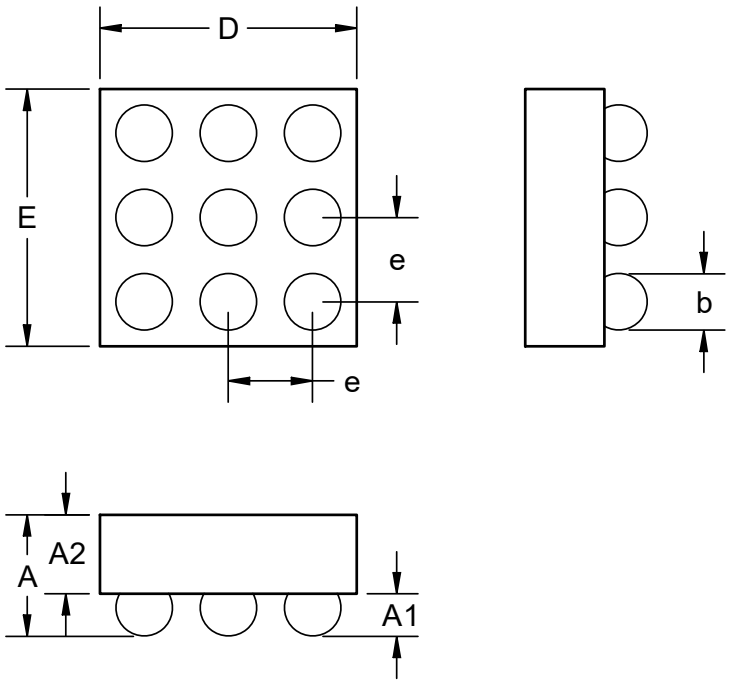


Figure 6.Automatic direction control level translator for HIGH-level direction change interfaces

Package Dimension

FOWLP 9

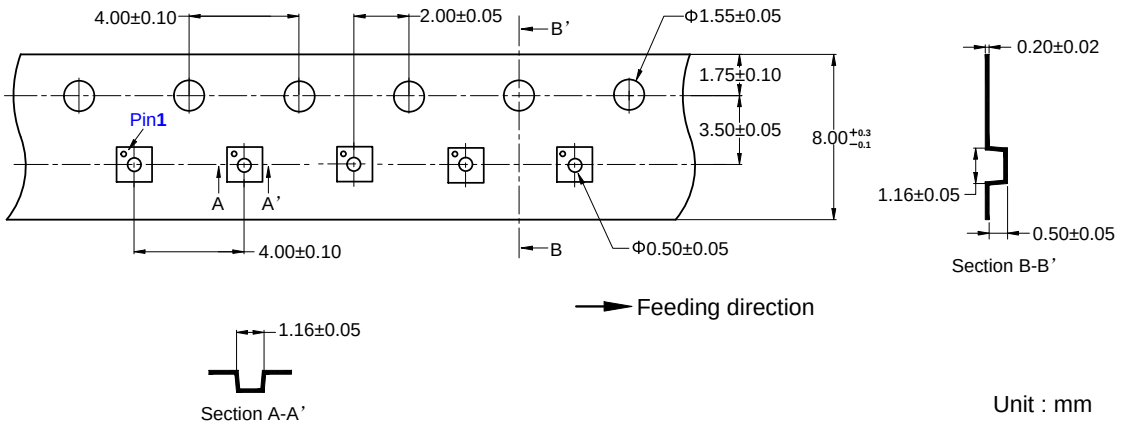


COMMON DIMENSIONS

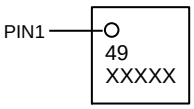
SYMBOL	MIN	NOM	MAX
A	0.377	0.430	0.483
A1	0.140	0.160	0.180
A2	0.237	0.270	0.303
b	0.191	0.211	0.231
D	1.010	1.060	1.110
E	1.010	1.060	1.110
e	0.350BSC		

Unit: mm

Tape Information



Marking



49 - Part Number

XXXXX - Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024.02.26	Preliminary Version	Liu Kangsheng	Liu Kangsheng	Liujy
1.0	2024.09.18	Update package Dimension	Cao-Jiachen	Liu Kangsheng	Liujy