# 2 Channel Auto-Bidirectional Multi-Voltage Level Translator for Open-Drain and Push-Pull Applications

## General Description

The ETF0102 supports bidirectional voltage translation without the need for DIR pin which minimizes system effort. The ETF0102 supports up to 100MHz up translation and greater than 100MHz down translation at ≤ 30pF capacitive load and up to 40MHz up or down translation at 50pF capacitive load.

The ETF0102 supports 5V tolerance on I/O port which makes it compatible with TTL levels in industrial and telecom applications. The ETF0102 is able to set up different voltage translation levels which makes it very flexible.

The ETF0102 is available in DFN8 (1.4mm ×1mm) package.

## Features

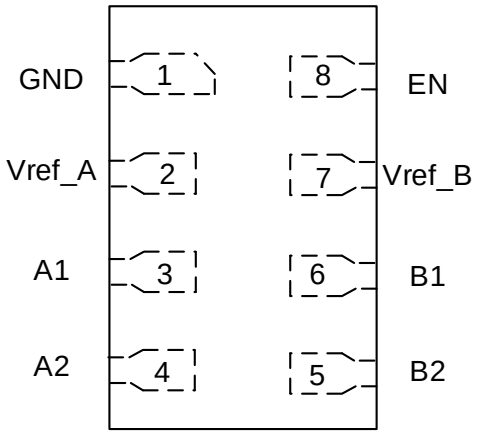
- No directional control required
- Data Rates: 100MHz up translation and greater than 100MHz down translation at ≤ 30pF capacitive load and up to 40MHz up or down translation at 50pF capacitive load
- Allows bidirectional voltage-level translation between: 0.95V ~3.3V ↔ 1.8V~5V
- Low standby current
- 5V tolerance I/O port to support TTL
- Low $R_{ON}$ provides less signal distortion
- Flow-through pinout for easy PCB trace routing
- Extended temperature: -40°C to 85°C
- Package information:

| Part No. | Package | MSL |
|---|---|---|
| ETF0102Y | DFN8 (1.4mm×1mm) | Level 1 |

## Applications

- $I^2C$, SMBus, PMBus, MDIO, UART, SDIO, GPIO, and other two-signal interfaces
- Enterprise systems
- Communications equipment
- Personal computers
- Industrial automation

## Pin Configuration

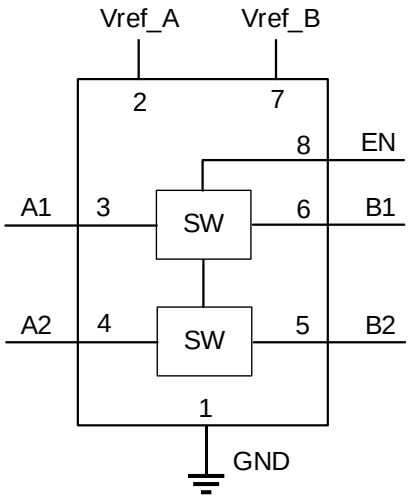



Top View

## Pin Function

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| GND | 1 | Ground pin. |
| Vref_A | 2 | Reference supply voltage. |
| An | 3,4 | Auto-Bidirectional Data port. |
| Bn | 5,6 | Auto-Bidirectional Data port. |
| Vref_B | 7 | Reference supply voltage. |
| EN | 8 | Enable input.<br>Connect to Vref_B and pull-up through a high resistor(200kΩ). |

## Block Diagram



## Functional Description

The ETF0102 can be used in level-translation applications for interfacing devices or systems operating with one another that operate at different interface voltages. The ETF0102 is ideal for use in applications where an open-drain driver is connected to the data I/Os. With appropriate pull-up resistors and layout, ETF0102 can achieve 100MHz. The ETF0102 can also be used in applications where a push-pull driver is connected to the data I/Os.

### Auto Bidirectional Voltage Translation

The device is an auto bidirectional voltage level translator that is operational from 0.95 to 5.5V on Vref_A and 1.8 to 5.5V on Vref_B. This allows bidirectional voltage translation between 0.95V and 5.5V without the need for a direction pin in open-drain or push-pull applications. The ETF0102 supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 30pF capacitance and 250Ω pullup resistor. Both the output driver of the controller and the peripheral device output can be push-pull or open-drain (pull-up resistors may be required). In both up and down translation, the B-side is often referred to as the high side and refers to devices connected to the B ports. The A-side can be referred to as the low side.

### Output Enable

To enable the I/O pins, the EN input should be tied directly to Vref_B during operation and both pins must be pulled up to the HIGH side (VCCB) through a bias resistor (typically 200kΩ). To be in the high impedance state during power-up, power-down, or during operation, the EN pin must be LOW. The EN pin should always be tied directly to the Vref_B pin and is recommended to be disabled by an open-drain driver without a pullup resistor. This allows Vref_B to regulate the EN input and bias the channels for proper translation. A filter capacitor on Vref_B is recommended for a stable supply at the device.

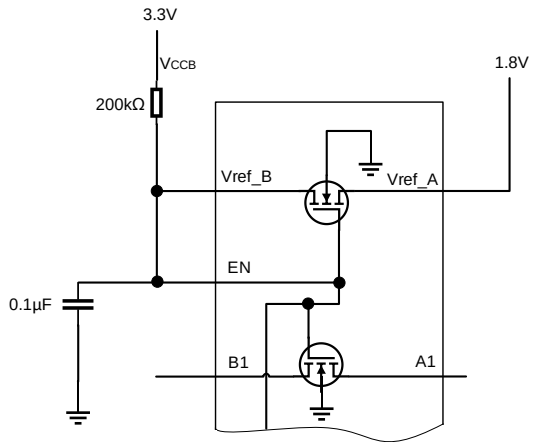



**Figure 1. Enable Pin Tied to Vref_B Directly and to VCCB Through a Bias Resistor**

The supply voltage of open drain I/O devices can be completely different from the supplies used for the ETF0102 and has no impact on the operation.

**Table 1. Enable Pin Function Table（EN is controlled by Vref_B logic levels.）**

| EN PIN | Data Port State |
|---|---|
| Tied directly to Vref_B | An = Bn |
| L | Hi-Z |

**Device Functional Modes**

For each channel (n), when either the An or Bn port is LOW, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled LOW. The low RON of the switch allows connections to be made with minimal propagation delay and signal distortion.Table 2. provides a summary of device operation.

**Table 2. Device Functionality**

| Signal Direction(1) | Input State | Switch State | Functionality |
|---|---|---|---|
| B to A (Down Translation) | B = LOW | ON (Low Impedance) | A-side voltage is pulled low through the switch to the B-side voltage |
| | B = HIGH | OFF (High Impedance) | A-side voltage is clamped at $V_{ref\_A}$ (2) |
| A to B (Up Translation) | A = LOW | ON (Low Impedance) | B-side voltage is pulled low through the switch to the A-side voltage |
| | A = HIGH | OFF (High Impedance) | B-side voltage is clamped at $V_{ref\_A}$ and then pulled up to the $V_{PU}$ supply voltage |

***Note (1)***: The downstream channel should not be actively driven through a low impedance driver, or else bus contention may occur.

***Note (2)***: The A-side can have a pullup to Vref_A for additional current drive capability or may also be pulled above Vref_A with a pullup resistor. Specifications in the Recommended Operating Conditions section should always be followed.

**Up Translation**

When the signal is being driven from A to B and the An port is HIGH, the switch will be OFF and the Bn port will then be driven to a voltage higher than Vref_A by the pull-up resistor that is connected to the pull-up supply voltage ($V_{PU}$). This functionality allows seamless translation between higher and lower voltages selected by the user, without the need for directional control. Pull-up resistors are always required on the high side, and pull-ups are only required on the low side, if the low side of the device's output is open drain or its input has a leakage greater than 1μA.

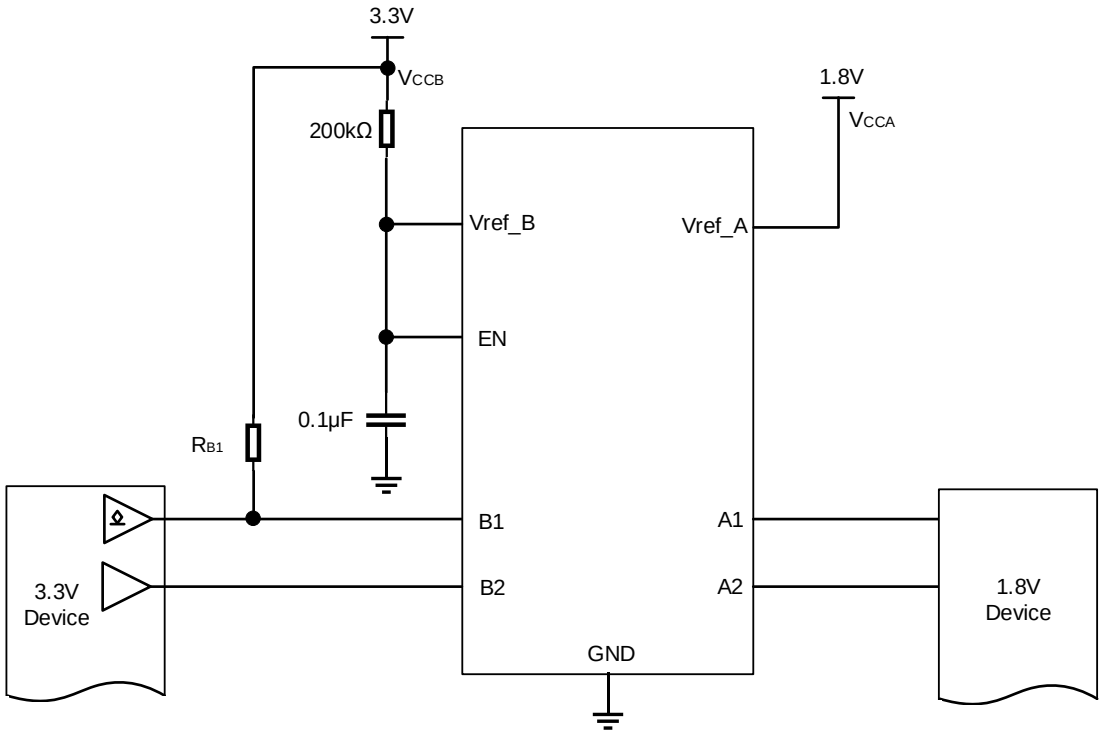



**Figure 2. Up Translation Example Schematic with Push-Pull and Open Drain Configuration**

Up translation with the ETF0102 requires attention to two important factors: maximum data rate and sink current. Maximum data rate is directly related to the rising edge of the output signal. Sink current depends on supply values and the chosen pull-up resistor values. Equation 1 shows the maximum data rate formula and Equation 2 shows the maximum sink current formula, both of which are estimations. A low RC value is needed to reach high speeds, which also require strong drivers.

$$\frac{1}{3\times 2R_{B1}C_{B1}} \equiv \frac{1}{6R_{B1}C_{B1}}\left(\frac{\text{bits}}{\text{sec}\,ond}\right) \quad (1)$$

$$I_{OL} \cong \frac{VCCA}{R_{A1}} + \frac{VCCB}{R_{B1}}(A) \quad (2)$$

**Down Translation**

When the signal is being driven HIGH from the Bn port to An port, the switch will be OFF, clamping the voltage on the An port to the voltage set by Vref_A. A pull-up resistor can be added on either side of the device. There are special circumstances that allow the removal of one or both of the pull-up resistors. If the signal is always going to be down translated from a push-pull transmitter, then the resistor on the B-side can be removed. If the leakage current into the receiver on the A-side is less than 1µA, then the resistor on the A-side can also be removed. This arrangement with no external pull-up resistors can be used when down translating from a push-pull output to a low-leakage input. For an open drain transmitter, the pull-up resistor on the B-side is necessary because an open drain output can't drive high by itself.

## Absolute Maximum Ratings

| Symbol | Parameters (Items) | Value | Unit |
|---|---|---|---|
| $V_I$ | Input Voltage | -0.3 to 6.0 | V |
| $V_{I/O}$ | Input/output Voltage | -0.3 to 6.0 | V |
| $I_O$ | Continuous Channel Current | 0 to 128 | mA |
| $I_{IK}$ | Input Clamp Current | -50 | mA |
| $T_{STG}$ | Storage Temperature Range | -65 to +150 | ºC |
| $T_J$ | Operating Junction Temperature | -40 to +150 | ºC |
| $R_{\theta JA}$ | Junction-to-ambient Thermal Resistance | 250 | °C/W |
| $V_{ESD}$ | Human Body Model (JESD22-A114) | ±2000 | V |
| | Charged Device Model (JESD22-C101) | ±1000 | V |
| Latch-up | JESD 17 | ±100 | mA |

## Recommended Operating Conditions

| Symbol | Parameters | Rating | Unit |
|---|---|---|---|
| $V_{I/O}$ | Input/output Voltage | 0 to 5.5 | V |
| $V_{REF\_A/B/EN}$ | Reference Voltage | 0 to 5.5 | V |
| $I_{PASS}$ | Pass transistor Current | 64 | mA |
| $T_A$ | Operating Ambient Temperature | -40 to +85 | ºC |

## Electrical Characteristics

$T_A$=-40ºC~85ºC, from A to B or B to A (unless otherwise noted, all typical values are at $T_A$ = 25°C.)

| Symbol | Parameters | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | I/O Input Clamp Voltage | $I_I$ = -18mA, $V_{EN}$ = 0V | | | | -1.2 | V |
| $I_{IH}$ | Input Leakage Current | $V_I$ = 5V, $V_{EN}$ = 0V | | | | 5.0 | uA |
| $I_{CC}$ | Input Current | $V_{ref\_B}$ = $V_{EN}$ = 5.5V, $V_{ref\_A}$ = 4.5V, $I_O$ = 0mA, $V_I$ = $V_{CC}$ or GND | | | 0.1 | 1 | uA |
| $C_{I(ref\_A/B/EN)}$ (3) | Input Capacitance | $V_I$ = 3V or 0V， $T_A$ = 25°C. | | | 11 | | pF |
| $C_{iO(off)}$ (3) | Off Capacitance | $V_I$ = 3V or 0V, $V_{EN}$ = 0V， $T_A$ = 25°C. | | | 4.0 | 6.0 | pF |
| $C_{iO(on)}$ (3) | On Capacitance | $V_I$ = 3V or 0V, $V_{EN}$ = 3V， $T_A$ = 25°C. | | | 12 | 17 | pF |
| $R_{on}$(4) | On-State Resistance | $V_I$ = 0V, $I_O$=64mA | $V_{ref\_A}$=3.3V; $V_{ref\_B}$=$V_{EN}$=5V | | 3.0 | 7.0 | Ω |
| | | | $V_{ref\_A}$=1.8V; $V_{ref\_B}$=$V_{EN}$=5V | | 4.0 | 10 | |
| | | | $V_{ref\_A}$=1.0V; $V_{ref\_B}$=$V_{EN}$=5V | | 5.0 | 25 | |
| | | $V_I$ = 0V, $I_O$=32mA | $V_{ref\_A}$=1.8V; $V_{ref\_B}$=$V_{EN}$=5V | | 4.0 | 9.0 | |
| | | | $V_{ref\_A}$=2.5V; $V_{ref\_B}$=$V_{EN}$=5V | | 3.0 | 8.0 | |
| | | $V_I$ = 1.8V, $I_O$=15mA | $V_{ref\_A}$=3.3V; $V_{ref\_B}$=$V_{EN}$=5V | | 4.0 | 13 | |
| | | $V_I$ = 1.0V, $I_O$=10mA | $V_{ref\_A}$=1.8V; $V_{ref\_B}$=$V_{EN}$=3.3V | | 7.0 | 24 | |
| | | $V_I$ = 0V, $I_O$=10mA | $V_{ref\_A}$=1.0V; $V_{ref\_B}$=$V_{EN}$=3.3V | | 5.0 | 18 | |
| | | $V_I$ = 0V, $I_O$=10mA | $V_{ref\_A}$=1.0V; $V_{ref\_B}$=$V_{EN}$=1.8V | | 6.0 | 19 | |

***Note (3)***: Guaranteed by design and characterization, not a FT item.

***Note (4)***: Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

## AC Performance (Translating Down) Switching Characteristics

$T_A$=-40ºC~85ºC, from B to A, RL=1KΩ (unless otherwise noted, all typical values are at $T_A$ = 25°C.)

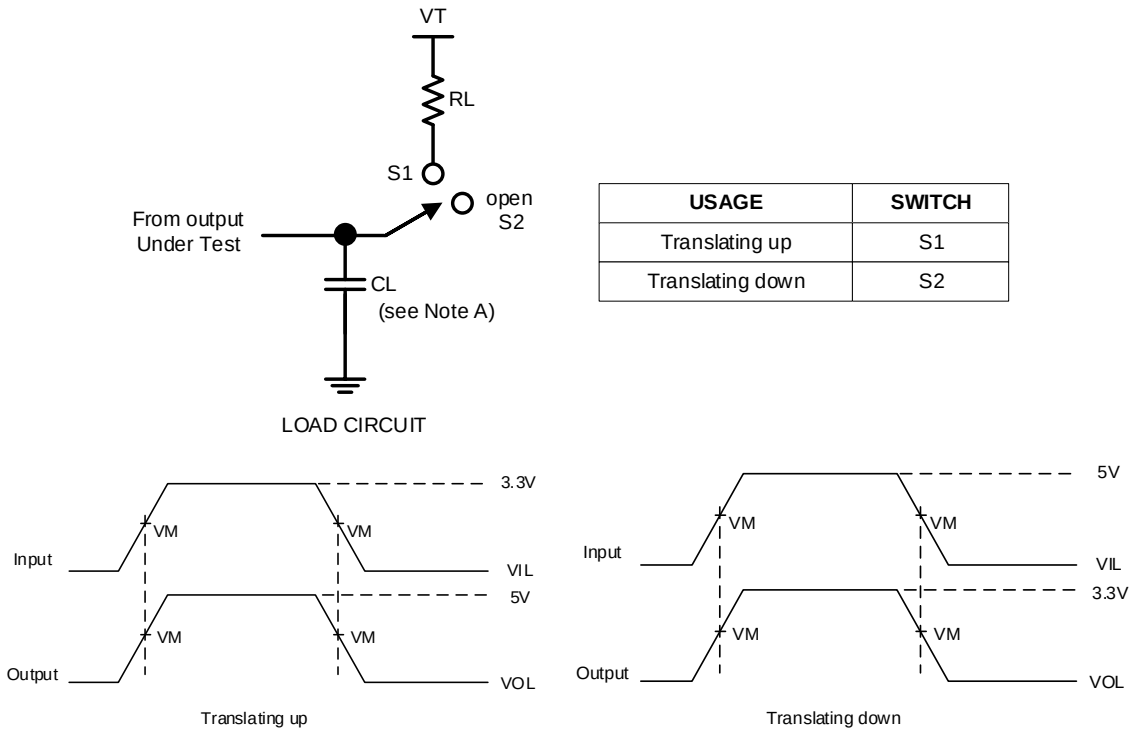
| Symbol | Parameters | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Low-to-High Propagation Delay | $V_{CCB}$ = $V_{IH}$ =1.8V, $V_{CCA}$ = 1.2V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.8 | | ns |
| | | | $C_L$ = 30pF | | 1.4 | | |
| | | | $C_L$ = 50pF | | 3.0 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.62V, $V_{CCA}$ = 1.08V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.8 | | |
| | | | $C_L$ = 30pF | | 1.2 | | |
| | | | $C_L$ = 50pF | | 3.2 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.62V, $V_{CCA}$ = 1.32V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.8 | | |
| | | | $C_L$ = 30pF | | 1.1 | | |
| | | | $C_L$ = 50pF | | 2.4 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.98V, $V_{CCA}$ = 1.08V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.8 | | |
| | | | $C_L$ = 30pF | | 1.1 | | |
| | | | $C_L$ = 50pF | | 2.6 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.98V, $V_{CCA}$ = 1.32V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.8 | | |
| | | | $C_L$ = 30pF | | 1.2 | | |
| | | | $C_L$ = 50pF | | 2.4 | | |
| $t_{PHL}$ | High-to-Low Propagation Delay | $V_{CCB}$ = $V_{IH}$ =1.8V, $V_{CCA}$ = 1.2V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.7 | | |
| | | | $C_L$ = 30pF | | 1.3 | | |
| | | | $C_L$ = 50pF | | 2.0 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.62V, $V_{CCA}$ = 1.08V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.8 | | |
| | | | $C_L$ = 30pF | | 1.4 | | |
| | | | $C_L$ = 50pF | | 2.2 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.62V, $V_{CCA}$ = 1.32V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.9 | | |
| | | | $C_L$ = 30pF | | 1.7 | | |
| | | | $C_L$ = 50pF | | 2.6 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.98V, $V_{CCA}$ = 1.08V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.6 | | |
| | | | $C_L$ = 30pF | | 1.1 | | |
| | | | $C_L$ = 50pF | | 1.7 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.98V, $V_{CCA}$ = 1.32V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.7 | | |
| | | | $C_L$ = 30pF | | 1.2 | | |
| | | | $C_L$ = 50pF | | 1.9 | | |

## AC Performance (Translating Up) Switching Characteristics

$T_A$=-40ºC~85ºC, from A to B, RL=1KΩ (unless otherwise noted, all typical values are at $T_A$ = 25°C.)

| Symbol | Parameters | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Low-to-High Propagation Delay | $V_{CCB}$ = $V_{IH}$ =1.8V, $V_{CCA}$ = 1.2V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 1.1 | | ns |
| | | | $C_L$ = 30pF | | 1.3 | | |
| | | | $C_L$ = 50pF | | 1.9 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.62V, $V_{CCA}$ = 1.08V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 1.0 | | |
| | | | $C_L$ = 30pF | | 1.1 | | |
| | | | $C_L$ = 50pF | | 1.8 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.62V, $V_{CCA}$ = 1.32V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.9 | | |
| | | | $C_L$ = 30pF | | 1.0 | | |
| | | | $C_L$ = 50pF | | 1.4 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.98V, $V_{CCA}$ = 1.08V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.9 | | |
| | | | $C_L$ = 30pF | | 1.0 | | |
| | | | $C_L$ = 50pF | | 1.6 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.98V, $V_{CCA}$ = 1.32V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 0.9 | | |
| | | | $C_L$ = 30pF | | 1.0 | | |
| | | | $C_L$ = 50pF | | 1.8 | | |
| $t_{PHL}$ | High-to-Low Propagation Delay | $V_{CCB}$ = $V_{IH}$ =1.8V, $V_{CCA}$ = 1.2V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 1.7 | | |
| | | | $C_L$ = 30pF | | 2.6 | | |
| | | | $C_L$ = 50pF | | 4.2 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.62V, $V_{CCA}$ = 1.08V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 1.8 | | |
| | | | $C_L$ = 30pF | | 2.8 | | |
| | | | $C_L$ = 50pF | | 4.5 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.62V, $V_{CCA}$ = 1.32V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 1.6 | | |
| | | | $C_L$ = 30pF | | 2.5 | | |
| | | | $C_L$ = 50pF | | 4.1 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.98V, $V_{CCA}$ = 1.08V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 1.7 | | |
| | | | $C_L$ = 30pF | | 2.7 | | |
| | | | $C_L$ = 50pF | | 4.4 | | |
| | | $V_{CCB}$ = $V_{IH}$ =1.98V, $V_{CCA}$ = 1.32V, $V_{IL}$ = 0V, and $V_M$ = 0.5 $V_{CCA}$ | $C_L$ = 20pF | | 1.5 | | |
| | | | $C_L$ = 30pF | | 2.4 | | |
| | | | $C_L$ = 50pF | | 4.0 | | |

## AC Performance Test Circuit




| USAGE | SWITCH |
|---|---|
| Translating up | S1 |
| Translating down | S2 |

**Figure 3. AC Performance Load Circuit for Outputs**

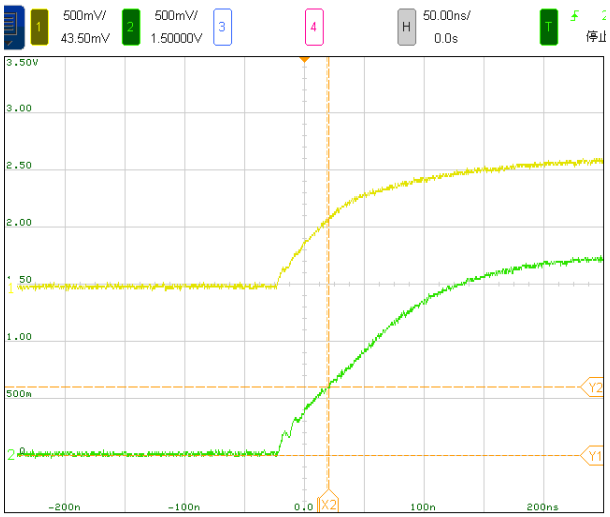
***Note A :*** CL includes probe and jig capacitance.

***Note B :*** Generators that have the following characteristics generate all input pulses: PRR ≤ 10MHs, Zo = 50Ω, tr ≤ 2ns, tf ≤ 2ns.

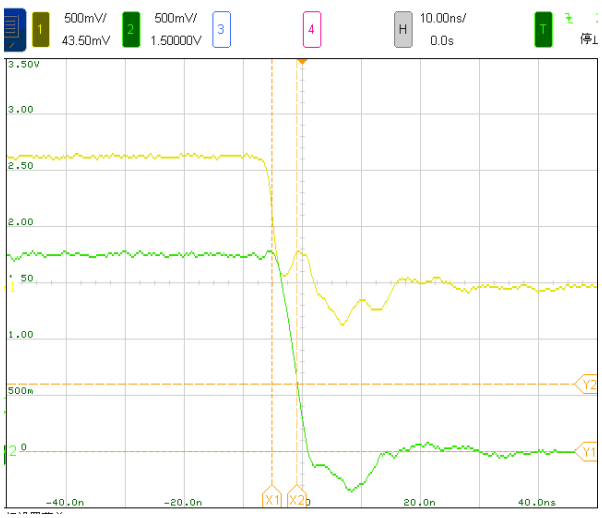
***Note C :*** The outputs are measured one at a time, with one transition per measurement.

Typical Characteristics

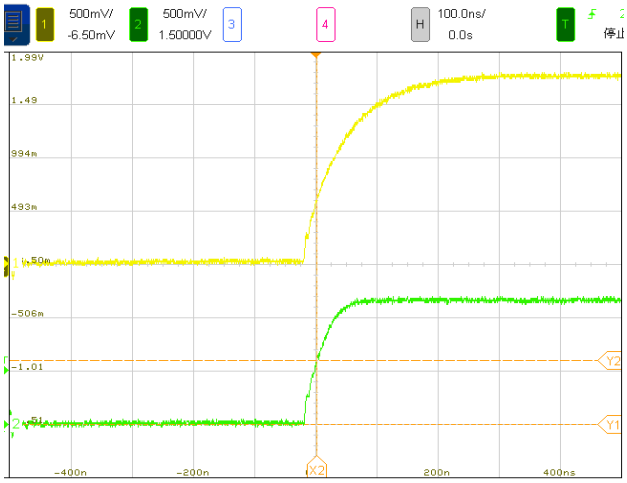
($V_{CCB}$=1.8V, $V_{CCA}$=1.2V, $C_L$=50pF, $R_{PU}$ =1KΩ，$C_L$ = 50pF unless otherwise noted $T_A$=25°C.)



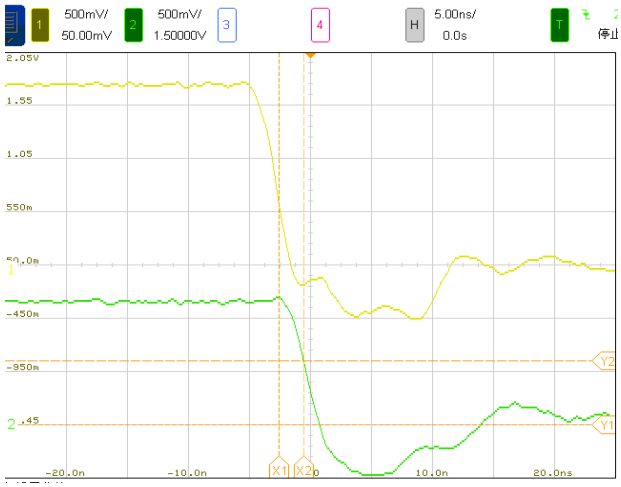
AC Performance $t_{PLH}$ 1.2V to 1.8V



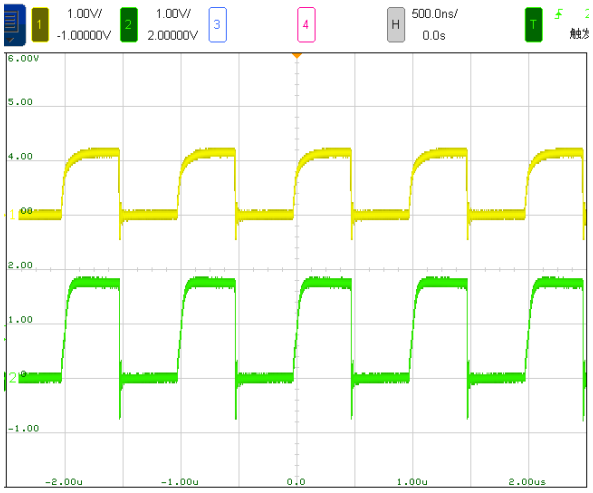
AC Performance $t_{PHL}$ 1.2V to 1.8V



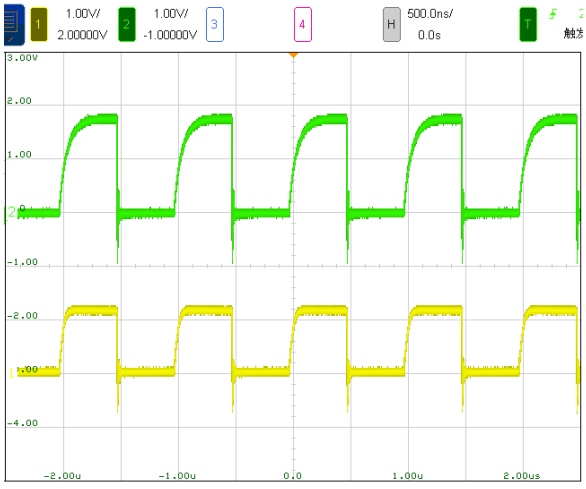
AC Performance $t_{PLH}$ 1.8V to 1.2V



AC Performance $t_{PHL}$ 1.8V to 1.2V



Voltage Translation, 1.2V to 1.8V, f=1MHz



Voltage Translation, 1.8V to 1.2V, f=1MHz

## Application Circuits

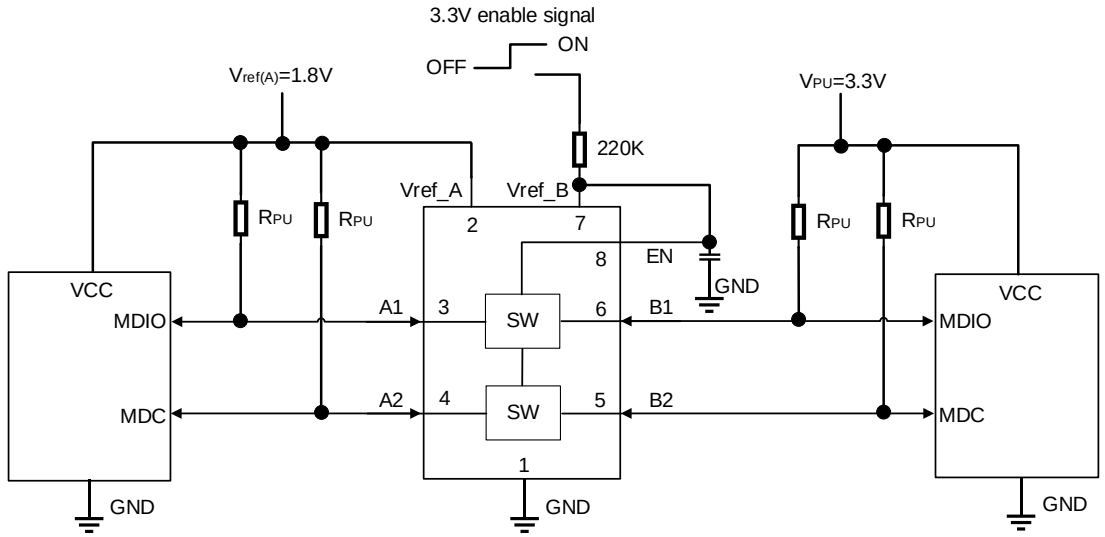



**Figure 4. Typical Application Circuit for Open-Drain Translation (MDIO Shown as an Example)**

In the previous figure, Vref_B is connected through a 200kΩ resistor to a 3.3V power supply and Vref_A is set to 1.8V. The A1 and A2 channels have a maximum output voltage equal to Vref_A and the B1 and B2 channels have has a maximum output voltage equal to $V_{PU}$.

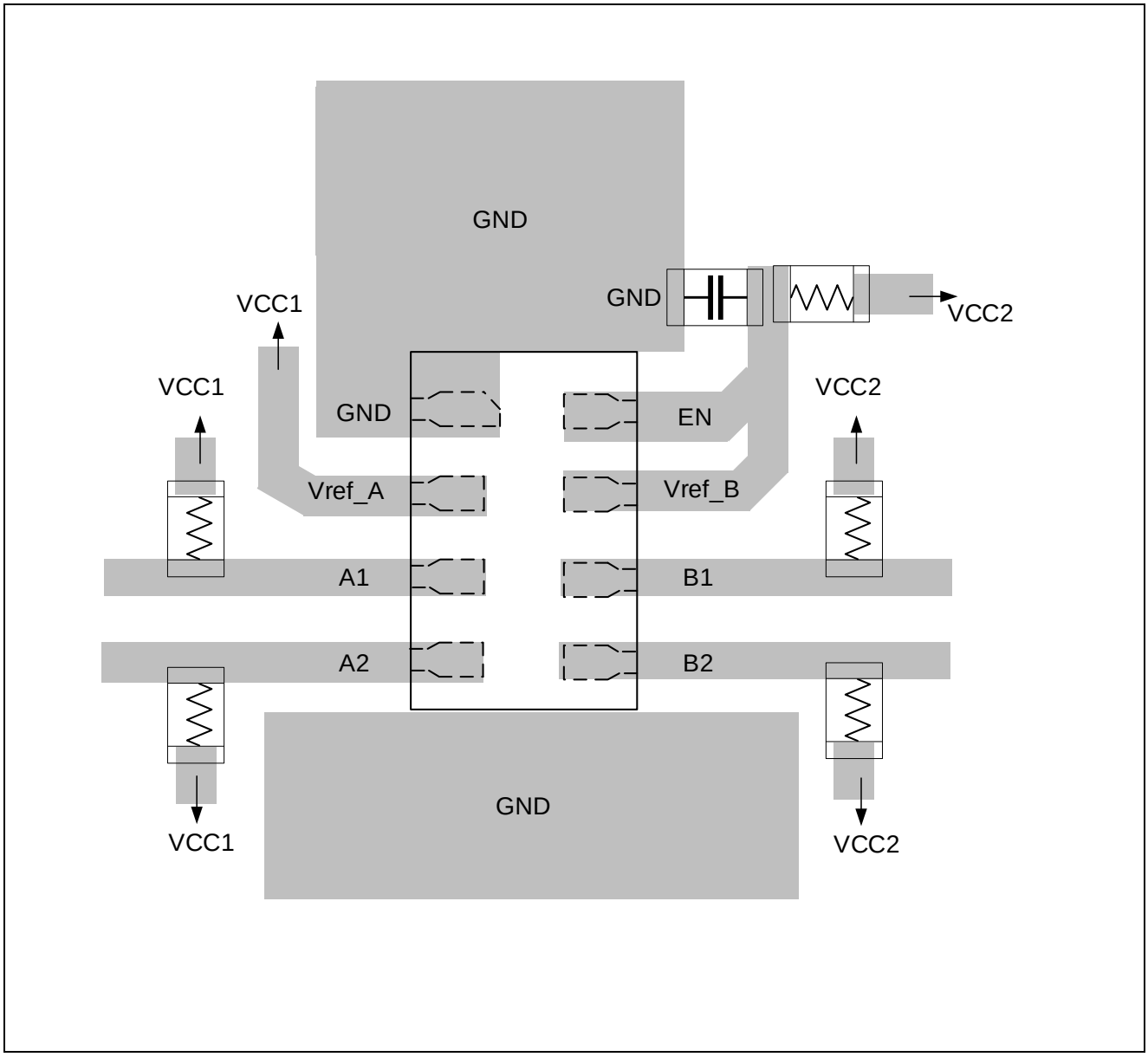
The ETF0102 has an EN input that is used to disable the device by setting EN LOW, placing all I/Os in the high-impedance state. Since the ETF0102 of devices are switch-type voltage translators, the power consumption is very low.

**Table 3. Application Operating Condition**

| Symbol | Parameters | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{ref\_A}$ (5) | reference voltage (A) | 0.9 | | 5.5 | V |
| $V_{ref\_B}$ | reference voltage (B) | $V_{ref\_A}$ + 0.8 | | 5.5 | V |
| $V_{I(EN)}$ | input voltage on EN pin | $V_{ref\_A}$ + 0.8 | | 5.5 | V |
| $V_{PU}$ | pull-up supply voltage | 0 | | $V_{ref\_B}$ | V |

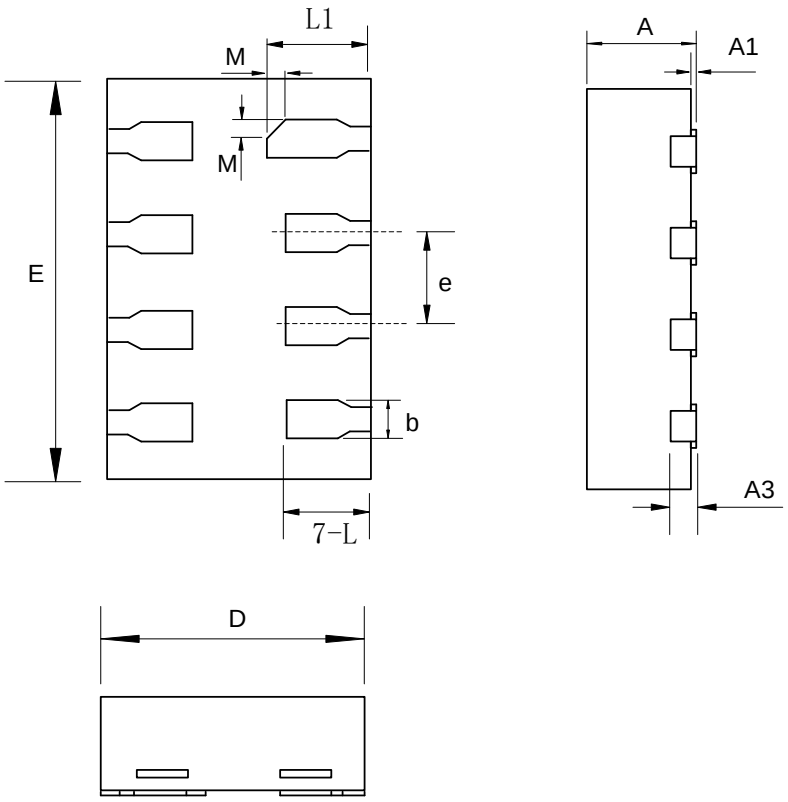
***Note (5):*** Vref_A is required to be the lowest voltage level across all inputs and outputs. The 200kΩ, bias resistor is required to allow Vref_B to regulate the EN input and properly bias the device for translation.

**PCB Layout Guide**



## Package Dimension

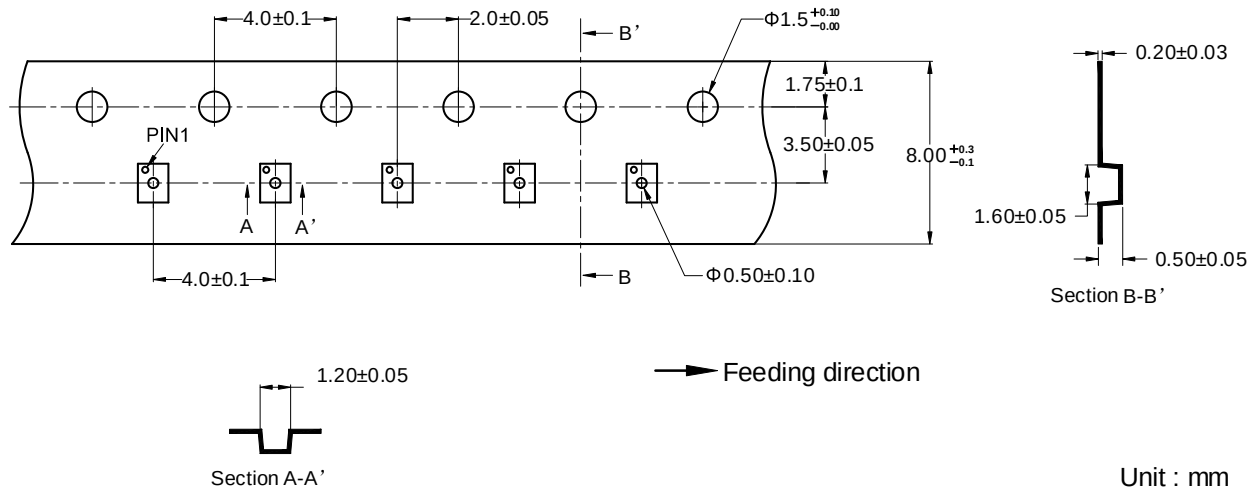
**DFN8(1.4×1.0)**



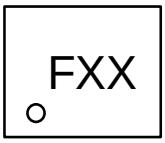

**Dimensions Table (Units: mm)**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.34 | 0.37 | 0.40 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.10REF | |
| b | 0.125 | 0.175 | 0.225 |
| D | 0.90 | 1.00 | 1.10 |
| E | 1.30 | 1.40 | 1.50 |
| e | 0.30 | 0.35 | 0.40 |
| L | 0.25 | 0.30 | 0.35 |
| L1 | 0.35 | 0.40 | 0.45 |
| M | | 0.10REF | |

## Tape Information




## Marking Information




F = Part Number

XX = Tracking Number

## Revision History and Checking Table

| Version | Date | Revision Item | Modifier | Function & Spec Checking | Package & Tape Checking |
|---|---|---|---|---|---|
| 1.0 | 2025.03.06 | Initial Version | Zhangwang | Liuyg | Liujy |
| | | | | | |