Octal Buffers/Drivers With 3-State Outputs

General Description

The ET74HCT541V octal buffers/drivers is ideal for driving bus lines or buffer memory address registers. The device feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable($\overline{OE}$ 1 or $\overline{OE}$ 2) input is high, all corresponding outputs are in the high-impedance state. The outputs provide non-inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to VCC through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Features

- Designed for 4.5 to 5.5V VCC Operation
- Inputs are TTL Voltage Compatible
- Latch-Up performance > 250mA
- ESD Performance:

  -- Human Body Model >2000V

  -- Charged Device Model >1000V
- Part No. and package

Part No.	Package
ET74HCT541V	TSSOP20 (6.5mm×4.4mm)

Applications

- Fully compliant with standards for automotive applications
- Combine normal power signals from multiple power rails

Pin Configuration

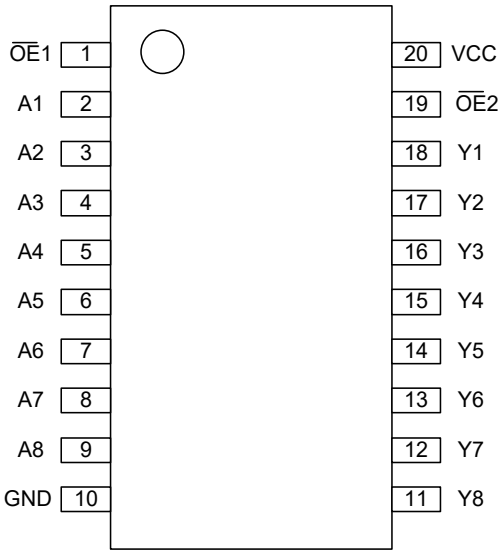


Figure 1. Top View

Pin Function

Pin No.	Name	Description
1	$\overline{OE}$ 1	Output Enable 1
2	A1	Input A1
3	A2	Input A2
4	A3	Input A3
5	A4	Input A4
6	A5	Input A5
7	A6	Input A6
8	A7	Input A7
9	A8	Input A8
10	GND	Ground
11	Y8	Output Y8
12	Y7	Output Y7
13	Y6	Output Y6
14	Y5	Output Y5
15	Y4	Output Y4
16	Y3	Output Y3
17	Y2	Output Y2
18	Y1	Output Y1
19	$\overline{OE}$ 2	Output Enable 2
20	VCC	Power

Block Diagram

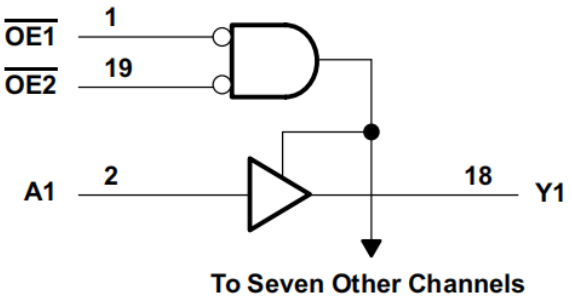


Figure 2. Logic Diagram

Functional Description

Function Table

Inputs			Output
$\overline{OE}$ 1	$\overline{OE}$ 2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Note: H = High voltage level ,

L = Low voltage level ,

X = Don't care ,

Z = High-impedance OFF-state.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage range	-0.5 to 7.0	V
V_I	Input voltage range (1)	-0.5 to 7.0	V
V_O	Output voltage range(1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	Input clamp current, V_I < GND	-20	mA
I_{OK}	Output clamp Current V_O < GND, V_O > V_{CC}	±20	mA
I_O	Continuous output current, I_O(V_O=0 to V_{CC})	±25	mA
I_{CC}	Continuous current through V_{CC}	±75	mA
I_{GND}	Continuous current through GND	±75	mA
T_{JMAX}	Maximum Junction Temperature	150	°C
P_D	Max Power Dissipation (TSSOP20)	400	mW
T_{STG}	Storage Temperature Range	-65 to 150	°C
V_{ESD}	Human Body Model ESD (JESD22-A114)	±2000	V
	Charged Device Model ESD (JESD22-C101)	±1000	
I_{LU}	Latch up Current Maximum Rating (JESD78E)	±250	mA

Note1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_I	Input Voltage	0	5.5	V
V_O	Output Voltage	0	V_{CC}	V
I_{OH}	High-level output current		-8	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating Temperature Range	-40	125	°C
$\Delta t/\Delta v$	Input Transition rise or fall rate		20	ns/V

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC}(V)	T_A=25°C			−40°C≤T_A≤125°C		Unit
				Min	Typ	Max	Min	Max	
V_{OH}	High−Level Output Voltage	I_{OH}=-50uA	4.5	4.4	4.5		4.4		V
		I_{OH}=-8mA		3.94			3.8		
V_{OL}	Low−Level Output Voltage	I_{OH}=-50uA	4.5			0.1		0.1	V
		I_{OH}=-8mA				0.36		0.44	
I_I	Input Leakage Current	V_I=5.5V or GND	0 to 5.5			±0.1		±1	uA
I_{OZ}	Output Leakage Current	Vo=V_{CC} or GND	5.5			±0.25		±2.5	
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	5.5			4		40	μA
△I_{CC}[(2)]	One Input at 3.4V, Other Inputs at V_{CC} or GND		5.5			1.35		1.5	mA
C_i	V_I=V_{CC} or GND		5.0		2	10		10	pF
C_O	Vo=V_{CC} or GND		5.0		4			10	

Note2: This is the increase in supply current for each input at one of the specified TTL voltage levels,rather than 0V or VCC

Switching Characteristics [(3)]

Symbol	Condition	T_A=25°C		−40°C≤T_A≤125°C			Unit
		Typ	Max	Min	Typ	Max	
t_{PLH}	From A to Y, C_L=15pF	4.1	6.0	1.0		6.5	ns
t_{PHL}		4.1	6.0	1.0		6.5	
t_{PZH}	From /OE to Y, C_L=15pF	5.0	7.0	1.0		8.0	
t_{PZL}		5.0	7.0	1.0		8.0	
t_{PHZ}	From /OE to Y, C_L=15pF	4.5	7.0	1.0		8.0	
t_{PLZ}		4.5	7.0	1.0		8.0	
t_{PLH}	From A to Y, C_L=50pF	6.2	8.5	1.0		9.5	
t_{PHL}		6.2	8.5	1.0		9.5	
t_{PZH}	From /OE to Y, C_L=50pF	7.5	10.0	1.0		12.0	
t_{PZL}		7.5	10.0	1.0		12.0	
t_{PHZ}	From /OE to Y, C_L=50pF	7.0	10.0	1.0		12.0	
t_{PLZ}		7.0	10.0	1.0		12.0	

Note3. Guaranteed by design and characterization. not a FT item.

AC Characteristics Test Waveform

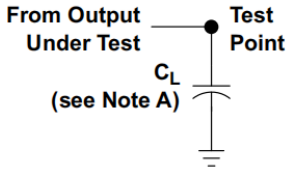
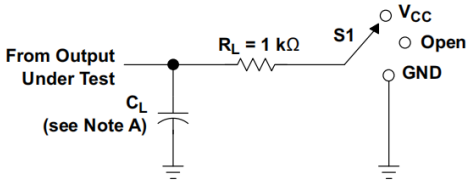


Figure 3. Load circuit for pole outputs



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

Figure 4. Load circuit for 3-state and open-drain outputs

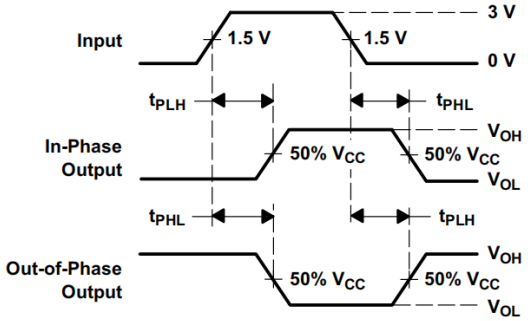


Figure 5. Voltage waveform propagation delay times inverting and noninverting outputs

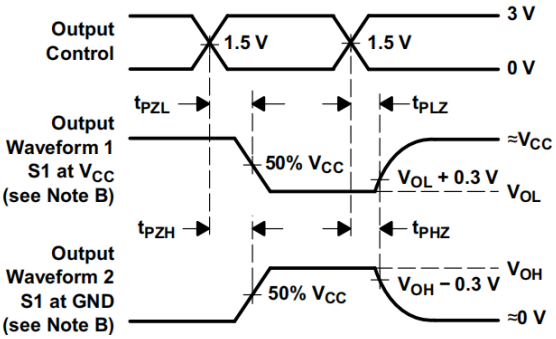


Figure 6. Voltage waveforms enable and disable times low-and high-level enabling

Note A: C_L includes probe and jig capacitance.

Note B: Figure 5 is for an output with internal conditions such that the output is low except when disable by the output control. Figure 6 is for an output with internal conditions such that the output is high except when disable by the output control.

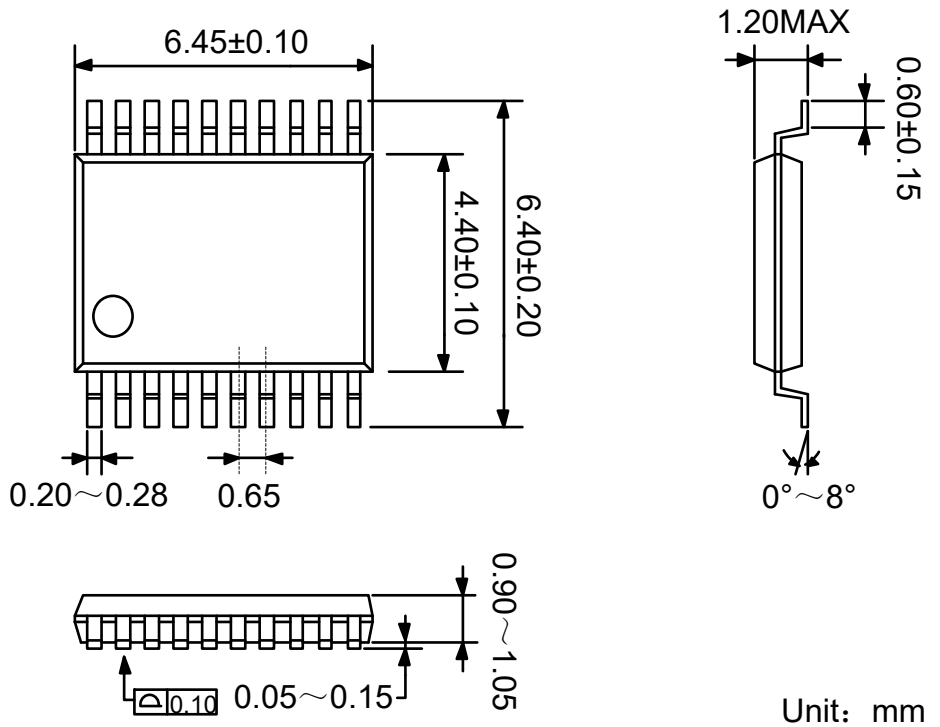
Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{PD}[(4)]	Power Dissipation Capacitance	1MHz,V_{CC}= 5.0 V, T_A=25°C,No load	12	pF

Note4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Package Dimension

TSSOP20



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2023-10-20	Initial version	Shibo	Luh	Liujy