8-Bit Serial or Parallel-Input/Serial-Output Shift Register

General Description

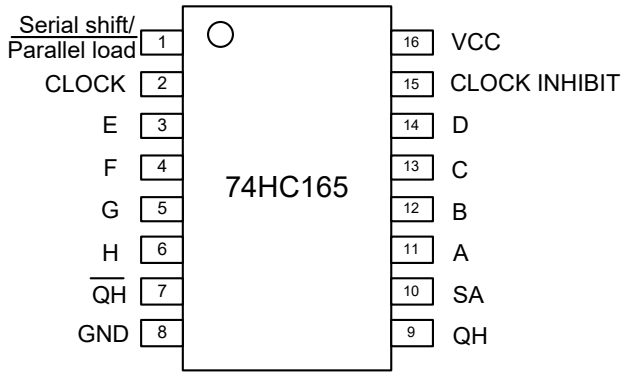
The 74HC165 is a high-performance silicon-gate CMOS 8-bit shift register. Data may be loaded into register either in parallel or in serial form. When the $\frac{\text{serial shift/}}{\text{parallel load}}$ input is low, the data is loaded asynchronously in parallel. When the $\frac{\text{serial shift/}}{\text{parallel load}}$ input is high, the data is loaded serially on the rising edge of either Clock or Clock Inhibit (see the Function Table).

The 74HC165 inputs are compatible with standard CMOS outputs, with pull-up resistors, they are compatible with LSTTL outputs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0V
- Low Input Current: 1uA
- High Noise Immunity Characteristic of CMOS Devices
- Pb-Free Packages: SOP16

Pin Configuration

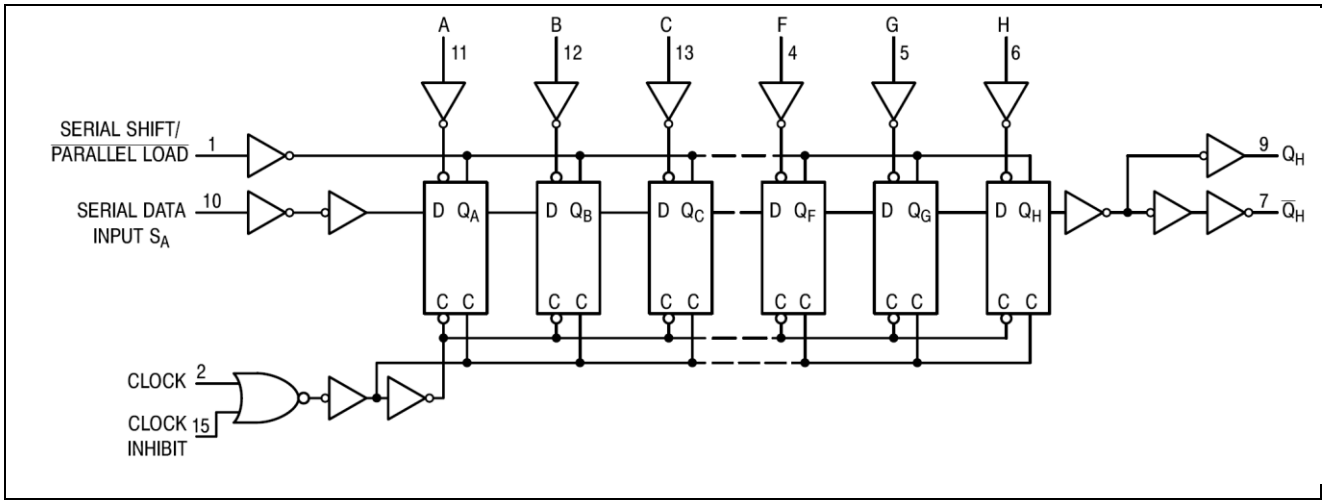


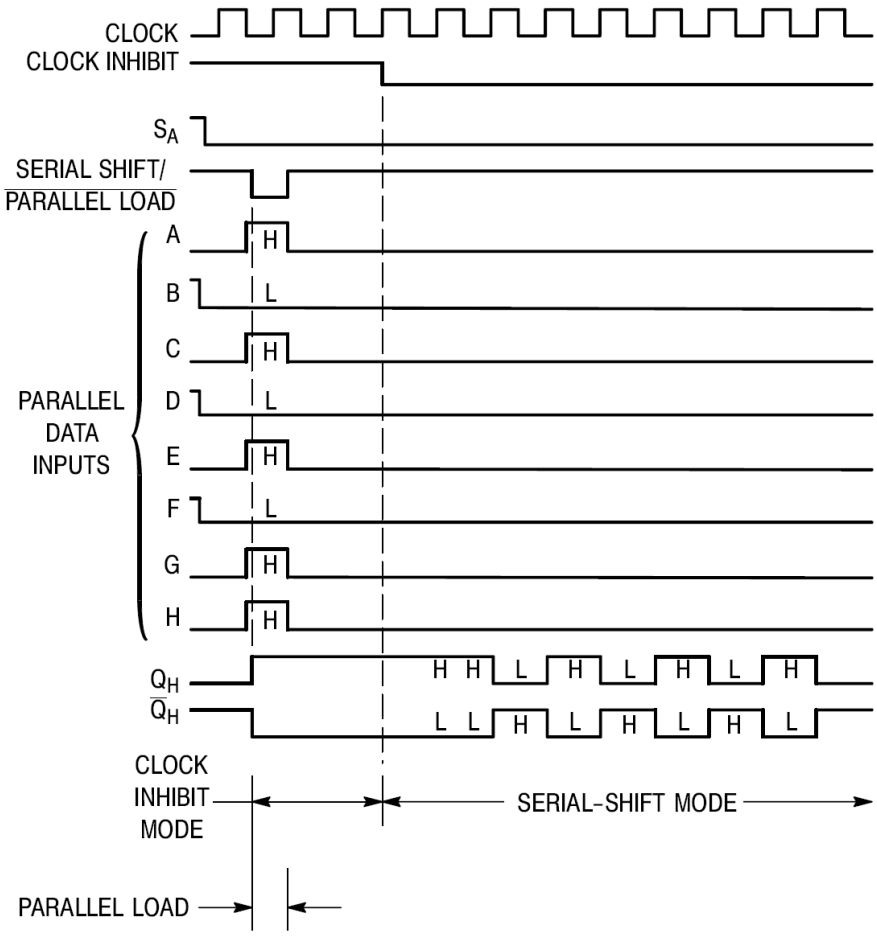
TOP VIEW

Pin Function

Pin Number	Pin Name	Description
1	serial shift/ parallel load	Data-entry control input.
2	CLOCK	Clock input.
3~6、11~14	A~H	8-bit parallel data inputs.
7	$\overline{QH}$	Shift register output (inverted).
8	GND	Ground.
9	QH	Shift register output (noninverted).
10	SA	Serial data input.
15	CLOCK INHIBIT	Clock input
16	VCC	Power supply.

Block Diagram





Timing Diagram

Functional Description

The 74HC165 is an 8-bit Serial or $\frac{\text{serial shift/}}{\text{parallel load}}$ shift register. The following is function table:

Inputs					Internal Stages		Output	Operation
$\overline{\text{Serial Shift/}}$ Parallel Load	Clock	Clock Inhibit	S_A	A-H	QA	QB	Q_H	
L	X	X	X	a…h	a	b	h	Asynchronous Parallel Load
H	↗	L	L	X	L	Q_{An}	Q_{Gn}	Serial Shift via Clock
H	↗	L	H	X	H	Q_{An}	Q_{Gn}	
H	L	↗	L	X	L	Q_{An}	Q_{Gn}	Serial Shift via Clock Inhibit
H	L	↗	H	X	H	Q_{An}	Q_{Gn}	
H	X	H	X	X	No Change			Inhibited Clock
H	H	X	X	X				
H	L	L	X	X	No Change			No Clock

X = don't care , Q_{An} − Q_{Gn} = Data shifted from the preceding stage.

Inputs

A，B，C，D，E，F，G，H (Pins 11,12,13,14,3,4,5,6)

Parallel Data inputs. Data on these inputs are asynchronously entered in parallel into the internal flip-flops when the Serial Shift/Parallel Load input is low.

SA (Pin 10)

Serial Data input. When the $\frac{\text{serial shift/}}{\text{parallel load}}$ input is high, data on this pin is serially entered into the first stage of the shift register with the rising edge of the Clock.

Control Inputs

$\frac{\text{serial shift/}}{\text{parallel load}}$ **(Pin 1)**

Data-entry control input. When a high level is applied to this pin, data at the Serial Data input(SA) are shifted into the register with the rising edge of the Clock. When a low level is applied to this pin, data at the Parallel Data inputs are asynchronously loaded into each of the eight internal stages.

Clock，Clock Inhibit (Pins 2,15)

Clock Inputs.These two clock inputs function identically. Either may be used as an active-high clock inhibit. However, to avoid double clocking, the inhibit input should go high only while the clock input is high.

The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

Outputs

QH，$\overline{\text{QH}}$ (Pins 9,7)

Complementary Shift Register outputs. These pins are the noninverted and inverted outputs of the eighth stage of the shift register.

Maximum Ratings

Parameter	Value	Unit
DC Supply Voltage V_{CC}	-0.5~7	V
DC Input Voltage V_{IN}	-0.5~VCC+0.5	V
DC Output Voltage V_{OUT}	-0.5~VCC+0.5	V
DC Input Current, per pin I_{IN}	±20	mA
DC Output Current, per pin I_{OUT}	±25	mA
DC Supply Current, VCC and GND Pins I_{CC}	±50	mA
Power Dissipation P_D	750	mW
Storage Temperature T_{STG}	-65~150	℃

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}	DC Input Voltage, Output Voltage(Referenced to GND)	0	V_{CC}	V
V_{OUT}	DC Input Voltage, Output Voltage(Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-40	+125	°C
tr,tf	Input Rise and Fall Time (Figure 1) V_{CC}=2.0V V_{CC}=3.0V V_{CC}=4.5V V_{CC}=6.0V	 0 0 0 -	 1000 600 500 400	ns

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				-40~25°C	≤85°C	≤125°C	
Minimum High-Level Input Voltage	V_{IH}	V_{OUT}=0.1V or V_{CC}-0.1V，$\|I_{OUT}\|$≤20uA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
Maximum Low-Level Input Voltage	V_{IL}	V_{OUT}=0.1V or V_{CC}-0.1V $\|I_{OUT}\|$≤20uA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}, $\|I_{OUT}\|$≤20uA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}=V_{IH} or V_{IL}, $\|I_{OUT}\|$≤2.4mA, $\|I_{OUT}\|$≤4.0mA, $\|I_{OUT}\|$≤5.2mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}, $\|I_{OUT}\|$≤20uA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}=V_{IH} or V_{IL}， $\|I_{OUT}\|$≤2.4mA, $\|I_{OUT}\|$≤4.0mA, $\|I_{OUT}\|$≤5.2mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
Maximum Input leakage Current	I_{IN}	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	uA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND， I_{OUT}=0uA	6.0	4	40	160	uA

AC Electrical Characteristics (CL = 50 pF, Input tr = tf = 6 ns)

Parameter	Symbol	V_{CC} V	Guaranteed Limit			Unit
			-40~25°C	≤85°C	≤125°C	
Maximum Clock Frequency(50% Duty Cycle) (Figures 1 and 8)	f_{max}	2.0	6	4.8	4	MHz
		3.0	18	17	15	
		4.5	30	24	20	
		6.0	35	28	24	
Maximum Propagation Delay, Clock (or Clock Inhibit) to Q_H or $\overline{QH}$ (Figures 1 and 8)	t_{PLH}, t_{PHL}	2.0	150	190	225	ns
		3.0	52	63	65	
		4.5	30	38	45	
		6.0	26	33	38	
Maximum Propagation Delay, serial shift/parallel load to Q_H or $\overline{QH}$ (Figures 2 and 8)	t_{PLH}, t_{PHL}	2.0	175	220	265	ns
		3.0	58	70	72	
		4.5	35	44	53	
		6.0	30	37	45	
Maximum Propagation Delay, Input H to Q_H or $\overline{QH}$ (Figures 3 and 8)	t_{PLH}, t_{PHL}	2.0	150	190	225	ns
		3.0	52	63	65	
		4.5	30	38	45	
		6.0	26	33	38	
Maximum Output Transition Time, Any Output(Figures 1 and 8)	t_{TLH}, t_{THL}	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
Maximum Input Capacitance	C_{in}	-	10	10	10	pF

Timing Requirements（Input tr=tf=6ns）

Parameter	Symbol	V_{CC}V	Guaranteed Limit			Unit
			-40~25°C	≤85°C	≤125°C	
Minimum Setup Time, Parallel Date Inputs to serial shift/parallel load (Figure 4)	t_{su}	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
Minimum Setup Time,Input SA to Clock (or Clock Inhibit) (Figure 5)	t_{su}	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
Minimum Setup Time, serial shift/parallel load to Clock (or Clock Inhibit) (Figure 6)	t_{su}	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
Minimum Setup Time, Clock to Clock Inhibit (Figure 7)	t_{su}	2.0	75	95	110	ns
		3.0	30	40	55	

		4.5 6.0	15 13	19 16	22 19	
Minimum Hold Time, $\frac{\text{serial shift/}}{\text{parallel load}}$ to Parallel Data Inputs (Figure 4)	t_h	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
Minimum Hold Time, Clock (or Clock Inhibit) to Input SA (Figure 5)	t_h	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
Minimum Hold Time, Clock (or Clock Inhibit) to $\frac{\text{serial shift/}}{\text{parallel load}}$ (Figure 6)	t_h	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
Minimum Recovery Time, Clock to Clock Inhibit (Figure 7)	t_{rec}	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
Minimum Pulse Width, Clock (or Clock Inhibit) (Figure 1)	t_w	2.0 3.0 4.5 6.0	70 27 15 13	90 32 19 16	100 36 22 19	ns
Minimum Pulse Width, ($\frac{\text{serial shift/}}{\text{parallel load}}$ Figure 2)	t_w	2.0 3.0 4.5 6.0	70 27 15 13	90 32 19 16	100 36 22 19	ns
Maximum Input Rise and Fall Times (Figure 1)	t_r, t_f	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

Switching Waveforms

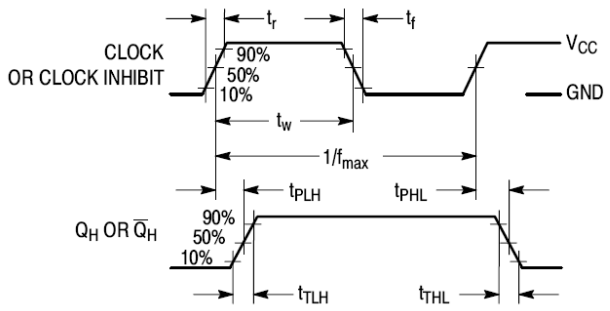


Figure 1、Serial-Shift Mode

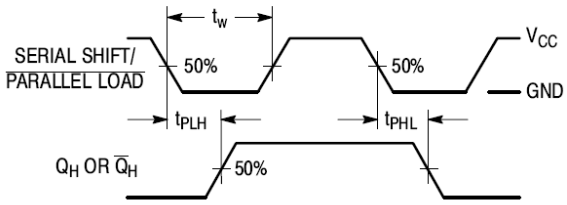


Figure 2、Parallel-Load Mode

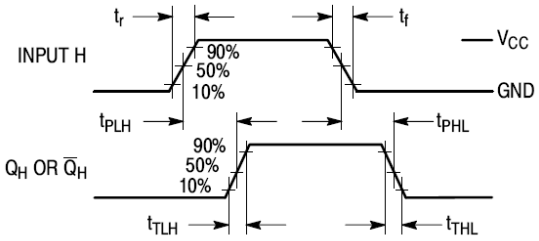


Figure 3、Parallel-Load Mode

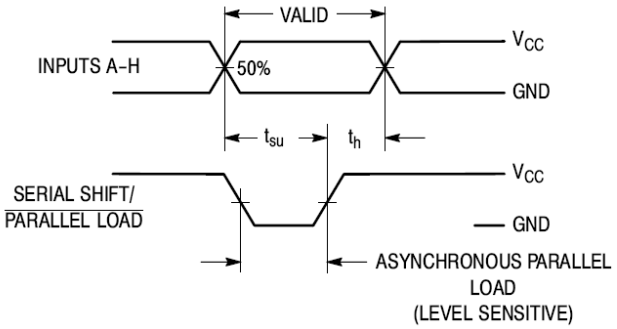


Figure 4、Parallel-Load Mode

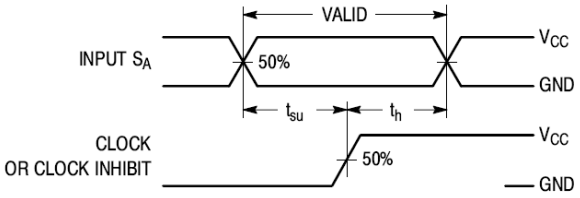


Figure 5、Serial-Shift Mode

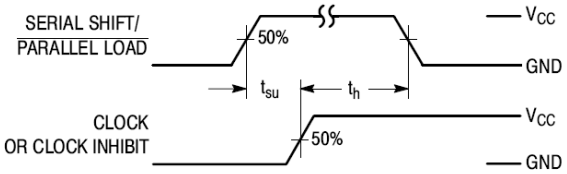


Figure 6、Serial-Shift Mode

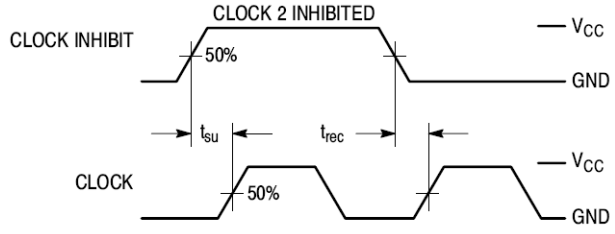


Figure 7、Serial-Shift，Clock Inhibit Mode

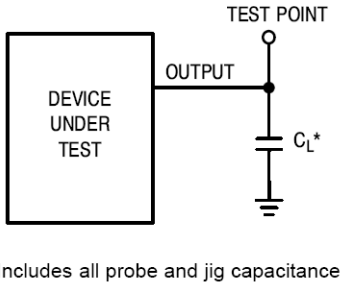


Figure 8、Test Circuit

Package Dimension