8-bit Parallel-out Serial Shift Registers

General Description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear $\overline{CLR}$ input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop.

Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

Features

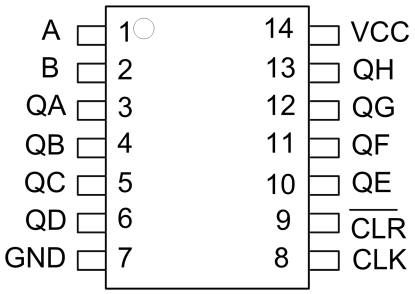
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Product name and package

Product Name	Package
74HC164M	SOP14
74HC164V	TSSOP14

Applications

- Memory chip select decoding
- Data transmission system

Pin Configuration



74HC164M/V
TOP VIEW

Pin Function

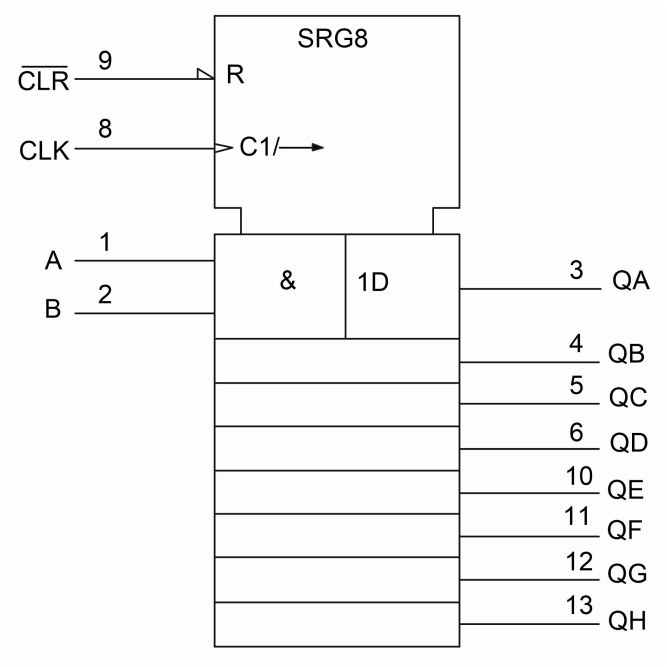
Input Pin				Output Pin			
$\overline{CLR}$	CLK	A	B	QA	QB	…	QH
L	X	X	X	L	L		L
H	L	X	X	QA0	QB0		QH0
H	↑	H	H	H	QAn		QGn
H	↑	L	X	L	QAn		QGn
H	↑	X	L	L	QAn		QGn

Notes:

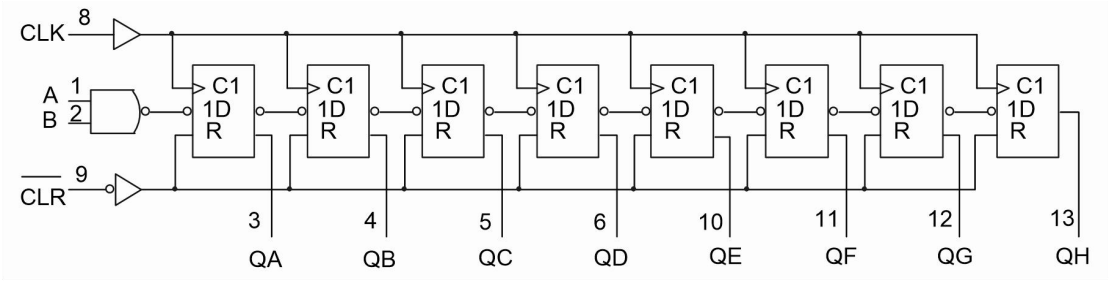
- QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.
- QAn, QGn = the level of QA or QG before the most recent↑transition of CLK: indicates a 1-bit shift.

Block Diagram

Logic symbol

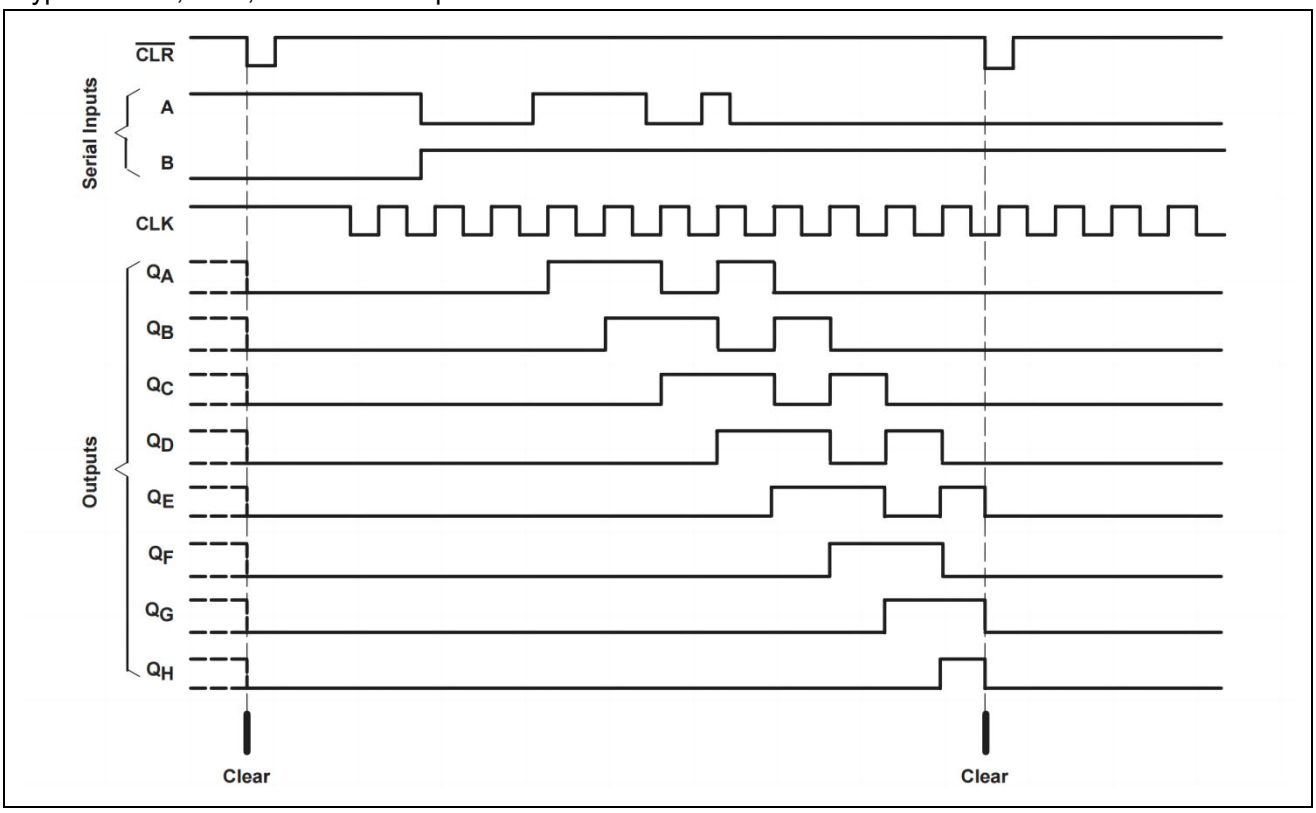


Logic Diagram



Functions Description

Typical Clear, Shift, and Clear Sequence



Absolute Maximum Ratings

Parameter	Symbol		Rating	Unit
Supply voltage[1]	V_{CC}		-0.5 ～ 7.0	V
Input clamp current	I_{IK}		±20	mA
Output clamp current	I_{OK}		±20	mA
Continuous output current	I_O		±25	mA
Continuous current through VCC or GND	I_{CC}		±50	mA
Package thermal impedance[2]	θ_{JA}	SOP14	125	°C/W
		TSSOP14	140	°C/W
Storage temperature	T_{STG}		-65 ～150	°C

Notes:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

Recommended operating conditions

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Supply voltage	V_{CC}		2	5	6	V
High-level input voltage	V_{IH}	V_{CC} =2V	1.5			V
		V_{CC} =4.5V	3.15			
		V_{CC} =6V	4.2			
Low-level input voltage	V_{IL}	V_{CC} =2V	0		0.5	V
		V_{CC} =4.5V	0		1.35	
		V_{CC} =6V	0		1.8	
Input voltage	V_I		0		V_{CC}	V
Output voltage	V_O		0		V_{CC}	V
Input transition (rise and fall) time	t_t	V_{CC} =2V	0		1000	ns
		V_{CC} =4.5V	0		500	
		V_{CC} =6V	0		400	
Operating free-air temperature	T_A		-40		85	°C

Note:

If this device is used in the threshold region (from V_{IL_MAX} = 0.5V to V_{IH_MIN} = 1.5V), there is a potential to go into the wrong state from induced grounding, causing double clocking.

Operating with the inputs at tt = 1000ns and V_{CC} = 2V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

Electrical Characteristics

Symbol	Test Condition		V_{CC}	T_A=25°C			T_A = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{OH}	V_I = V_{IH} or V_{OH}	I_{OH} =20μA	2V	1.9	1.998		1.9		V
			4.5V	4.4	4.499		4.4		
			6V	5.9	5.999		5.9		
		I_{OH} =-4mA	4.5V	3.98	4.3		3.84		
		I_{OH} =-5.2mA	6V	5.48	5.8		5.34		
V_{OL}	V_I = V_{IH} or V_{OH}	I_{OL} =20μA	2V		0.002	0.1		0.1	V
			4.5V		0.001	0.1		0.1	
			6V		0.001	0.1		0.1	
		I_{OL} =4mA	4.5V		0.17	0.26		0.33	
		I_{OL} =5.2mA	6V		0.15	0.26		0.33	
I_I	V_I = V_{CC} or 0		6V		±0.1	±100		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O =0		6V			8		80	μA
C_I			2V to 6V		3	10		10	pF

Timing Characteristics

Symbol	Characteristic		V_{CC}	T_A=25°C		T_A = -40°C to +85°C		Unit
				Min	Max	Min	Max	
F_{CLOCK}	Clock frequency		2V	0	6	0	5	MHz
			4.5V	0	31	0	25	
			6V	0	36	0	28	
t_W	Pulse duration	$\overline{CLR}$ low	2V	100		125		ns
			4.5V	20		25		
			6V	17		21		
		CLK high or low	2V	80		100		
			4.5V	16		20		
			6V	14		18		
t_{SU}	Setup time before CLK	Data	2V	100		125		ns
			4.5V	20		25		
			6V	17		21		
I_{CC}		$\overline{CLR}$ inactive	2V	100		125		
			4.5V	20		25		
			6V	17		21		
t_h	Hold time, data after CLK		2V	5		5		ns
			4.5V	5		5		
			6V	5		5		

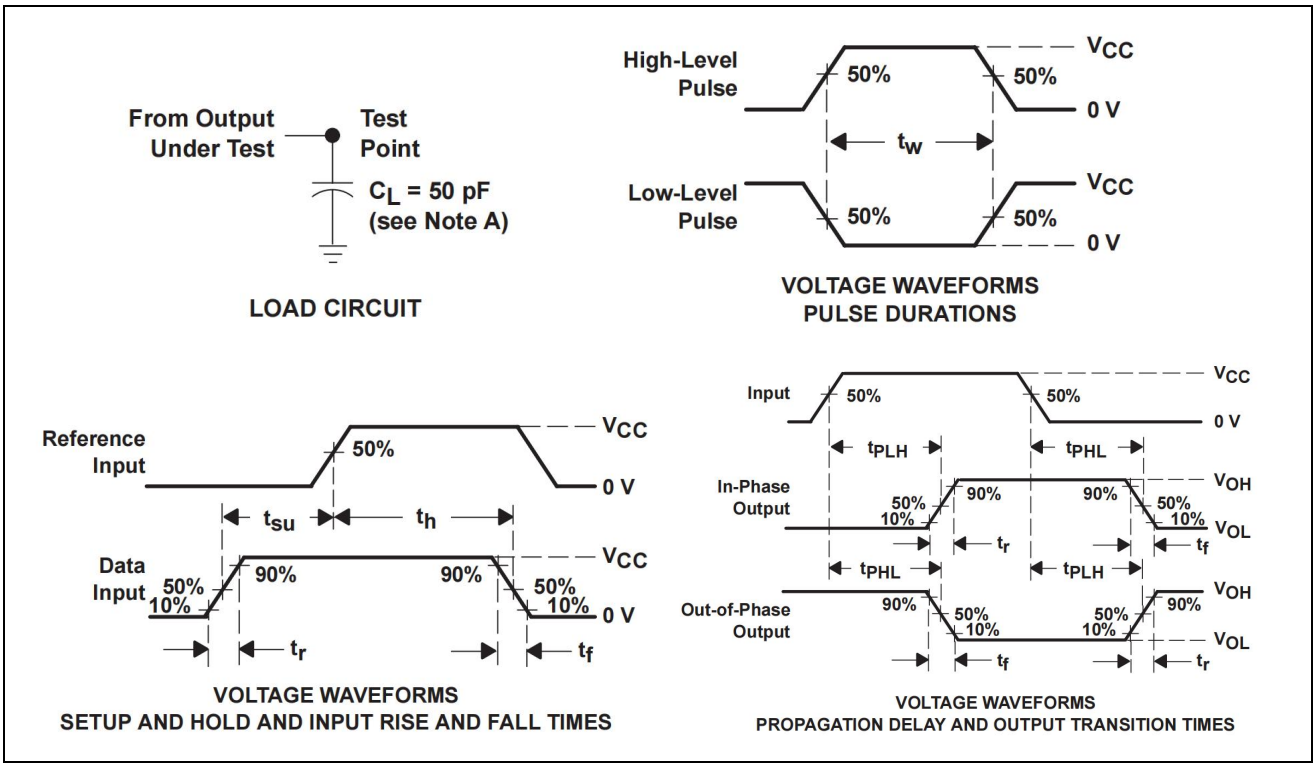
Switching characteristics (CL = 50pF)

Symbol	From (Input)	To (Output)	V_{CC}	T_A=25℃			T_A = -40℃ to +85℃		Unit
				Min	Typ	Max	Min	Max	
F_{MAX}			2V	6	10		5		MHz
			4.5V	31	54		25		
			6V	36	62		28		
t_{PHL}	$\overline{CLR}$	Any Q	2V		140	205		255	ns
			4.5V		28	41		51	
			6V		24	35		46	
t_{pd}	CLK	Any Q	2V		115	175		220	
			4.5V		23	35		44	
			6V		20	30		38	
t_t			2V		38	75		95	ns
			4.5V		8	15		19	
			6V		6	13		16	

Operating characteristics (T_A=25°C)

Symbol	Characteristic	Test Conditions	Typ	Unit
C_{pd}	Power dissipation capacitance	No Load	135	pF

Parameter Measurement Information

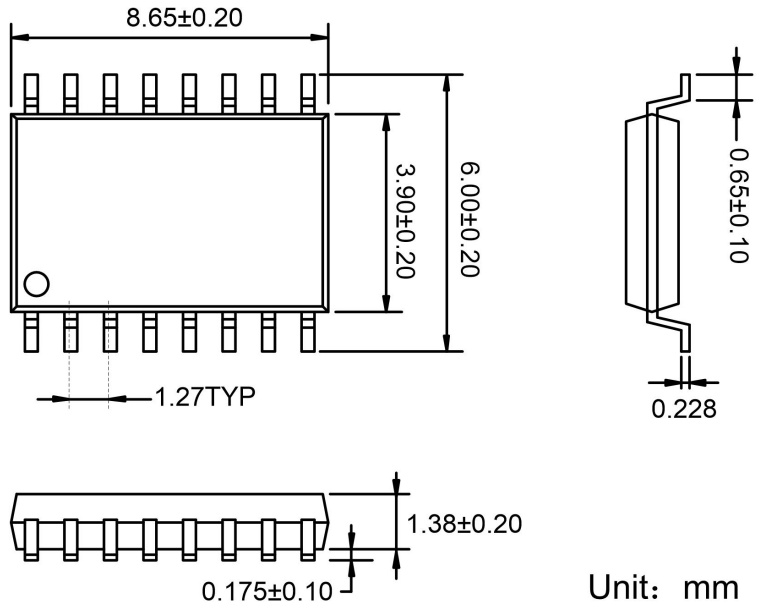


Note:

When using the circuit, in order to strengthen the anti-jamming ability,a capacitor of 100pF should be connected between the $\overline{CLR}$ and VCC or GND .

Package Dimension

SOP14



TSSOP14