Single D-type Flip-Flop with Reset; Positive-Edge Trigger

General Description

The ET74LVC1G175 is a low-power, low-voltage single positive edge triggered D-type flip-flop with individual data (D) input, clock (CP) input, master reset ($\overline{MR}$) input, and Q output.

The master reset ($\overline{MR}$) is an asynchronous active LOW input and operates independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device in a mixed 3.3V and 5V environment.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging back-flow current through the device when it is powered down.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

Features

- Wide Supply Voltage Range from 1.65V to 5.5V
- 5V Tolerant Inputs for Interfacing with 5V Logic
- High Noise Immunity
- ±24mA Output Drive (V_{CC} = 3.0V)
- CMOS Low Power Consumption
- I_{OFF} Circuitry Provides Partial Power-down Mode Operation
- Direct Interface with TTL Levels
- Inputs Accept Voltages up to 5V
- Multiple Package Options
- ESD Protection Exceeds JESD22
  - 4000V Human-Body Model (A114-A)
  - 1500V Charged-Device Model (C101)
- Latch-up Performance Exceeds 200mA per JESD78, Class II

Applications

- Server
- LED Display Screen
- Network Switches
- Telecommunications Infrastructure
- Motor Driver
- I/O Extender

Ordering Information

Part No.	Package	MSL
ET74LVC1G175	SC70-6	3
ET74LVC1G175T	SOT23-6	3

Pin Configuration

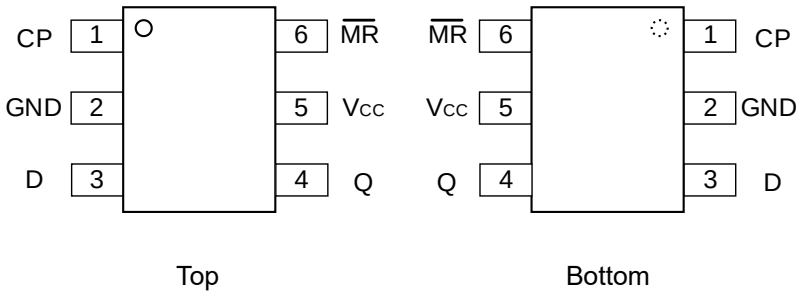


Fig 1. Top View & Bottom View

Pin Function

Pin No.	Pin Name	Pin Function
1	CP	Clock Input (Low-to-High, Edge-Triggered)
2	GND	Ground
3	D	Data Input
4	Q	Flip-Flop Output
5	V_{CC}	Supply Voltage
6	$\overline{MR}$	Master Reset Input (Active LOW)

Functional Diagram

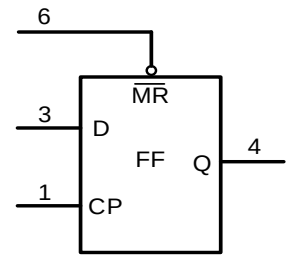


Fig 2. Logic Symbol

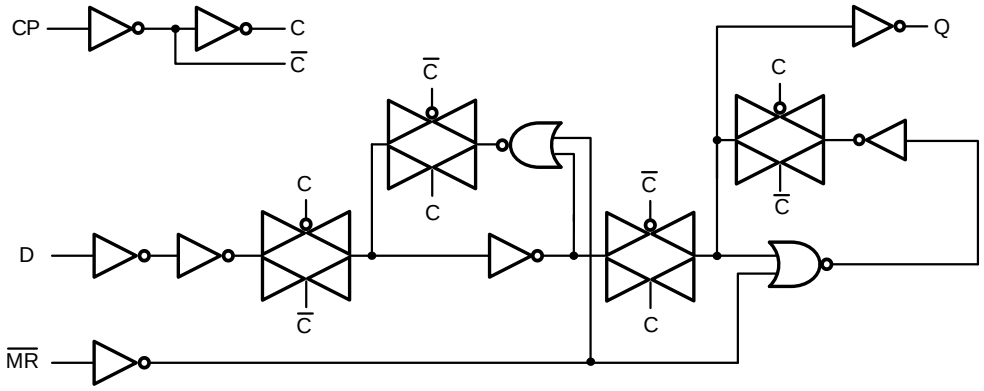


Fig 3. Logic Diagram

Functional Description

Table 1. Function Table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
↑ = LOW-to-HIGH CP transition; X = don't care.

Operating Mode	Input			Output
	$\overline{MR}$	CP	D	Q
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage		-0.5~+6.5	V
I_{IK}	Input Clamping Current	V_I < 0V	-50	mA
V_I	Input Voltage (1)		-0.5~+6.5	V
I_{OK}	Output Clamping Current	V_O > V_{CC} or V_O < 0V	±50	mA
V_O	Output Voltage	Active Mode (1)	-0.5~V_{CC} + 0.5	V
		Power-Down Mode (1)	-0.5~+6.5	V
I_O	Output Current	V_O = 0V to V_{CC}	±50	mA
I_{CC}	Supply Current		+100	mA
I_{GND}	Ground Current		-100	mA
T_J	Operating Junction Range		-40 to +150	°C
T_{STG}	Storage Temperature		-65 to +150	°C
V_{ESD}	Human Body Mode (2)		±4000	V
	Charged Device Mode (3)		±1500	V
I_{LU}	Latch-up Current (4)		±200	mA

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per EIA/JESD22-A114−A;

Note3: CDM tested per EIA/JESD22-C101;

Note4: Latch-up Current Maximum Rating tested per EIA/JESD78E;

Recommended Operating Conditions

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage		1.65~5.5	V
V_I	Input Voltage		0~5.5	V
V_O	Output Voltage	Active Mode	0~V_{CC}	V
		Power-Down Mode V_{CC}=0V	0~5.5	V
T_A	Ambient Temperature		-40 to +125	°C
Δt/ΔV	Input Transition Rise and Fall Rate	V_{CC} = 1.65V to 2.7V	<20	ns/V
		V_{CC} = 2.7V to 5.5V	<10	ns/V

Electrical Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions	−40°C ≤ T_A ≤ +85°C			−40°C ≤ T_A ≤ +125°C		Unit
			Min	Typ [5]	Max	Min	Max	
V_{IH}	High−Level Input Voltage	V_{CC} = 1.65V to 1.95V	0.65V_{CC}			0.65V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7			1.7		
		V_{CC} = 2.7V to 3.6V	2.0			2.0		
		V_{cc} = 4.5V to 5.5V	0.7V_{CC}			0.7V_{CC}		
V_{IL}	Low−Level Input Voltage	V_{CC} = 1.65V to 1.95V			0.35V_{CC}		0.35V_{CC}	V
		V_{CC} = 2.3V to 2.7V			0.7		0.7	
		V_{CC} = 2.7V to 3.6V			0.8		0.8	
		V_{cc} = 4.5V to 5.5V			0.3V_{CC}		0.3V_{CC}	
V_{OH}	High-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_O = -100μA; V_{CC} = 1.65V to 5.5V	V_{CC} - 0.1			V_{CC} - 0.1		
		I_O = -4mA; V_{CC} = 1.65V	1.2	1.54		0.95		
		I_O = -8mA; V_{CC} = 2.3V	1.9	2.15		1.7		
		I_O = -12mA; V_{CC} = 2.7V	2.2	2.5		1.9		
		I_O = -24mA; V_{CC} = 3.0V	2.3	2.62		2.0		
		I_O = -32mA; V_{CC} = 4.5V	3.8	4.11		3.4		
V_{OL}	Low-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_O = -100μA; V_{CC} = 1.65V to 5.5V			0.10		0.10	
		I_O = 4mA; V_{CC} = 1.65V		0.07	0.45		0.70	
		I_O = 8mA; V_{CC} = 2.3V		0.09	0.30		0.45	
		I_O = 12mA; V_{CC} = 2.7V		0.16	0.40		0.60	
		I_O = 24mA; V_{CC} = 3.0V		0.17	0.55		0.80	
		I_O = 32mA; V_{CC} = 4.5V		0.18	0.55		0.80	
I_I	Input Leakage Current	V_I = 5.5V or GND; V_{CC} = 0V to 5.5V		±0.1	±5		±20	uA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V; V_{CC} = 0V		±0.1	±10		±20	uA
I_{CC}	Supply Current	V_I = 5.5V or GND; V_{CC} = 1.65V to 5.5V; I_O = 0A		0.1	10		40	uA
ΔI_{CC}	Additional Supply Current	V_I = V_{CC} - 0.6V; I_O = 0A; V_{CC} = 2.3V to 5.5V		5	500		5000	uA
C_I	Input Capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3V		4.5				pF

Dynamic Characteristics

Voltages are referenced to GND (ground = 0V); for test circuit see Fig.6.

Symbol	Parameter	Conditions	−40°C ≤ T_A ≤ +85°C			−40°C ≤ T_A ≤ +125°C		Unit
			Min	Typ[5]	Max	Min	Max	
t_{pd}	Propagation Delay	CP to Q; See Fig.4						ns
		V_{CC} = 1.65V to 1.95V	1.5	7.2	13.4	1.5	17	
		V_{CC} = 2.3V to 2.7V	1.0	4.2	7.1	1.0	9.0	
		V_{CC} = 2.7V	1.0	3.9	7.1	1.0	9.0	
		V_{CC} = 3.0V to 3.6V	1.0	3.8	5.7	0.5	7.5	
		V_{CC} = 4.5V to 5.5V	1.0	2.6	4.0	0.5	5.5	
		$\overline{MR}$ to Q; See Fig.5						
		V_{CC} = 1.65V to 1.95V	1.5	6.0	12.9	1.5	17	
		V_{CC} = 2.3V to 2.7V	1.0	3.6	7.0	1.0	9.0	
		V_{CC} = 2.7V	1.0	3.6	7.0	1.0	9.0	
		V_{CC} = 3.0V to 3.6V	1.0	3.0	5.8	0.5	7.5	
		V_{CC} = 4.5V to 5.5V	1.0	2.5	4.1	0.5	5.5	
t_W	Pulse Width	CP H or L; See Fig.4						ns
		V_{CC} = 1.65V to 1.95V	6.2			6.2		
		V_{CC} = 2.3V to 2.7V	2.7			2.7		
		V_{CC} = 2.7V	2.7			2.7		
		V_{CC} = 3.0V to 3.6V	2.7			2.7		
		V_{CC} = 4.5V to 5.5V	2.0			2.0		
		$\overline{MR}$ Low; See Fig.5						
		V_{CC} = 1.65V to 1.95V	6.2			6.2		
		V_{CC} = 2.3V to 2.7V	2.7			2.7		
		V_{CC} = 2.7V	2.7			2.7		
		V_{CC} = 3.0V to 3.6V	2.7			2.7		
		V_{CC} = 4.5V to 5.5V	2.0			2.0		
t_{rec}	Recovery Time	$\overline{MR}$; See Fig.5						ns
		V_{CC} = 1.65V to 1.95V	1.9			1.9		
		V_{CC} = 2.3V to 2.7V	1.4			1.4		
		V_{CC} = 2.7V	1.3			1.3		
		V_{CC} = 3.0V to 3.6V	1.2			1.2		
		V_{CC} = 4.5V to 5.5V	1.0			1.0		
t_{su}	Set-up Time	D to CP; See Fig.4						ns
		V_{CC} = 1.65V to 1.95V	2.9			2.9		
		V_{CC} = 2.3V to 2.7V	1.7			1.7		
		V_{CC} = 2.7V	1.7			1.7		
		V_{CC} = 3.0V to 3.6V	1.3			1.3		
		V_{CC} = 4.5V to 5.5V	1.1			1.1		

Dynamic Characteristics (Continued)

Voltages are referenced to GND (ground = 0V); for test circuit see Fig.6; for wave forms see Fig.4 and Fig.5.

Symbol	Parameter	Conditions	−40°C ≤ T_A ≤ +85°C			−40°C ≤ T_A ≤ +125°C		Unit
			Min	Typ[5]	Max	Min	Max	
t_h	Hold time	D to CP; See Fig.4						ns
		V_{CC} = 1.65V to 1.95V	0.0			0.0		
		V_{CC} = 2.3V to 2.7V	0.3			0.3		
		V_{CC} = 2.7V	0.5			0.5		
		V_{CC} = 3.0V to 3.6V	1.2			1.2		
		V_{CC} = 4.5V to 5.5V	0.5			0.5		
f_{max}	Maximum Frequency	D; See Fig.4						MHz
		V_{CC} = 1.65V to 1.95V	80	125		80		
		V_{CC} = 2.3V to 2.7V	175			175		
		V_{CC} = 2.7V	175			175		
		V_{CC} = 3.0V to 3.6V	175			175		
		V_{CC} = 4.5V to 5.5V	200			200		
C_{PD} [6]	Power Dissipation Capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3V		19				pF

Note5: All typical values are measured at T_A = 25°C and V_{CC} = 3.3V.

Note6: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = Input Frequency in MHz;

f_o = Output Frequency in MHz;

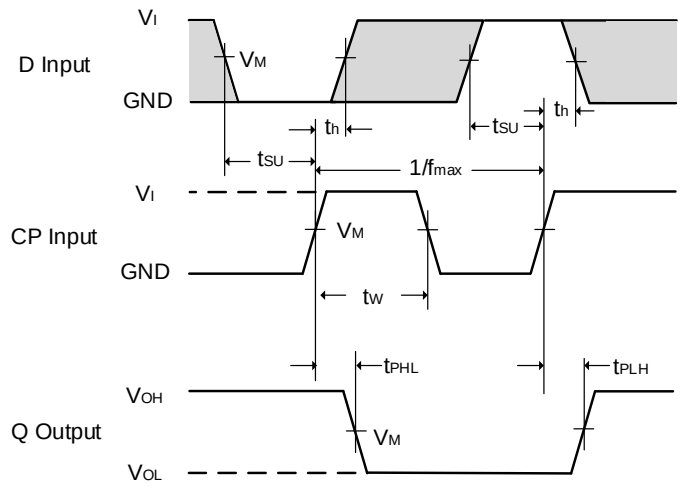
C_L = Output Load capacitance in pF;

V_{CC} = Supply Voltage in V;

N = Number of Inputs Switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of Outputs.

Test Circuit

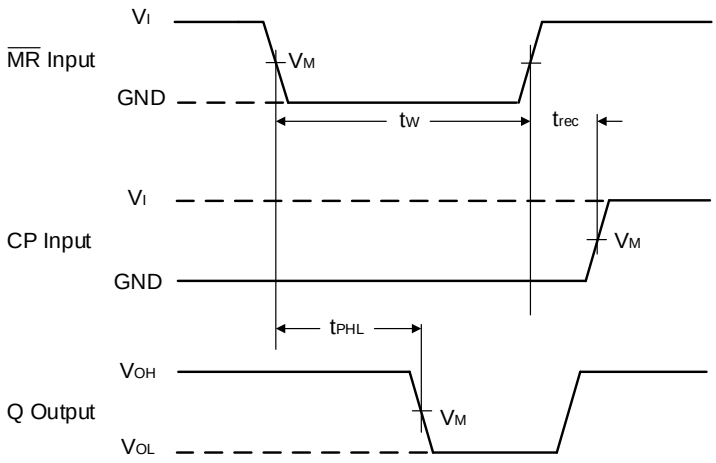


Measurement points are given in Table 3.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig.4 The clock input (CP) to output (Q) propagation delays, the clock pulse width,
D to CP set-up,CP to D hold times, and the maximum clock pulse frequency



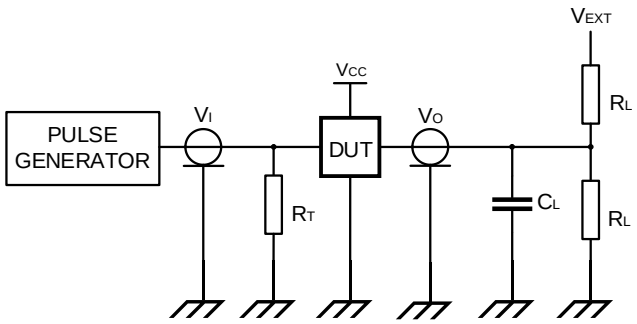
Measurement points are given in Table 3.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig.5 The master reset ($\overline{MR}$) input to output (Q) propagation delays,
the master reset pulse widths, and the $\overline{MR}$ to CP recovery time

Table 3.Measurement Points

Supply Voltage	Input	Output
V_{CC}	V_M	V_M
1.65V to 1.95V	0.5 × V_{CC}	0.5 × V_{CC}
2.3V to 2.7V	0.5 × V_{CC}	0.5 × V_{CC}
2.7V	1.5V	1.5V
3.0V to 3.6V	1.5V	1.5V
4.5V to 5.5V	0.5 × V_{CC}	0.5 × V_{CC}



Measurement points are given in Table 4.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig.6 Load circuit for switching times

Table 4.Test Data

Supply Voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r,t_f	C_L	R_L	t_{PLH},t_{PHL}
1.65V to 1.95V	V_{CC}	≤ 2.0ns	30pF	1kΩ	Open
2.3V to 2.7V	V_{CC}	≤ 2.0ns	30pF	500Ω	Open
2.7V	2.7V	≤ 2.5ns	50pF	500Ω	Open
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω	Open
4.5V to 5.5V	V_{CC}	≤ 2.5ns	50pF	500Ω	Open

Layout Guide

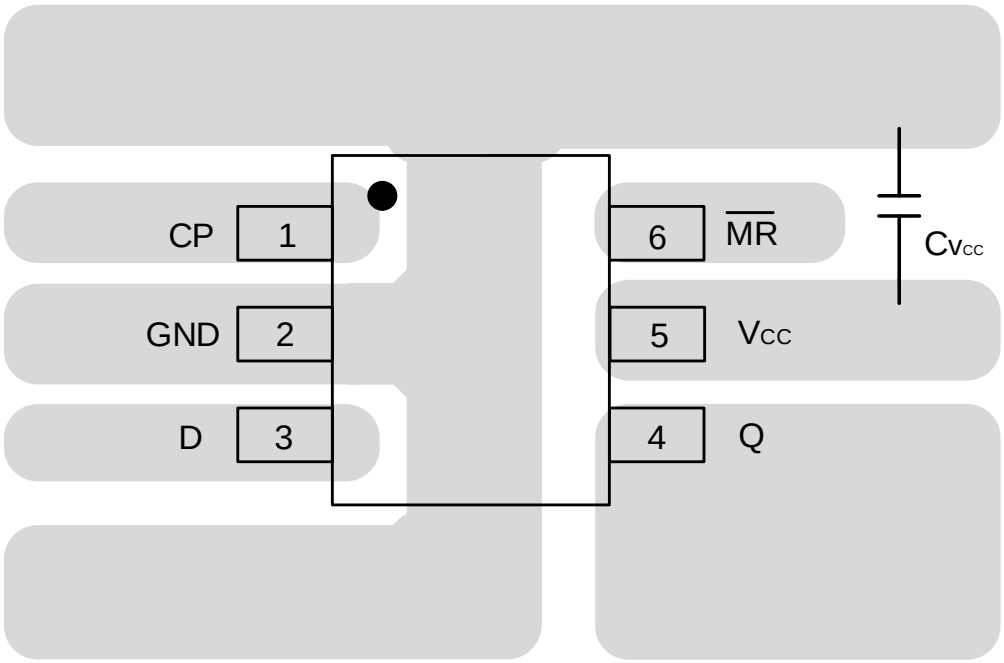
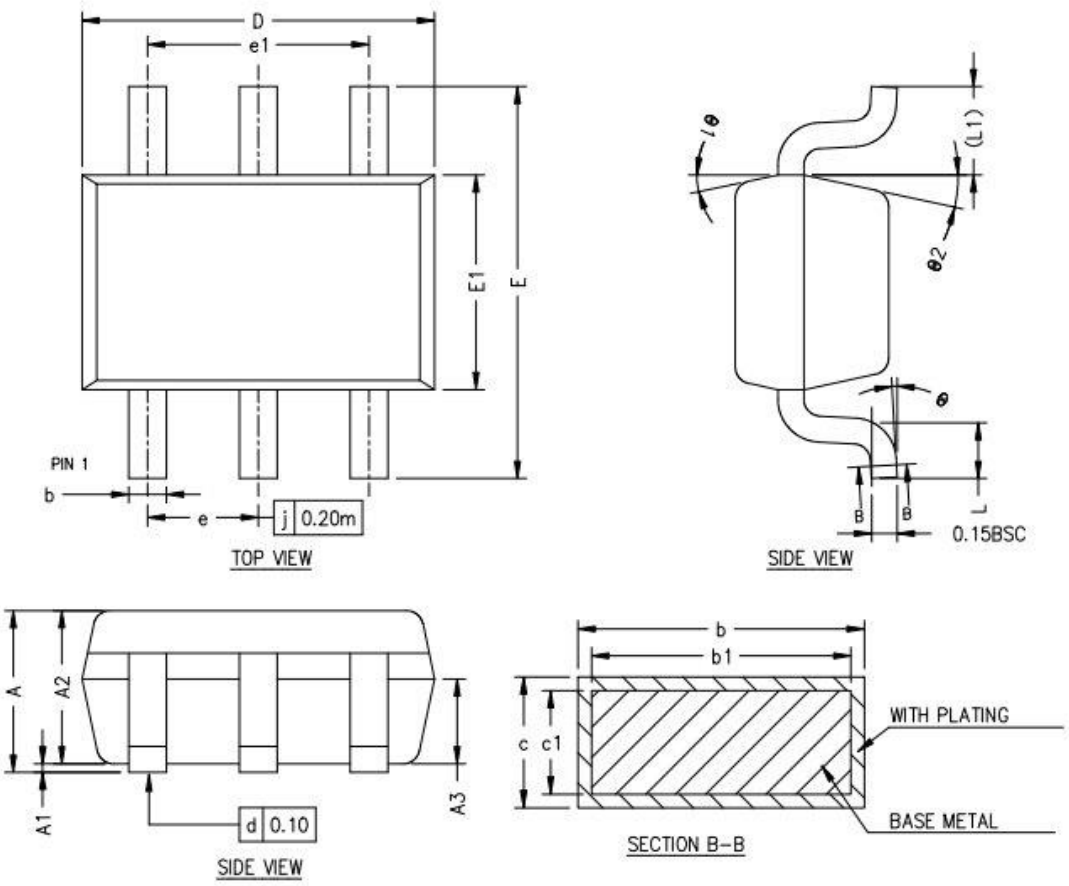


Fig.7 Layout Guide

Package Dimension

SC70-6 (2.00×1.25)



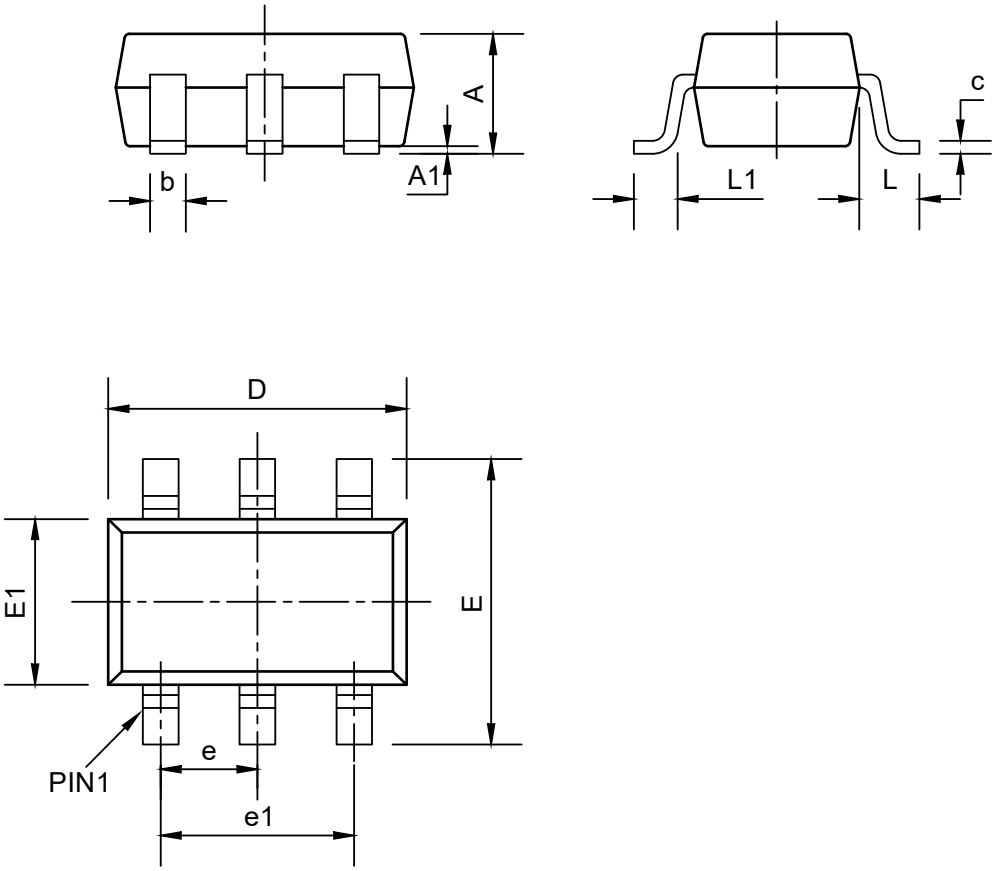
COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	0.80	--	1.10	E	2.20	2.30	2.40
A_1	0.	--	0.10	E_1	1.21	1.26	1.31
A_2	0.80	0.90	1.00	e	0.60	0.65	0.70
A_3	0.40	0.50	0.60	e_1	1.20	1.30	1.40
b	0.17	--	0.30	L	0.26	0.33	0.46
b_1	0.17	0.22	0.25	L_1	0.52RFF		
c	0.12	--	0.25	θ	0°	--	8°
c_1	0.12	0.15	0.16	θ_1	10°	12°	14°
D	2.02	2.07	2.12	θ_2	10°	12°	14°

Note7: . Plastic or metal protrusions of 0.2 mm maximum per side are not included.

SOT23-6 (2.90×1.50)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.90	--	1.10
A_1	0.013	--	0.10
b	0.25	--	0.40
c	0.10	--	0.26
D	2.70	--	3.10
e	--	0.95	--
e_1	--	1.90	--
E	2.50	--	3.00
E_1	1.30	--	1.70
L	0.60	--	0.65
L_1	0.20	--	0.60
Q	0.23	--	0.33

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-08-14	Preliminary Version	Xut	Tugz	Liujy
1.0	2025-03-29	Official Version	Wangar	Yangxx	Liujy