8-bit D-type Transparent Latch with 3-state Outputs

Description

The ET74HC573 is an 8-bit D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable ($\overline{OE}$) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features

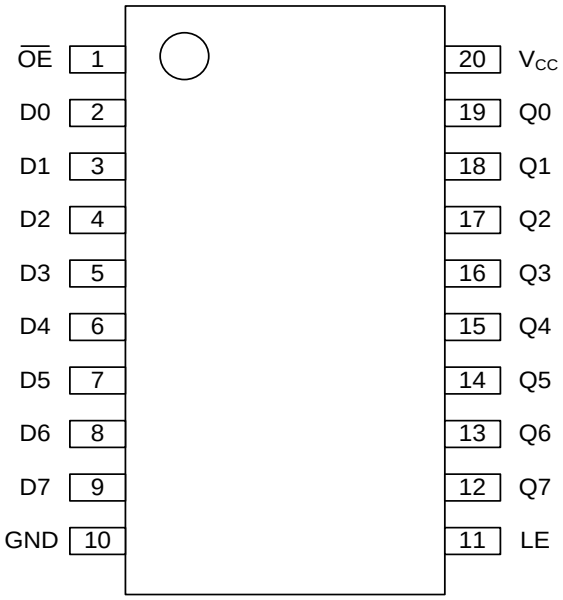
- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels: CMOS level
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors and microcomputers
- 3-state non-inverting outputs for bus-oriented applications
- Common 3-state output enable input
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  -- JESD8C (2.7 V to 3.6 V)
  -- JESD7A (2.0 V to 6.0 V)
- ESD Performance:
  -- HBM >2000V
  -- CDM >1000V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Part No. and Package

Product Name	Package
ET74HC573M	SOP20
ET74HC573V	TSSOP20

Applications

- Memory chip select decoding
- Data transmission system

Pin Configuration



SOP20/TSSOP20

TOP VIEW

Pin Function

Pin Number	Pin Symbol	Description
1	$\overline{OE}$	3-state output enable input (active LOW)
2-9	D0-A7	Data input
10	GND	GND
11	LE	latch enable input (active HIGH)
12-19	Q7-Q0	3-state latch output
20	V_{CC}	Supply Voltage

Block Diagram

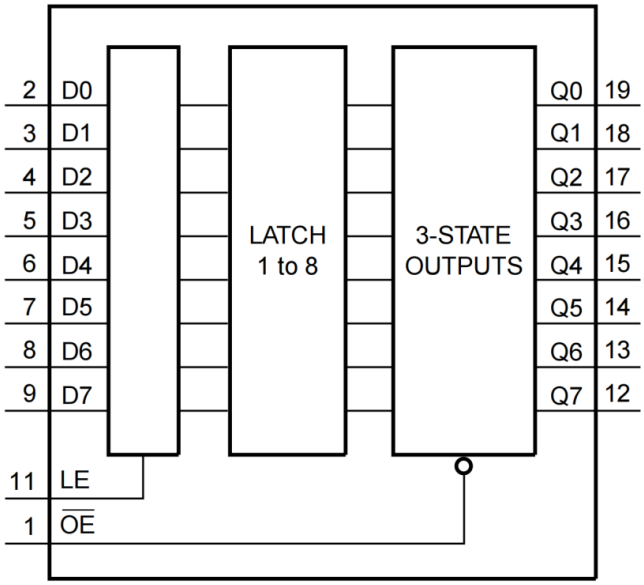


Figure 1. Functional diagram

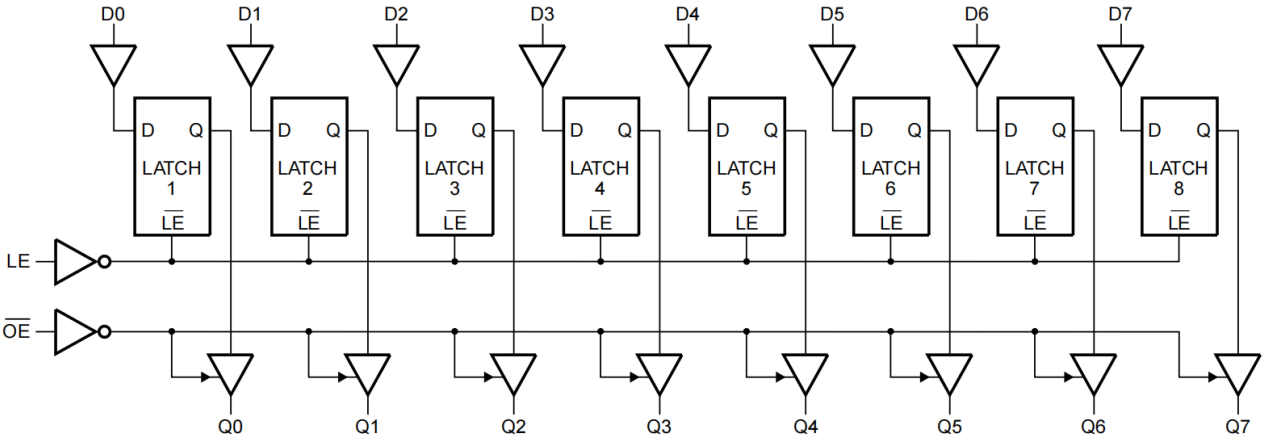


Figure 2. Logic diagram

Functional Description

Operating mode	Control		Input	Intemal latches	Output
	$\overline{OE}$	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	L	l	L	Z
			h	H	Z

Note: H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition, L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition, Z = High-impedance OFF-state.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		-0.5	+7	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{IK}	Input clamping current	V_I< -0.5 V or V_I> V_{CC} + 0.5 V	-	±20	mA
I_{OK}	Output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	-	±20	mA
I_O	Output current	V_O = -0.5 V to (V_{CC} + 0.5 V)	-	±35	mA
I_{CC}	Supply current		-	±70	mA
I_{GND}	Ground current		-70	-	mA
T_{STG}	Storage temperature		-65	+150	°C
P_D	Total power dissipation		-	500	mW

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Conditions	25°C			-40°C to +85°C		-40°C to +125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20μA;V_{CC} = 2.0V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20μA;V_{CC} = 4.5V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20μA;V_{CC} = 6.0V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -6.0mA;V_{CC} = 4.5V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -7.8mA;V_{CC} = 6.0V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20μA;V_{CC} = 2.0V	-	0	0.1	-	0.1	-	0.1	V
		I_O = -20μA;V_{CC} = 4.5V	-	0	0.1	-	0.1	-	0.1	V
		I_O = -20μA;V_{CC} = 6.0V	-	0	0.1	-	0.1	-	0.1	V
		I_O = -6.0mA;V_{CC} = 4.5V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = -7.8mA;V_{CC} = 6.0V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND V_{CC} = 6.0V	-	-	±0.1	-	±0.1	-	±1.0	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 6.0V V_O = V_{CC} or GND	-	-	±0.5	-	±0.5	-	±10	μA
I_{CC}	Supply current	V_I = V_{CC} or GND I_O = 0 A;V_{CC} = 6.0V	-	-	8.0	-	8.0	-	160	μA
C_I	Input capacitance		-	3.5	-					pF

Dynamic Characteristics (C_L=50pF unless otherwise specified)

Symbol	Parameter	Conditions	25°C			-40°C to +85°C		-40°C to +125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	Propagation delay	Dn to Qn								
		V_{CC} = 2.0V	-	47	150	-	190	-	225	ns
		V_{CC} = 4.5V	-	17	30	-	38	-	45	ns
		V_{CC} = 5V;C_L = 15pF	-	14	-	-	-	-	-	ns
		V_{CC} = 6.0V	-	14	26	-	33	-	38	ns
		LE to Qn								
		V_{CC} = 2.0V	-	50	150	-	190	-	225	ns
		V_{CC} = 4.5V	-	18	30	-	38	-	45	ns
		V_{CC} = 5V;C_L = 15pF	-	15	-	-	-	-	-	ns
		V_{CC} = 6.0V	-	14	26	-	33	-	38	ns
t_{en}	Enable time	OE to Qn								
		V_{CC} = 2.0V	-	44	140	-	175	-	210	ns
		V_{CC} = 4.5V	-	16	28	-	35	-	42	ns
		V_{CC} = 6.0V	-	13	24	-	30	-	36	ns
t_{dis}	Disable time	OE to Qn								
		V_{CC} = 2.0V	-	55	150	-	190	-	225	ns
		V_{CC} = 4.5V	-	20	30	-	38	-	45	ns
		V_{CC} = 6.0V	-	16	26	-	33	-	38	ns
t_t	Transition time	Qn								
		V_{CC} = 2.0V	-	14	60	-	75	-	90	ns
		V_{CC} = 4.5V	-	5	12	-	15	-	18	ns
		V_{CC} = 6.0V	-	4	10	-	13	-	15	ns
t_w	Pulse width	LE HIGH								
		V_{CC} = 2.0V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5V	16	5	-	20	-	24	-	ns
		V_{CC} = 6.0V	14	4	-	17	-	20	-	ns
t_{su}	Set_up time	Dn to LE								
		V_{CC} = 2.0V	50	11	-	65	-	75	-	ns
		V_{CC} = 4.5V	10	4	-	13	-	15	-	ns
		V_{CC} = 6.0V	9	3	-	11	-	13	-	ns
t_h	Hold time	Dn to LE								
		V_{CC} = 2.0V	5	3	-	5	-	5	-	ns
		V_{CC} = 4.5V	5	1	-	5	-	5	-	ns
		V_{CC} = 6.0V	5	1	-	5	-	5	-	ns
C_{PD}	Power dissipation capacitance	C_L = 50pF; f = 1MHz; V_I = GND to V_{CC}	-	26	-	-	-	-	-	pF

Dynamic Characteristics Test Waveform

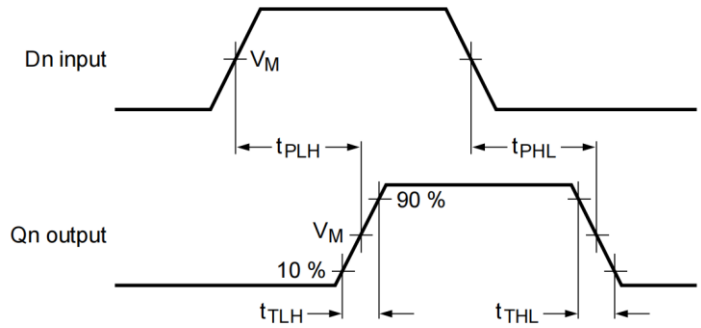


Figure 3. Propagation delay data input (Dn) to output (Qn) and output transition time

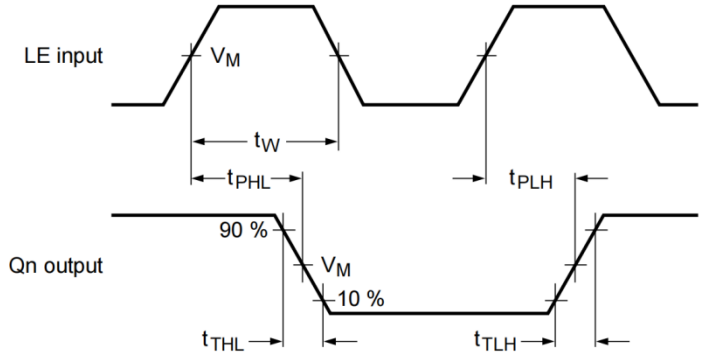


Figure 4.Pulse width latch enable input (LE),
propagation delay latch enable input (LE) to output (Qn) and output transition time

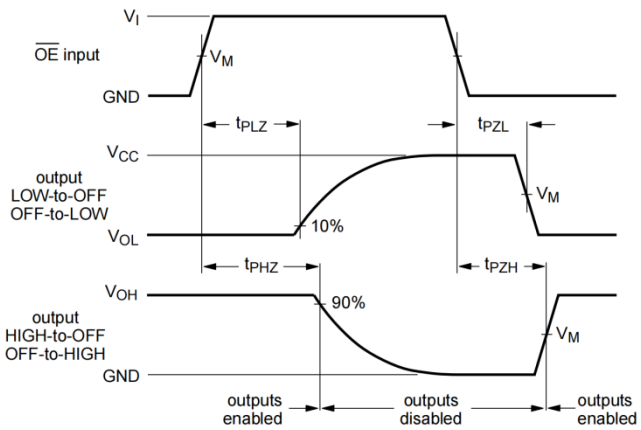


Figure 5.Enable and disable times

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

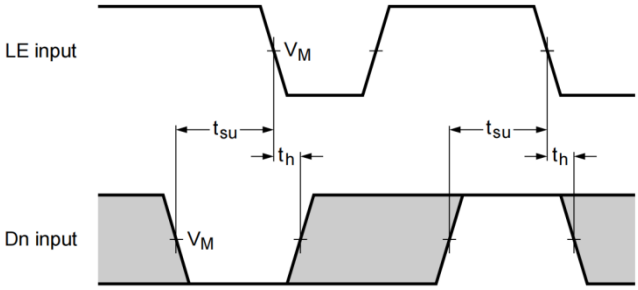


Figure 6.Set-up and hold times for data input (Dn) to latch input (LE)

The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points

Type	Input V_M	Output V_M
Value	0.5V_{CC}	0.5V_{CC}

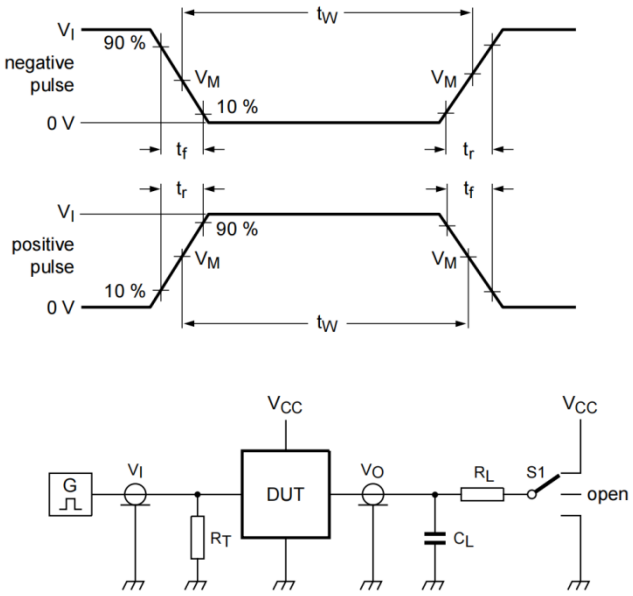


Figure 7.Test circuit for measuring switching times

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Zo of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

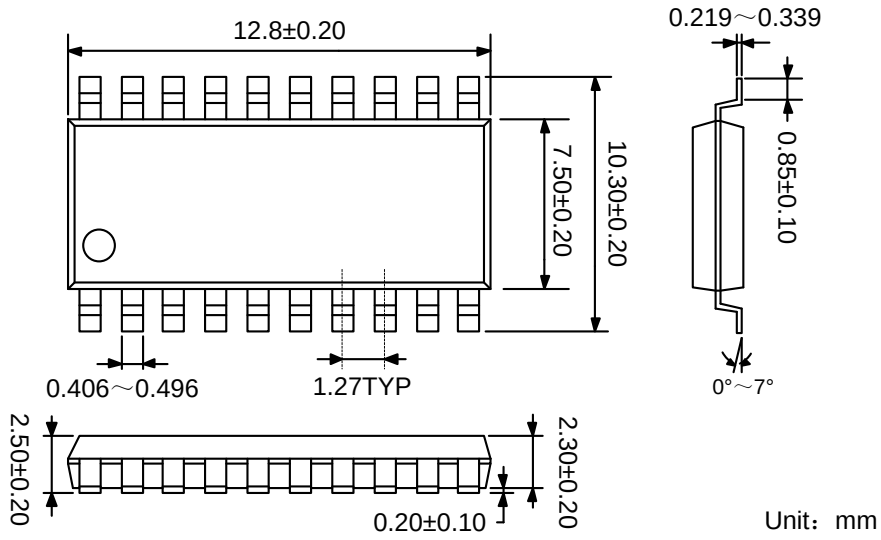
S1 = Test selection switch.

Test Data

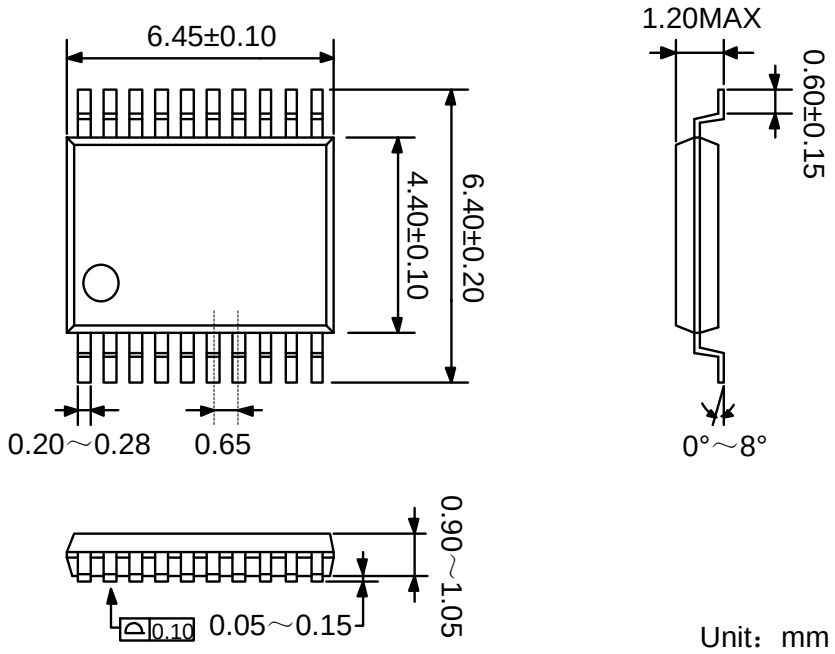
Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL},t_{PLH}	t_{PZH},t_{PHZ}	t_{PZL},t_{PLZ}
Value	V_{CC}	6ns	15pF,50pF	1kΩ	open	GND	V_{CC}

Package Dimension

SOP20(ET74HC573M)

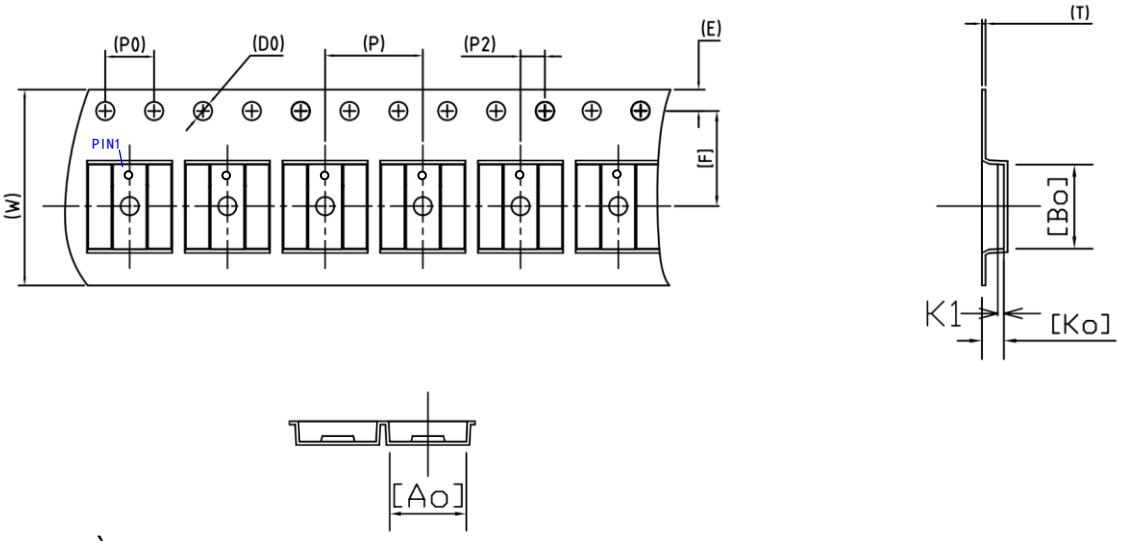


TSSOP20(ET74HC573V)



Tape Information

TSSOP20(ET74HC573V)



Item	W	A0	A1	B0	B1	K0	K1	E
Dim	16.0	6.75	0.00	6.95	0.00	1.80	0.50	1.75
Tole	+0.30 -0.30	±0.10	±0.00	±0.10	±0.00	±0.10	±0.10	±0.10
Item	F	P	P0	P2	D0	D1	T	
Dim	7.50	8.0	4.0	2.0	1.50	1.50	0.3	
Tole	±0.10	±0.10	±0.10	±0.10	+0.10 -0.00	+0.10 -0.00	±0.05	

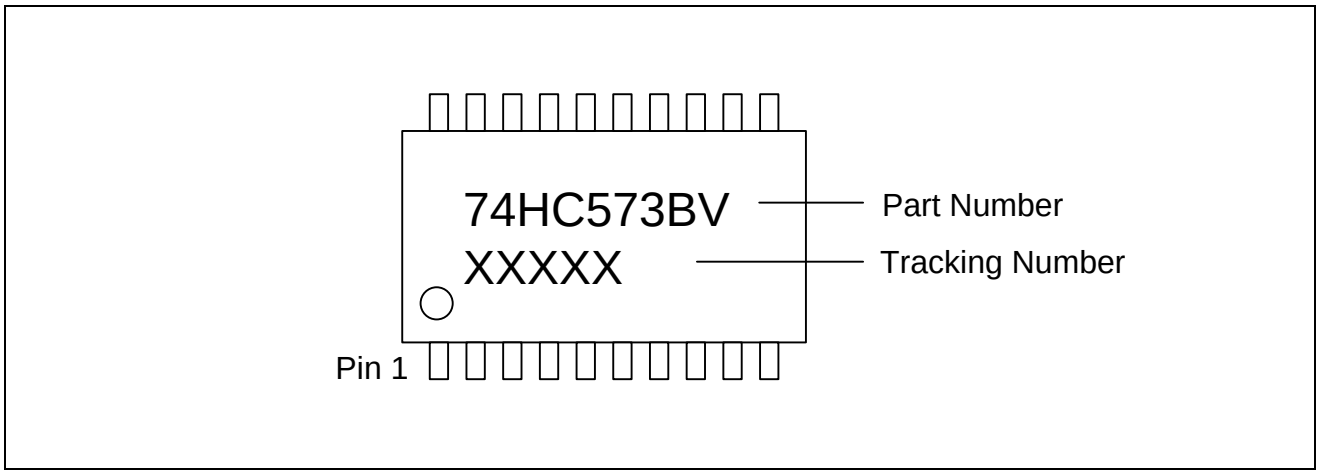
Unit: mm

Reel Information

Part No.	Package	Reel Size	Component Load
ET74HC573V	TSSOP20	13”	4000/Reel

Marking Information

TSSOP20 (ET74HC573V)



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.1	2022-10-12	Preliminary	Zhuzq Shibo	Chen Hui	Liu Jia Ying
1.0	2023-08-24	Official version Add Tape and Marking	Zhuzq	Chen Hui	Liu Jia Ying