36V, Single-Supply, General-Purpose Dual Operational Amplifier

General Description

ET85902 is a single-supply, low-noise dual operational amplifier with the ability to operate on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). The device is available in micro-packages and offer low offset, drift, and bandwidth with low quiescent current.

Unlike most operational amplifiers, which are specified at only one supply voltage, the ET85902 is specified from 2.7 to 36 V. Input signals beyond the supply rails do not cause phase reversal. The ET85902 is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. These devices can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

ET85902 is specified for the extended industrial/automotive temperature range (-40°C to +125°C). It is available in the SOP8 package.

Features

- Supply Range: 2.7 V ~ 36 V or ±1.35 V ~ ±18 V
- Low Noise: 14 nV/√Hz
- Low Offset Drift: ±0.3 μV/°C (typical)
- Input Range Includes the Negative Supply
- Input Range Operates to Positive Supply with Reduced Performance
- Rail-to-Rail Output
- Gain Bandwidth: 3 MHz
- Low Quiescent Current: 475 μA per Amplifier
- High Common-Mode Rejection: 120 dB (typical)
- Low-Input Bias Current: 8 pA

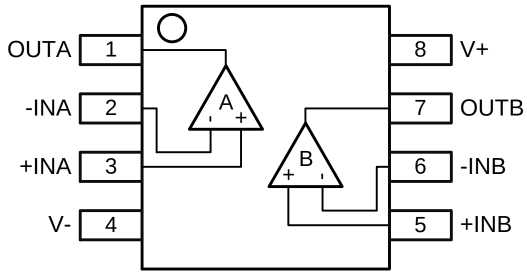
Applications

- Tracking Amplifier in Power Modules
- Merchant power supplies
- Transducer Amplifiers
- Bridge Amplifiers
- Temperature Measurements
- Test Equipment

Device Information

Part No.	Package	Tape / Reel
ET85902M	SOP8	Tape and Reel

Pin Configuration



Top View

Pin Function

Pin Number	Symbol	Descriptions
ET85902		
1,7	OUT	Output
4	V-	Negative supply
3,5	+IN	Non-inverting input
2,6	-IN	Inverting input
8	V+	Positive supply

Functional Description

Overview

ET85902 provides high overall performance, and are designed for many general purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the series offers good overall performance with high CMRR, PSRR, and AOL. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1 µF capacitors are adequate.

Functional Block Diagram

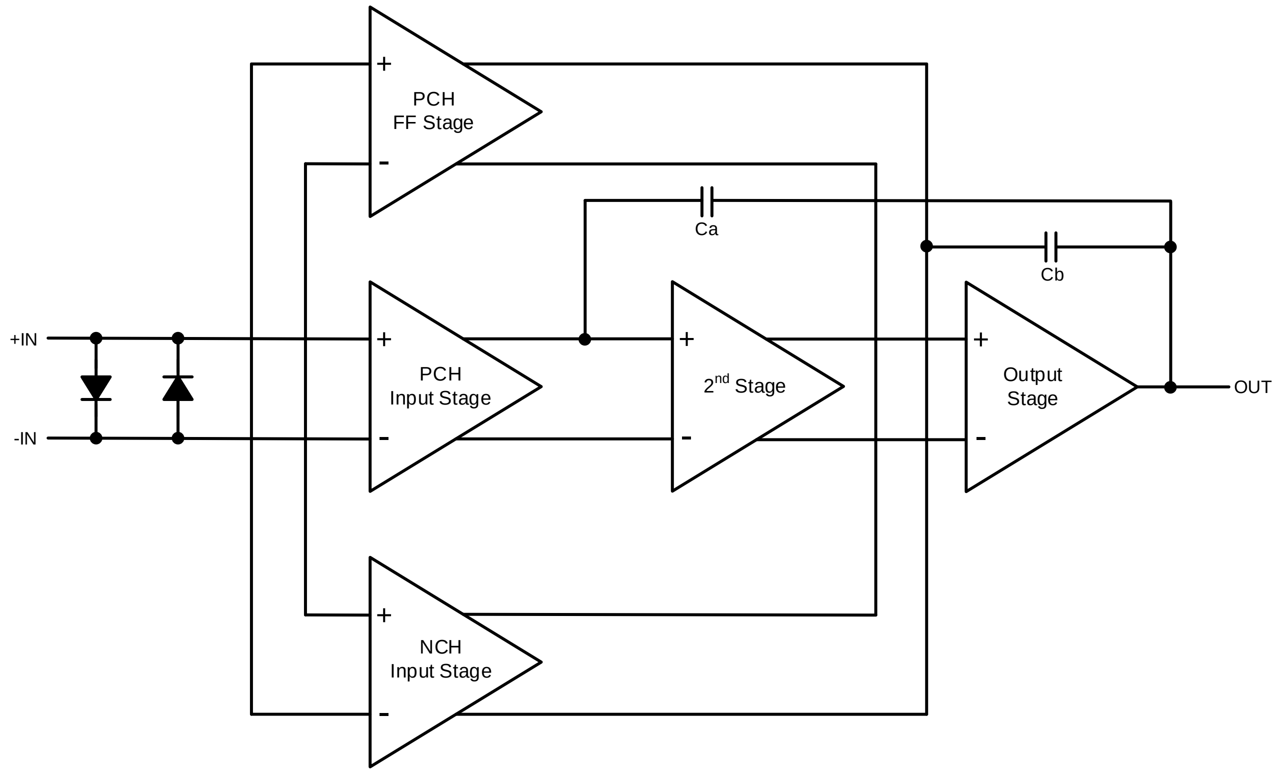


Figure 1. Functional Block Diagram

Capacitive Load and Stability

The dynamic characteristics have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output.

Operating Voltage

ET85902 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from -40°C to +125°C.

Place 0.1uF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Symbol	Parameter	Value	Unit
V_S	Supply Voltage[1]	0 ~ 40	V
V_{IN}	Signal input terminals Voltage	(V-) -0.5V ~ (V+) +0.5	V
I_{IN}	Signal input terminals Current	-10 ~ +10	mA
$T_{J(MAX)}$	Maximum Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 ~ +150	°C
V_{ESD}	HBM Max Capability[2]	±2000	V
	CDM Max Capability[2]	±1000	V
I_{LU}	Latch up Current Maximum Rating[2]	±200	mA

Note1: All voltage values, except differential voltage are with respect to network terminal.

Note2: This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per AEC-Q100-002(EIA/JESD22-A114);

CDM Charged Device Model tested per AEC-Q100-011(EIA/JESD22-C101);

Latch up Current Maximum Rating tested per AEC-Q100-004(EIA/JESD78E).

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_S	Supply Voltage: (V+) - (V-)	4.5(±2.25) ~ 36(±18)	V
T_A	Operating Temperature Range	-40 ~ +125	°C

Electrical Characteristics

V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S/2, and R_{LOAD} = 10kΩ connected to V_S/2, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFFSET VOLTAGE						
V_{OS}	Input Offset Voltage			±0.25	±1.8	mV
		T_A = -40°C to +125°C		±0.3	±2	mV
dV_{OS}/dT	V_{OS} vs Temperature	T_A = -40°C to +125°C		±0.3	±2	μV/°C
PSRR	Power Supply Rejection Ratio	V_S = 4 to 36 V, T_A = -40°C to +125°C		±1		μV/V
INPUT BIAS CURRENT						
I_B	Input Bias Current			±8		pA
		T_A = -40°C to +125°C			±3.5	nA
I_{OS}	Input Offset Current			±4		pA
		T_A = -40°C to +125°C			±3.5	nA
NOISE						
E_n	Input Voltage Noise	f = 0.1 Hz to 10 Hz		3		$μV_{PP}$
e_n	Input Voltage Noise Density	f = 100 Hz		25		nV/√Hz
		f = 1 kHz		14		nV/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode Voltage Range[3]		(V-) - 0.1		(V+) - 2	V
CMRR	Common-mode Rejection Ratio	V_S = ±2 V, (V-) - 0.1 V < V_{CM} < (V+) - 2 V, T_A = -40°C to +125°C		104		dB
		V_S = ±18 V, (V-) - 0.1 V < V_{CM} < (V+) - 2 V, T_A = -40°C to +125°C		120		dB
INPUT IMPEDANCE						
Z_{ID}	Differential[4]			100 || 3		MΩ || pF
Z_{IC}	Common-mode[4]			6 || 3		10^{12}Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop Voltage Gain	V_S = 4 V to 36 V, (V-) + 0.35V < V_O < (V+) - 0.35V, T_A = -40°C to +125°C		130		dB

Electrical Characteristics (Continued)

V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S/2, and R_{LOAD} = 10kΩ connected to V_S/2,T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FREQUENCY RESPONSE						
GBP	Gain Bandwidth Product			3		MHz
SR	Slew Rate	G = 1		1.5		V/μs
t_S	Settling Time(4)	To 0.1%, V_S = ±18 V, G = 1, 10 V step		6		μs
		To 0.01% (12 bit), V_S = ±18 V, G = 1, 10 V step		10		μs
t_{OR}	Overload Recovery Time	V_{IN} × gain > V_S		2		μs
THD+N	Total Harmonic Distortion + Noise	G = 1, f = 1 kHz, V_O = 3 V_{RMS}		0.0002		%
OUTPUT						
V_O	Voltage Output Swing From Rail	R_L = 10 kΩ	(V-) + 0.35		(V+) - 0.35	V
I_{SC}	Short-circuit Current	Sourcing		+25		mA
		Sinking		-35		
R_O	Open-loop Output Resistance(4)	f = 1 MHz,I_O = 0 A		150		Ω
POWER SUPPLY						
V_S	Specified Voltage Range		2.7		36	V
I_Q	Quiescent Current per Amplifier	I_O = 0 A		475	595	μA
		I_O = 0 A, T_A = -40°C to +125°C			650	μA

Note3: The input range can be extended beyond (V+) - 2 V up to V+.

Note4: Guaranteed by design.

Application Notes

The ET85902 provides high overall performance, making the device ideal for many general-purpose applications. and are designed for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the series offers good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1 µF capacitors are adequate.

Layout Guidelines

For best operational performance of the devices, good printed circuit board (PCB) layout practices are recommended. Low-loss, 0.1 µF bypass capacitors must be connected between each supply pin and ground, placed as close to the devices as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

Typical Applications

The ET85902 device can be used capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open loop gain of the system to ensure the circuit has sufficient phase margin.

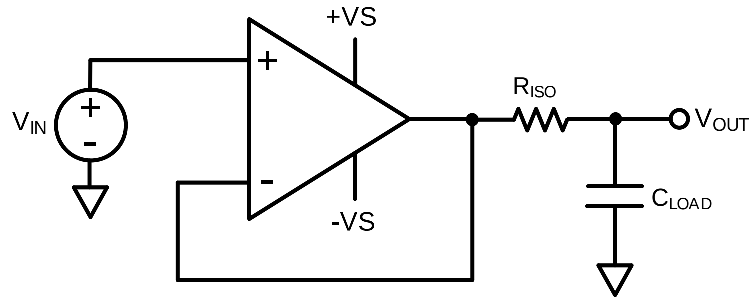
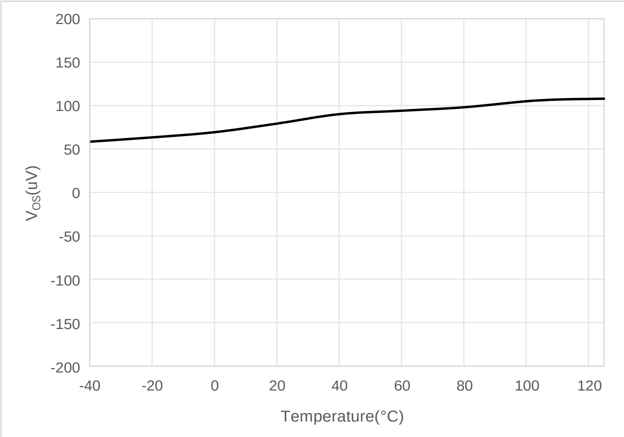


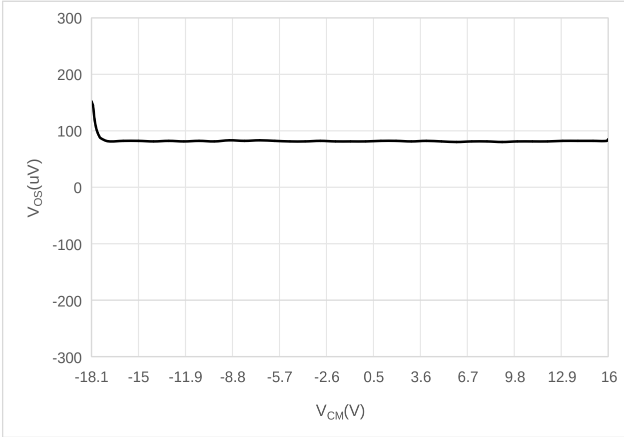
Figure 2. Unity-Gain Buffer with RISO Stability Compensation

Typical Characteristics

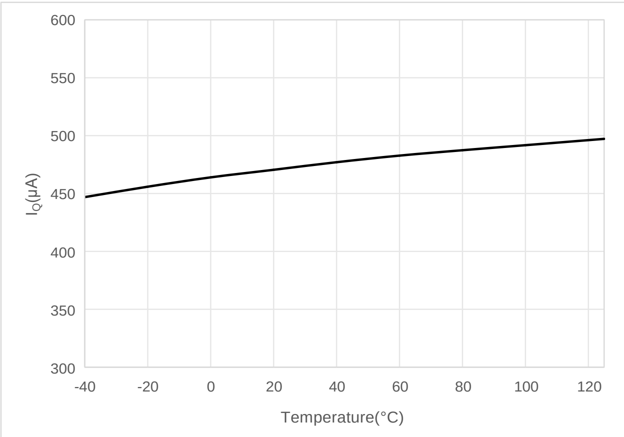
V_S = ±18 V, V_{CM} = V_{OUT} = V_S/2, and R_{LOAD} = 10kΩ connected to V_S/2,T_A = 25°C (unless otherwise noted)



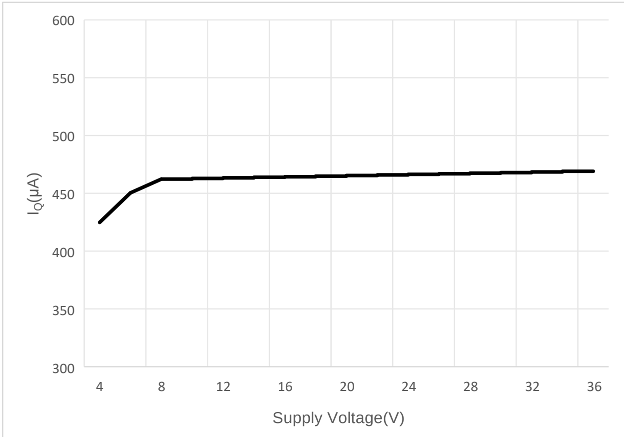
Offset Voltage vs Temperature



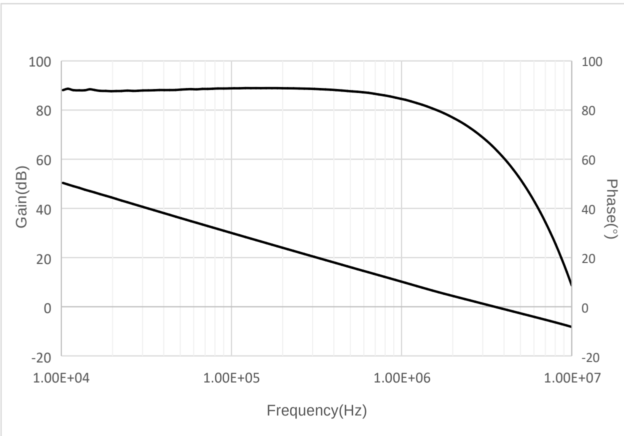
Offset Voltage vs Common-Mode Voltage



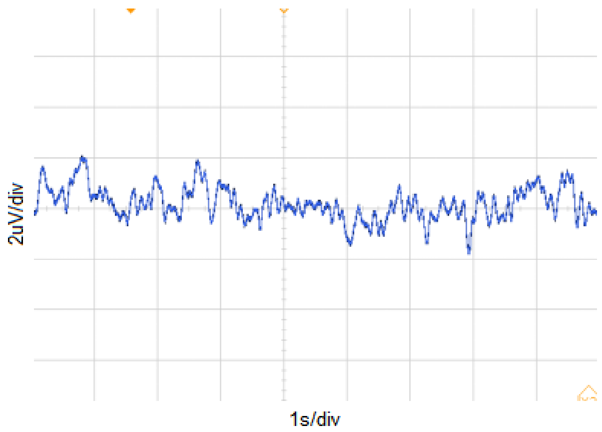
Quiescent Current vs Temperature



Quiescent Current vs Supply Voltage



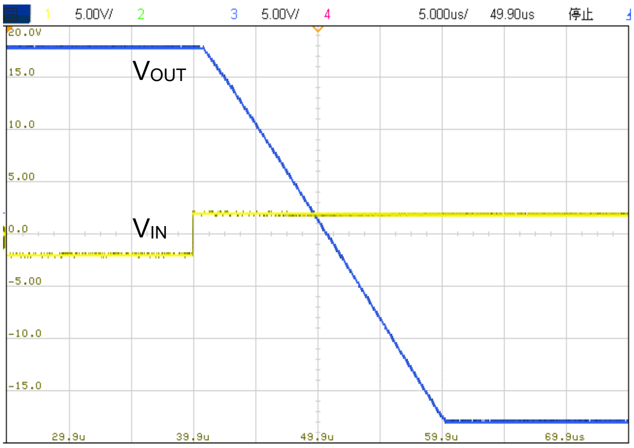
Open-Loop Gain and Phase vs Frequency



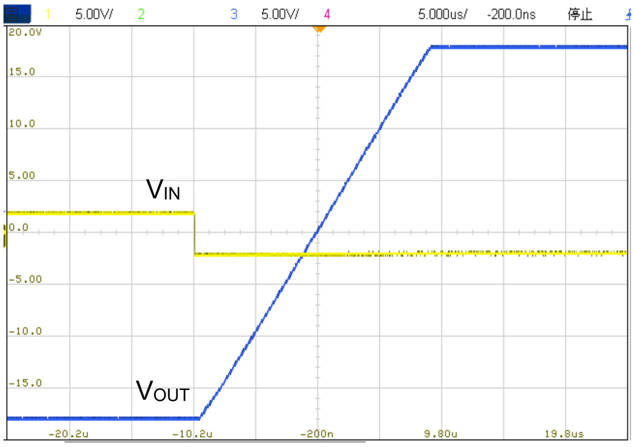
0.1 Hz to 10 Hz Noise

Typical Characteristics (Continued)

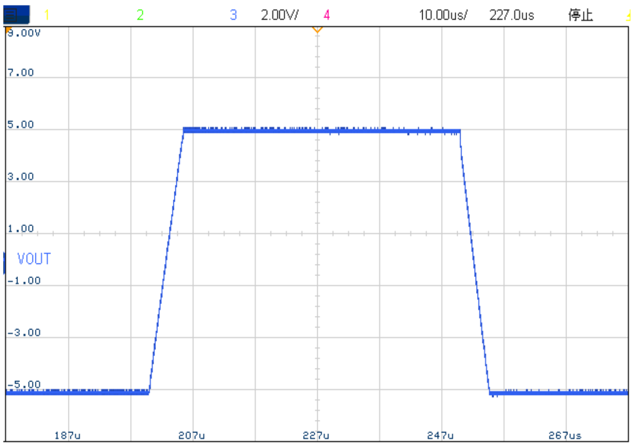
V_S = ±18 V, V_{CM} = V_{OUT} = $V_S/2$, and R_{LOAD} = 10kΩ connected to $V_S/2$, T_A = 25°C (unless otherwise noted)



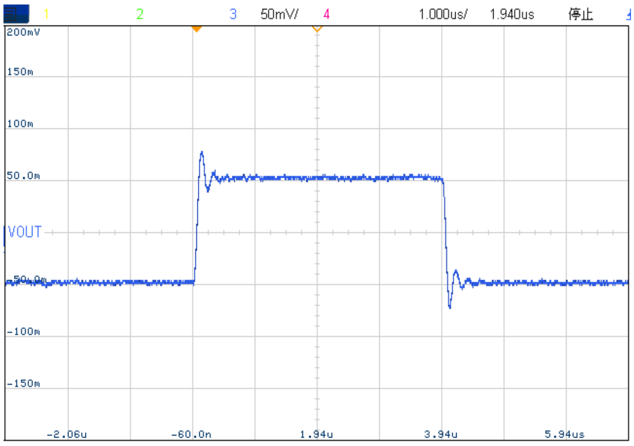
Positive Overload Recovery
(G = -10)



Negative Overload Recovery
(G = -10)



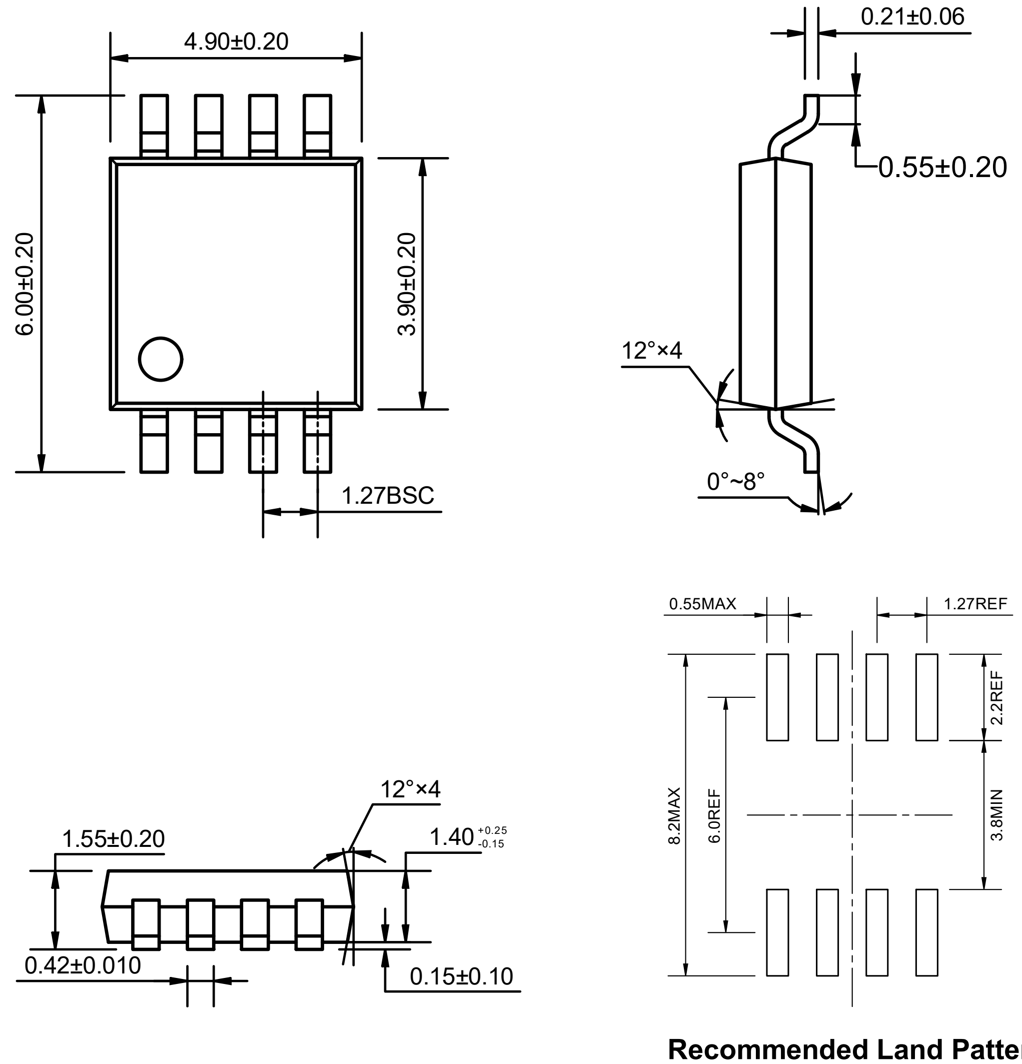
Large-Signal Step Response
(G = +1, R_L = 10 kΩ, C_L = 100 pF)



Small-Signal Step Response(100 mV)
(G = +1, R_L = 10 kΩ, C_L = 100 pF)

Package Dimension

SOP8



Recommended Land Pattern

Unit: mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-5-10	Preliminary Version	Huyt	Wanggp	Liujy
1.0	2024-11-4	Original Version	Huyt	Wanggp	Liujy